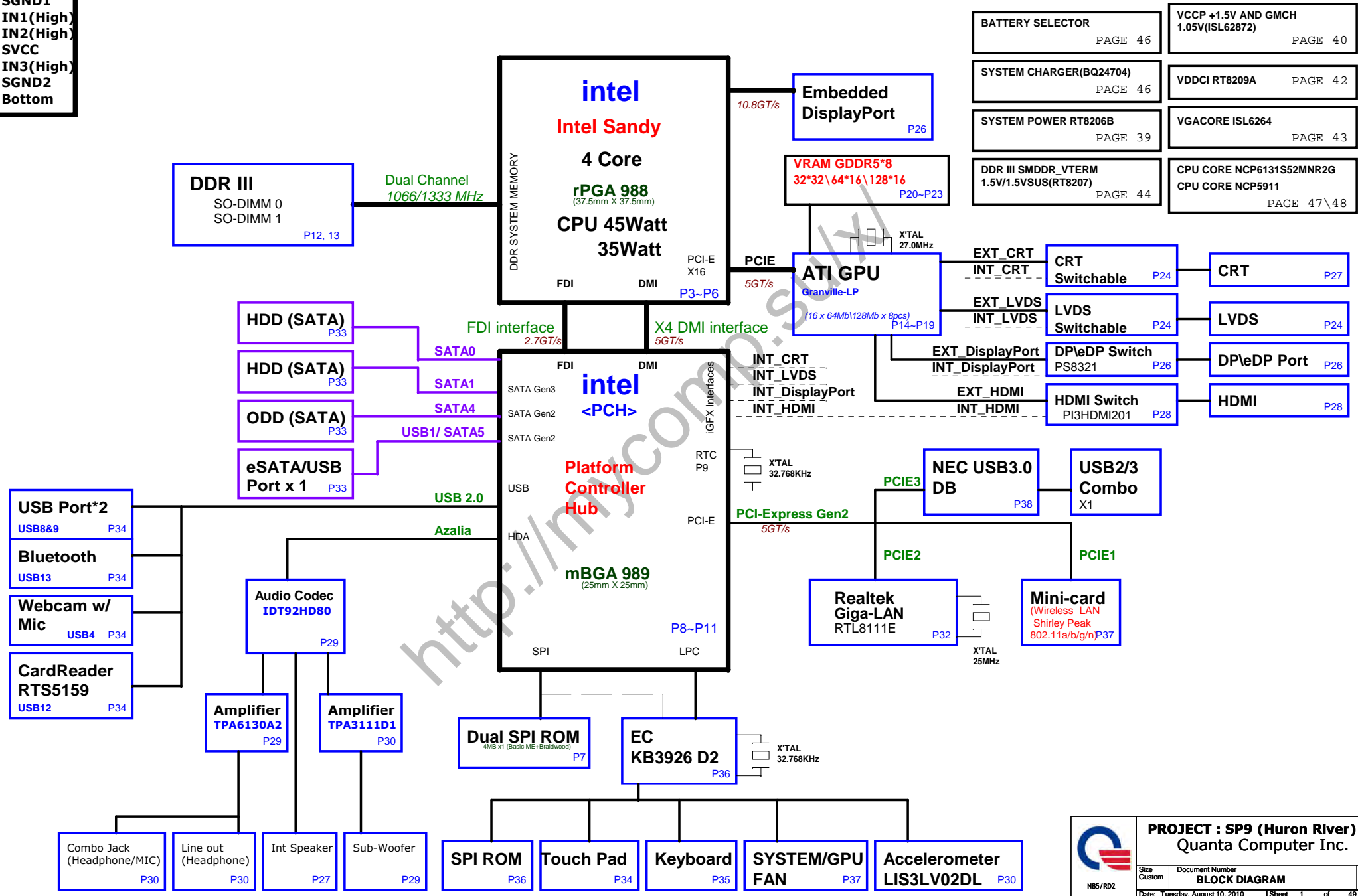


- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1(High)
- LAYER 4 : IN2(High)
- LAYER 5 : SVCC
- LAYER 6 : IN3(High)
- LAYER 7 : SGND2
- LAYER 8 : Bottom

SP9 BLOCK DIAGRAM

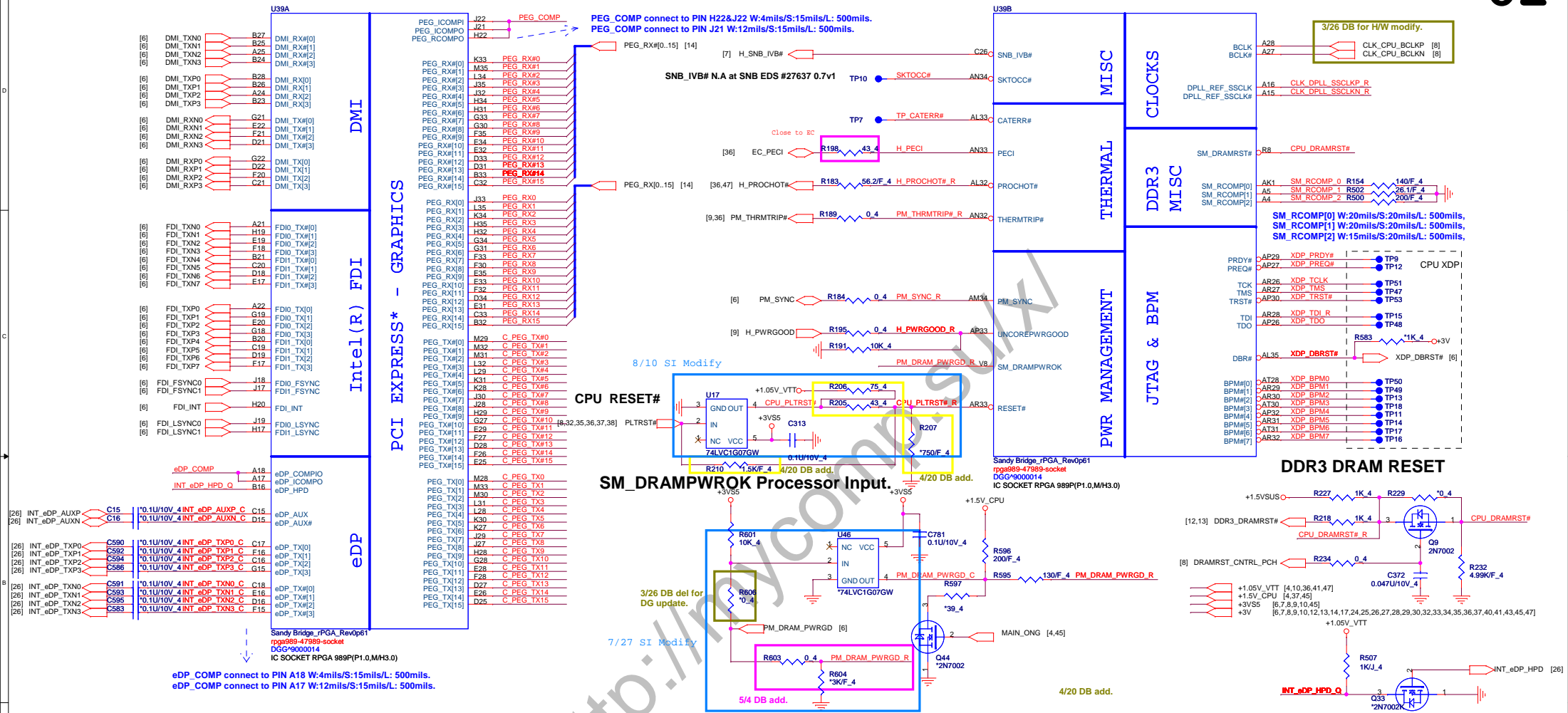


BATTERY SELECTOR PAGE 46	VCCP +1.5V AND GMCH 1.05V(ISL62872) PAGE 40
SYSTEM CHARGER(BQ24704) PAGE 46	VDDCI RT8209A PAGE 42
SYSTEM POWER RT8206B PAGE 39	VGACORE ISL6264 PAGE 43
DDR III SMDDR_VTERM 1.5V/1.5VSUS(RT8207) PAGE 44	CPU CORE NCP6131S52MMNR2G CPU CORE NCP5911 PAGE 47\48

	PROJECT : SP9 (Huron River)		Rev 1A
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Sandy Bridge Processor (DMI,PEG,FDI)

Sandy Bridge Processor (CLK,MISC,JTAG)



3/26 DB for HW modify.
 A28 CLK_CPU_BCLKP [8]
 A27 CLK_CPU_BCLKN [9]
 A16 CLK_DPLL_SSCCLKP R
 A15 CLK_DPLL_SSCCLKN R

R8 CPU_DRAMRST#
 AK1 SM_RCOMP0 R154 140/F 4
 A5 SM_RCOMP1 R502 261/F 4
 A4 SM_RCOMP2 R500 200/F 4

SM_RCOMP[0] W:20mils/S:20mils/L: 500mils
 SM_RCOMP[1] W:20mils/S:20mils/L: 500mils
 SM_RCOMP[2] W:15mils/S:20mils/L: 500mils

DDR3 DRAM RESET
 +1.5VSTUS R227 1K 4 R229 *0.4
 [12,13] DDR3_DRAMRST# R218 1K 4 3 CPU_DRAMRST# R
 [8] DRAMRST_CNTRL_PCH R234 0.4
 +1.05V_VTT [4,10,36,41,47]
 +1.5V_CPU [4,37,45]
 +3VS5 [6,7,8,9,10,45]
 +3V [6,7,8,9,10,12,13,14,17,24,25,26,27,28,29,30,32,33,34,35,36,37,40,41,43,45,47]
 C372 0.047U/10V_4
 R232 4.98K/F_4
 Q8 2N7002
 R597 1K/U_4
 Q3 2N7002K
 INT_eDP_HPD_Q [26]

SM_DRAMPWROK Processor Input.
 U17 +1.05V_VTT
 GND OUT 3
 IN 4 CPU_PLTRST# R206 75.4
 +3VS5 C313
 NC VCC 5
 74LVC1G07GW
 PLTRST# 2
 R207 750/F_4
 R210 1.5K/F_4 4/20 DB add.
 R205 43.4
 CPU_PLTRST# R
 4/20 DB add.

7/27 SI Modify
 R601 10K_4
 U46 74LVC1G07GW
 NC VCC 3
 IN 5
 GND OUT 4
 PM_DRAM_PWRGD R
 R597 *39_4
 R596 200/F_4
 R595 130/F_4 PM_DRAM_PWRGD R
 MAIN_ONG [4,45]
 Q44 2N7002
 R603 0.4 PM_DRAM_PWRGD R
 R604 *3K/F_4
 4/20 DB add.

Embedded Display PLL Clock

CLK_DPLL_SSCCLKP R 3
 CLK_DPLL_SSCCLKN R 2
 0.4P2R_4
 CLK_DPLL_SSCCLKP R
 CLK_DPLL_SSCCLKN R

Ra R5 R5
 Rb R50 R50
 Rc R50 R50

	Ra	Rb	Rc
DIS	NC	Stuff	Stuff
SG/UMA	Stuff	NC	NC

DP & PEG Compensation/ Hot-plug

+1.05V_VTT_ R503 24.9/F 4 eDP_COMP
 eDP_COMPO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms
 +1.05V_VTT_ R66 24.9/F 4 PEG_COMP
 PEG_ICOMPI and RCOMP0 signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

Processor pull-up (CPU)

+1.05V_VTT
 H_PROCHOT# R186 52.4
 XDP_TDO R591 51.4
 XDP_TMS R588 51.4
 XDP_TDI_R R200 51.4
 XDP_PREQ# R205 51.4
 XDP_TCLK R592 51.4
 XDP_TRST# R587 51.4

FDI disable (DIS only stuff)

FDI_INT
 R185 *0.4 FDI_FSYNCO
 R184 *0.4 FDI_FSYNCT
 R190 *0.4 FDI_LSYNCO
 R187 *1K 4
 R180 *1K 4

FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (DG V0.5 Ch2.2.9).

PEG x16 disable (UMA only remove)

[14] PEG_TX[0..15] PEG_TX0 C778 0.1U/10V_4
 PEG_TX1 C770 0.1U/10V_4
 PEG_TX2 C773 0.1U/10V_4
 PEG_TX3 C771 0.1U/10V_4
 PEG_TX4 C766 0.1U/10V_4
 PEG_TX5 C762 0.1U/10V_4
 PEG_TX6 C769 0.1U/10V_4
 PEG_TX7 C768 0.1U/10V_4
 PEG_TX8 C763 0.1U/10V_4
 PEG_TX9 C748 0.1U/10V_4
 PEG_TX10 C745 0.1U/10V_4
 PEG_TX11 C743 0.1U/10V_4
 PEG_TX12 C734 0.1U/10V_4
 PEG_TX13 C733 0.1U/10V_4
 PEG_TX14 C731 0.1U/10V_4
 PEG_TX15 C728 0.1U/10V_4

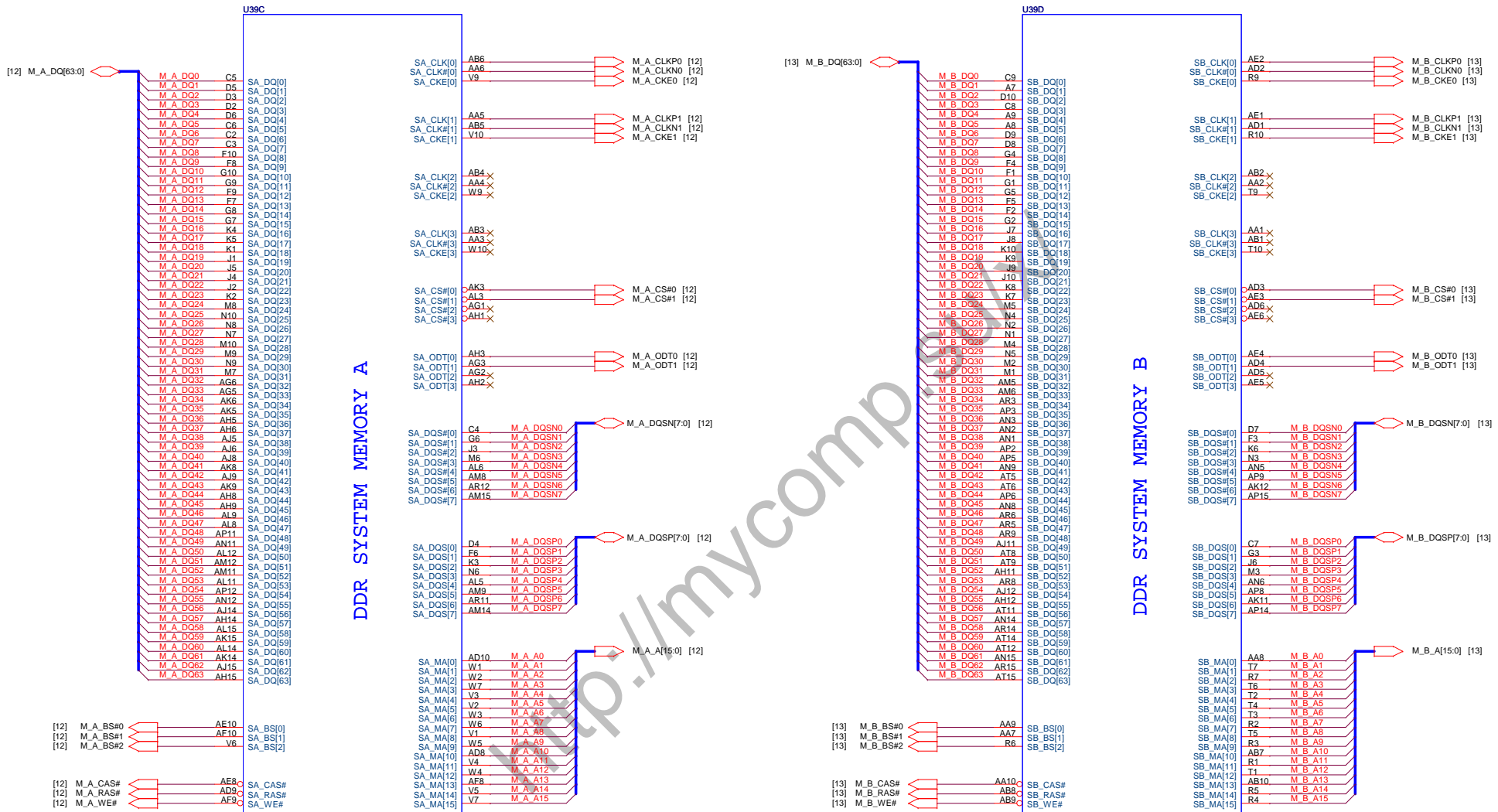
[14] PEG_TX[0..15] PEG_TX0 C780 0.1U/10V_4
 PEG_TX1 C774 0.1U/10V_4
 PEG_TX2 C775 0.1U/10V_4
 PEG_TX3 C776 0.1U/10V_4
 PEG_TX4 C764 0.1U/10V_4
 PEG_TX5 C760 0.1U/10V_4
 PEG_TX6 C766 0.1U/10V_4
 PEG_TX7 C765 0.1U/10V_4
 PEG_TX8 C761 0.1U/10V_4
 PEG_TX9 C750 0.1U/10V_4
 PEG_TX10 C749 0.1U/10V_4
 PEG_TX11 C746 0.1U/10V_4
 PEG_TX12 C741 0.1U/10V_4
 PEG_TX13 C739 0.1U/10V_4
 PEG_TX14 C736 0.1U/10V_4
 PEG_TX15 C728 0.1U/10V_4

0.22uF AC coupling Caps for PCIe GEN1/2/3
 0.22uF AC coupling Caps for PCIe GEN1/2/3

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 Quanta Computer Inc.

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 Document Number SNB 1/4 (PCIE&DMI&FDI)
 Date: Tuesday, August 10, 2010 Sheet 2 of 49
 Rev 1A

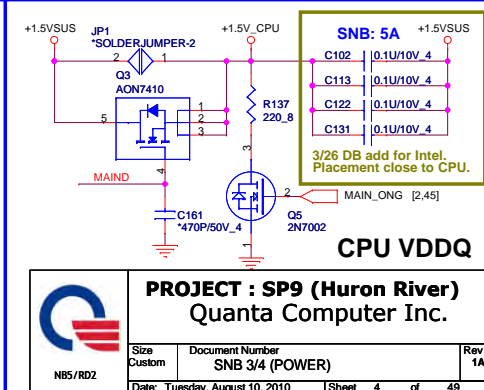
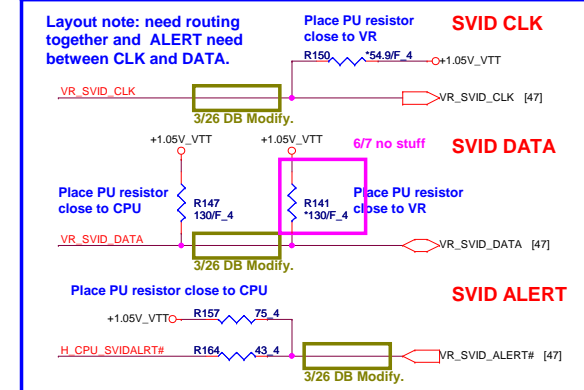
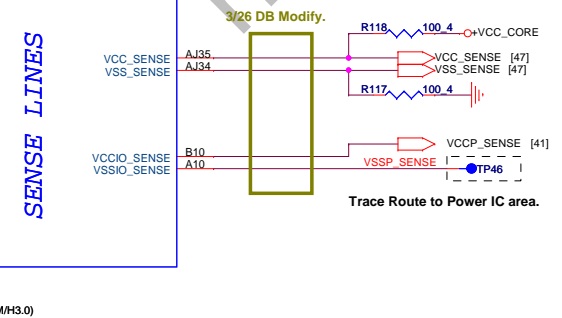
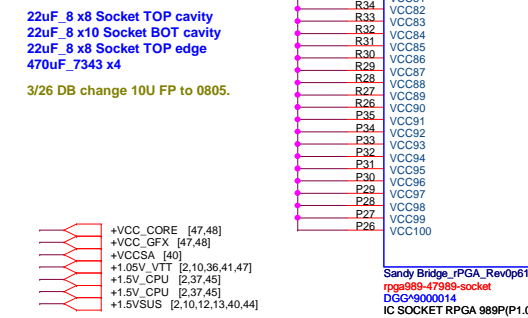
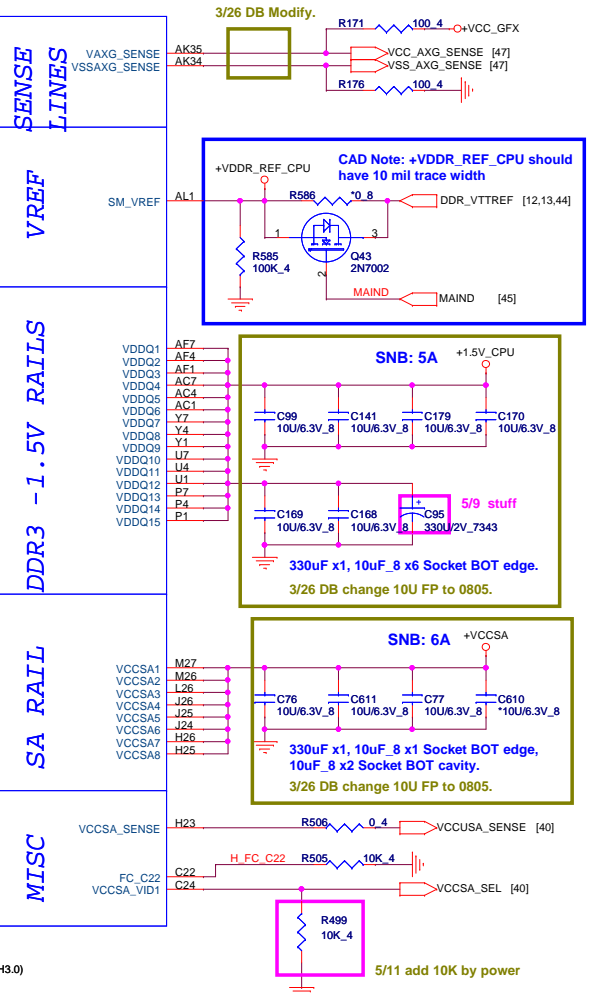
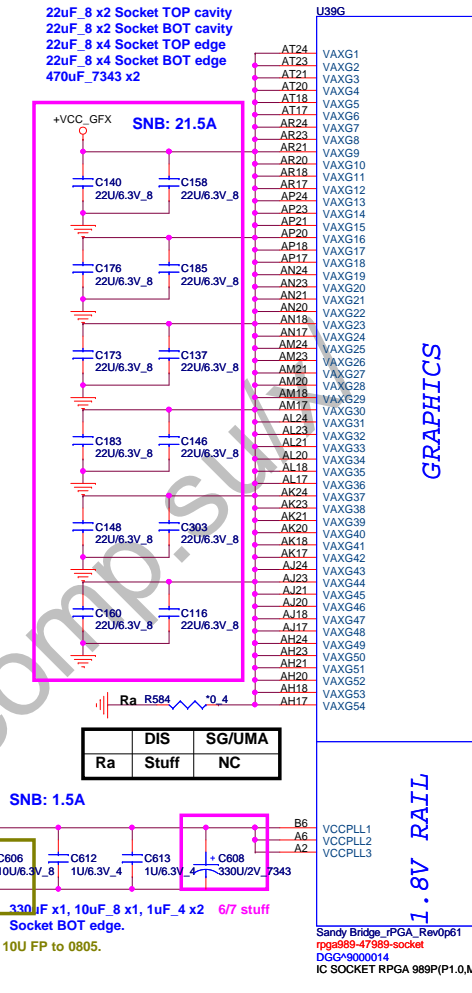
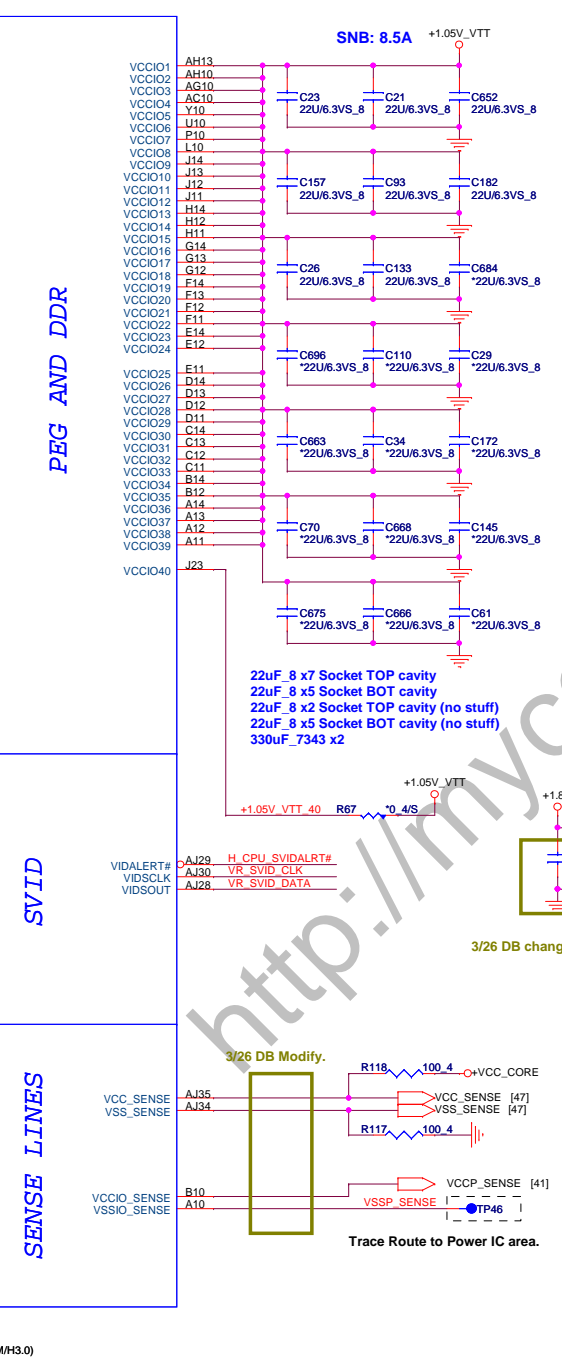
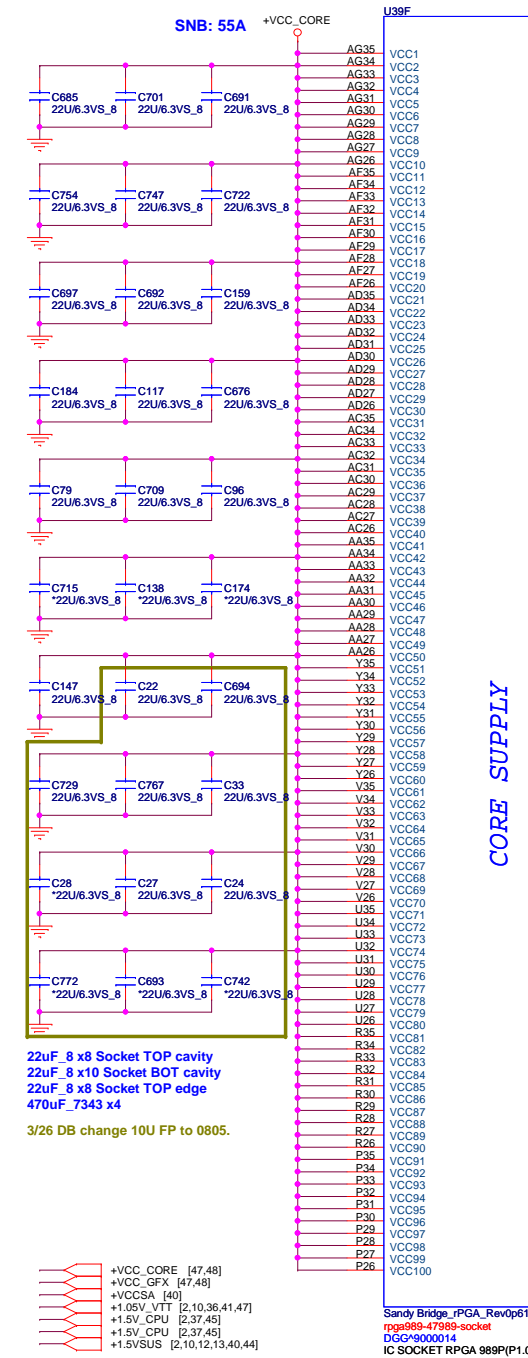
Sandy Bridge Processor (DDR3)



Sandy Bridge_rPGA_Rev0p61
 rpg989-47989-socket
 DGG-9000014
 IC SOCKET RPGA 989P(P1.0,M/H3.0)

Sandy Bridge_rPGA_Rev0p61
 rpg989-47989-socket
 DGG-9000014
 IC SOCKET RPGA 989P(P1.0,M/H3.0)

	PROJECT : SP9 (Huron River)		Rev 1A
	Quanta Computer Inc.		
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PEG AND DDR

SVID

SENSE LINES

GRAPHICS

1.8V RAIL

SENSE LINES

VREF

DDR3 - 1.5V RAILS

SA RAIL

MISC

Ra	DIS Stuff	SG/UMA NC
Ra	DIS	SG/UMA

- +VCC_CORE [47,48]
- +VCC_GFX [47,48]
- +VCCSA [40]
- +1.05V_VTT [2,10,36,41,47]
- +1.5V_CPU [2,37,45]
- +1.5V_CPU [2,37,45]
- +1.5VSUS [2,10,12,13,40,44]

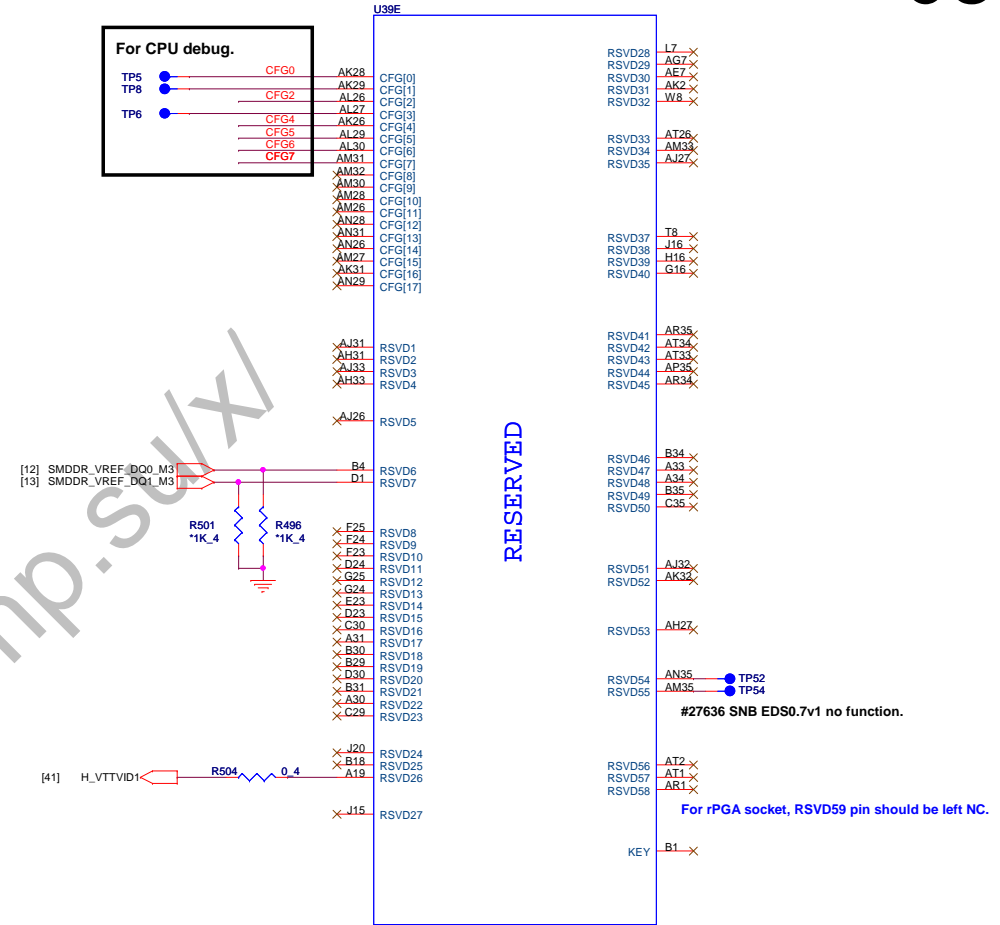
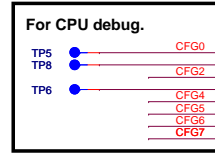
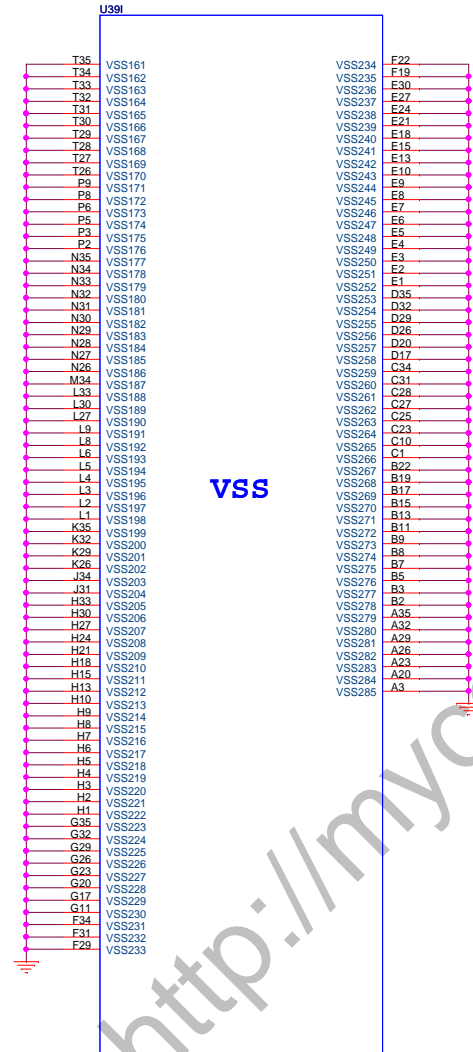
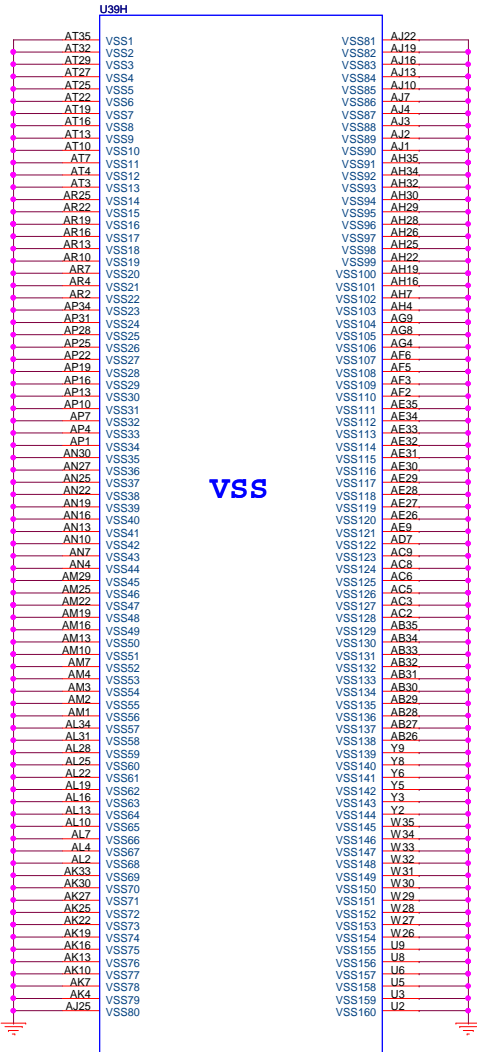
Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGG*9000014
IC SOCKET RPGA 989P(P1.0,MH3.0)

Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGG*9000014
IC SOCKET RPGA 989P(P1.0,MH3.0)



PROJECT : SP9 (Huron River)
Quanta Computer Inc.

Size Custom	Document Number SNB 3/4 (POWER)	Rev 1A
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Sandy Bridge_rPGA_Rev0p61
rpg989-47989-socket
DGG*9000014
IC SOCKET RPGA 989P(P1.0,M/H3.0)

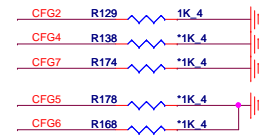
Sandy Bridge_rPGA_Rev0p61
rpg989-47989-socket
DGG*9000014
IC SOCKET RPGA 989P(P1.0,M/H3.0)

CFG[6:5] (PCIe Port Bifurcation Straps)
 11: (Default) x16 - Device 1 functions 1 and 2 disabled
 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled

Processor Strapping

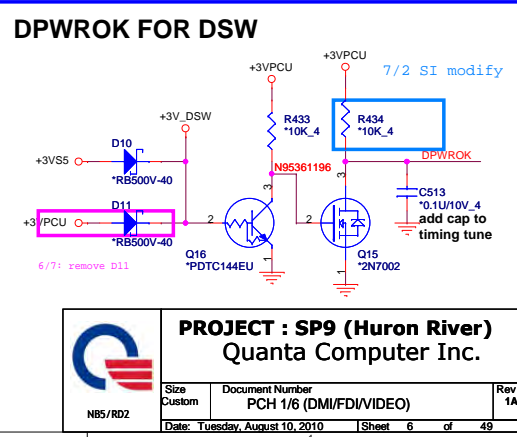
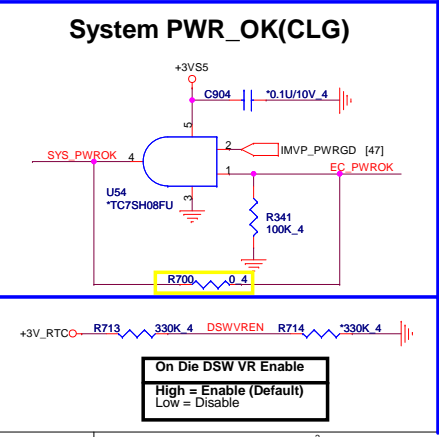
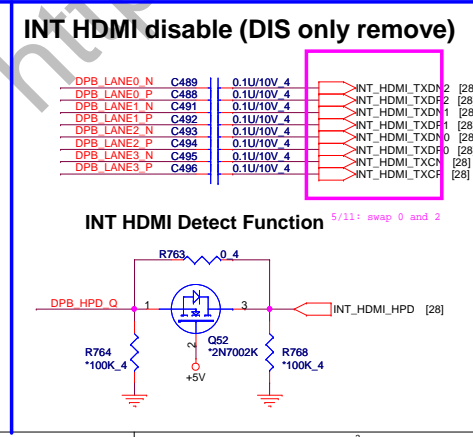
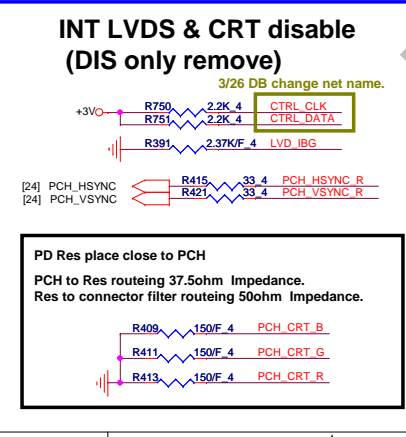
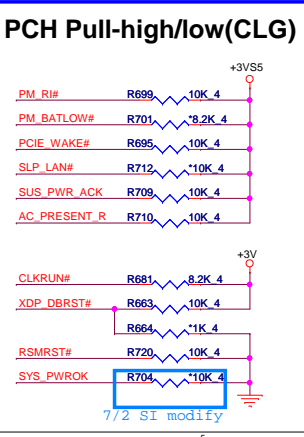
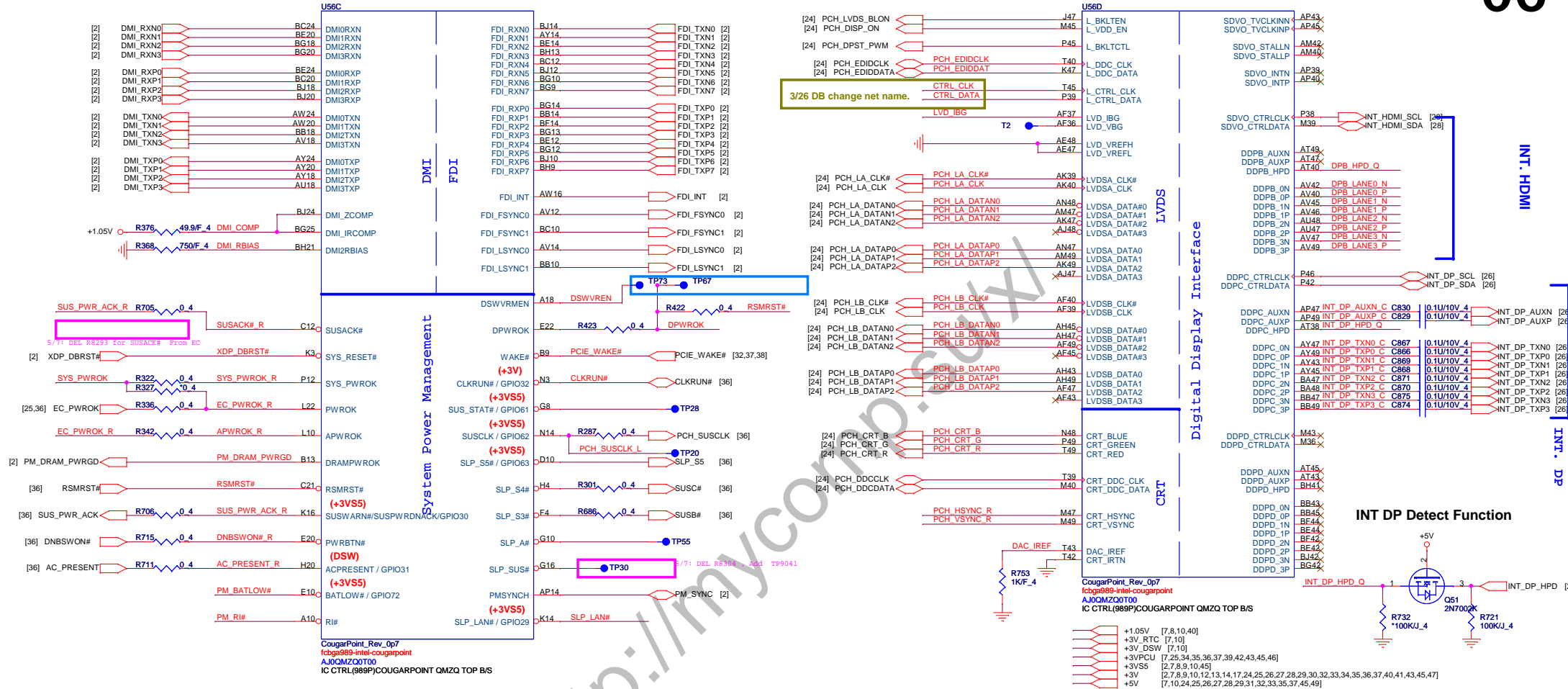
The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



PROJECT : SP9 (Huron River)
Quanta Computer Inc.

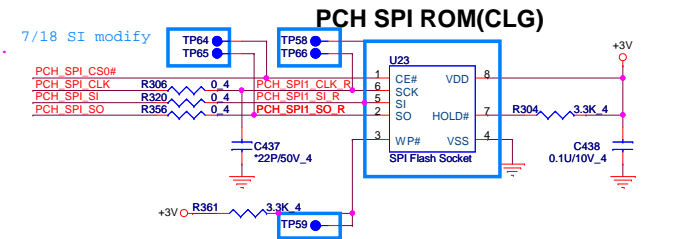
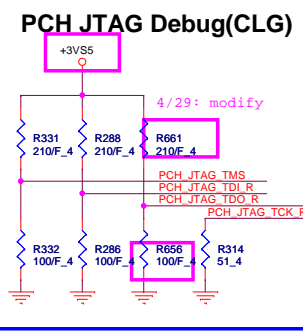
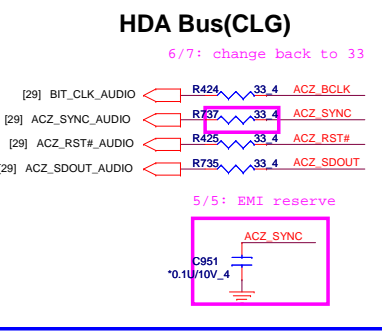
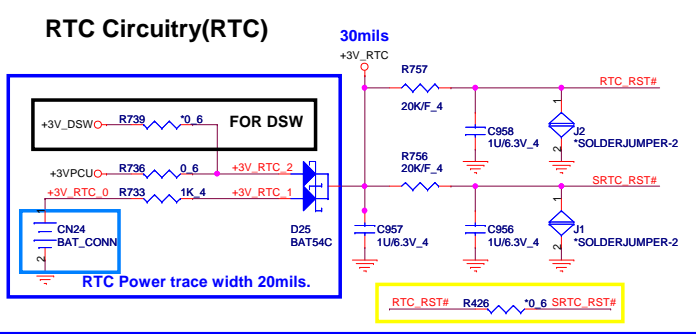
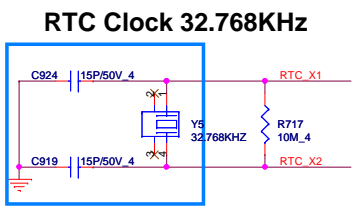
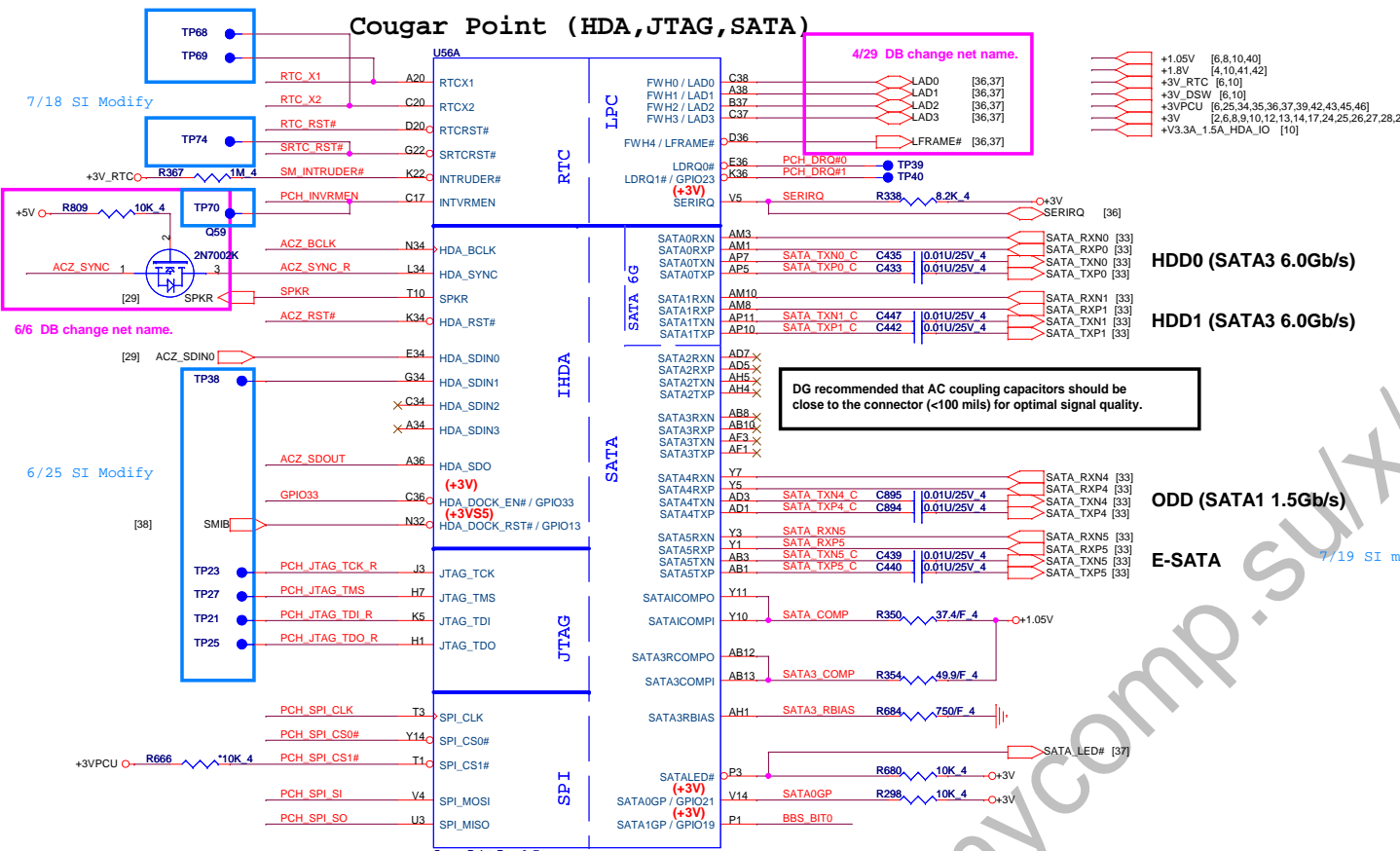
Size Custom	Document Number SNB 4/4 (GND)	Rev 1A
Date: Tuesday, August 10, 2010		Sheet 5 of 49



PROJECT : SP9 (Huron River)
Quanta Computer Inc.

Size Custom	Document Number PCH 1/6 (DMI/FDI/VIDEO)	Rev 1A
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Cougar Point (HDA,JTAG,SATA)



Vender	Size	P/N
EON	4MB	AKE39FN0Q00 (EN25F32-100HIP)
Winbond	4MB	AKE391PON00 (W25Q32BVSSIG)
Socket		DG008000031

PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR <i>Different from Calpella</i>	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	SPKR R660 *1K 4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R749 R746 *1K 4 +3V PCI_GNT3# [8]
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R716 330K 4 +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R727 1K 4 GPIO33_E [36]
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#	BBS_BIT0 R667 *1K 4 BBS_BIT0 [8]
GPIO19 <i>Different from Calpella</i>	Boot BIOS Selection 0 [bit-0]	PWROK		BBS_BIT1 R752 *1K 4 BBS_BIT1 [8]
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V R691 *1K 4 NV_ALE [8]
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm 4/30 reserve.	+1.8V R678 2.2K 4 R694 4.7K 4 NV_CLE [8]
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3VSS R734 *1K 4 ACZ_SYNC_R 5/4 add
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	ACZ_SDOUT R738 *1K 4 +V3.3A_1.5A_HDA_IO
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	R703 *1K 4 4/29 reserve. ICC_EN# [9]
GPIO28 <i>Different from Calpella</i>	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R693 *1K 4 PLL_OVR_EN [9]
SPI_MOSI	ITPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	PCH_SPI_SI R308 *1K 4 +3V

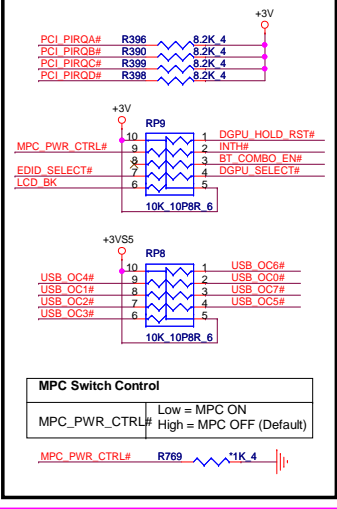


PROJECT : SP9 (Huron River)
Quanta Computer Inc.

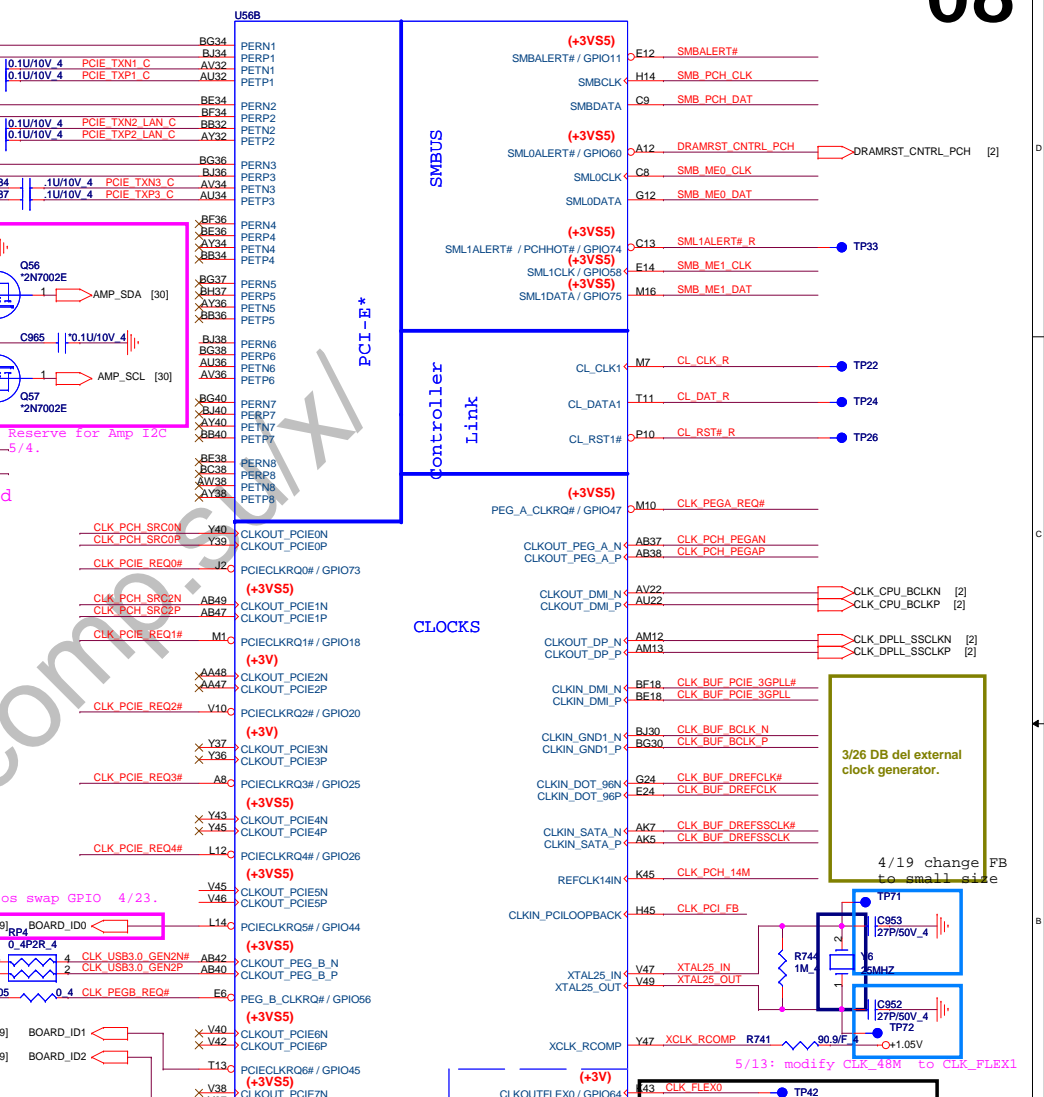
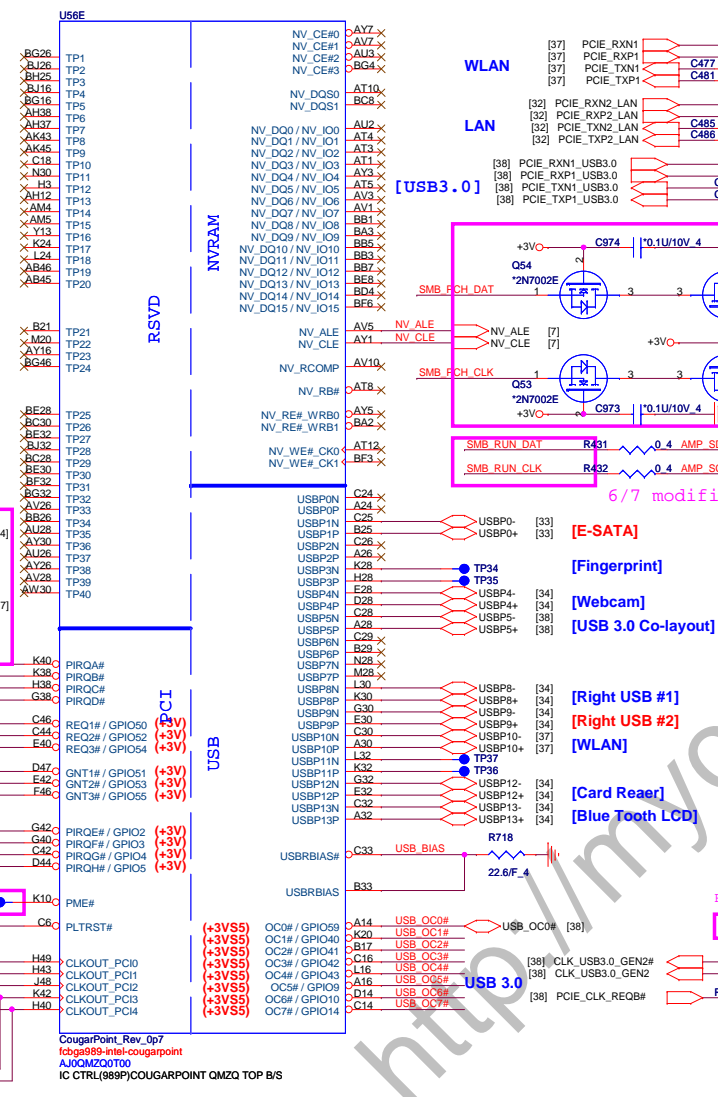
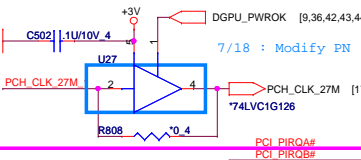
Size	Document Number	Rev
Custom	PCH 2/6 (SATA/HDA/SPI)	1A

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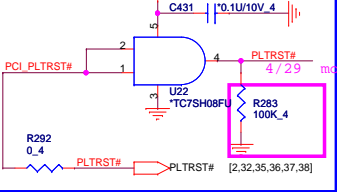
PCI/USBOC# Pull-up(CLG)



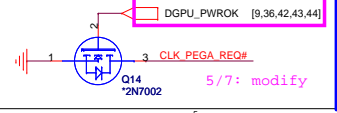
MPC Switch Control: MPC_PWR_CTRL# Low = MPC ON, High = MPC OFF (Default). Includes a schematic for the MPC_PWR_CTRL# pin connected to R769.



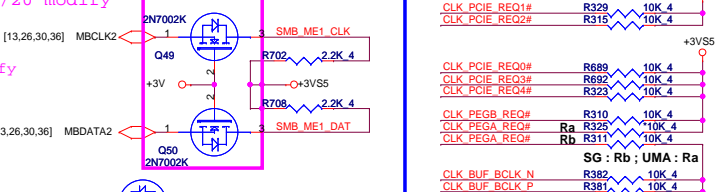
PLTRST#(CLG)



PEG Clock detect (SG only)



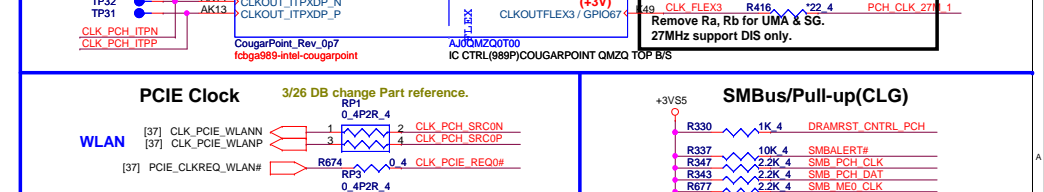
SMBus/Pull-up(CLG)



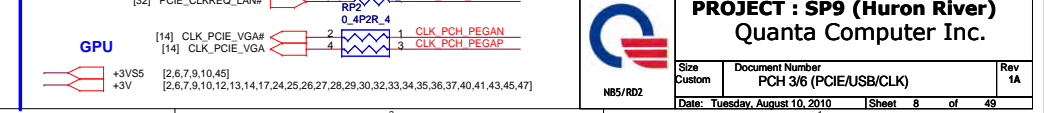
CLK_REQ/Strap Pin(CLG)



PCIE Clock



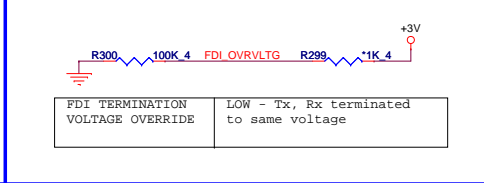
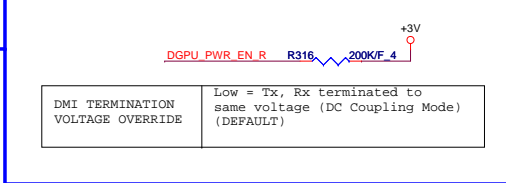
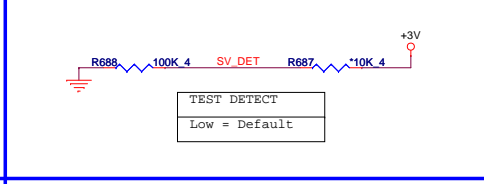
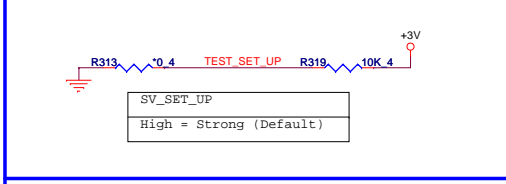
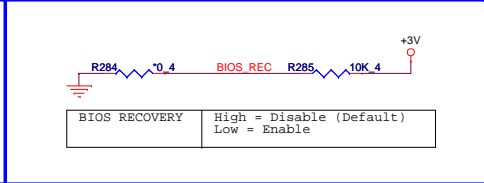
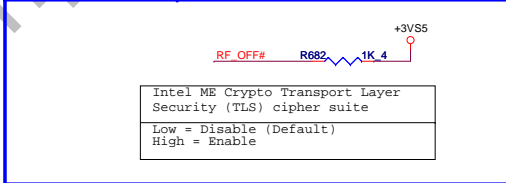
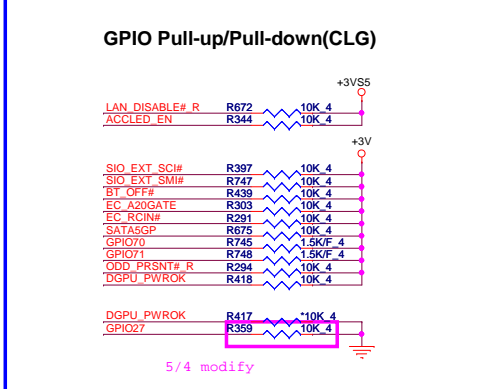
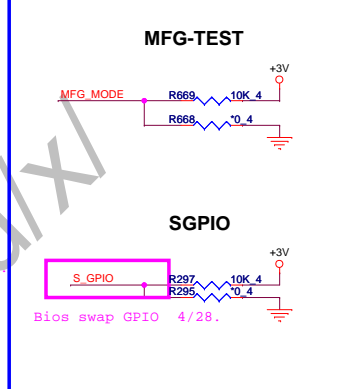
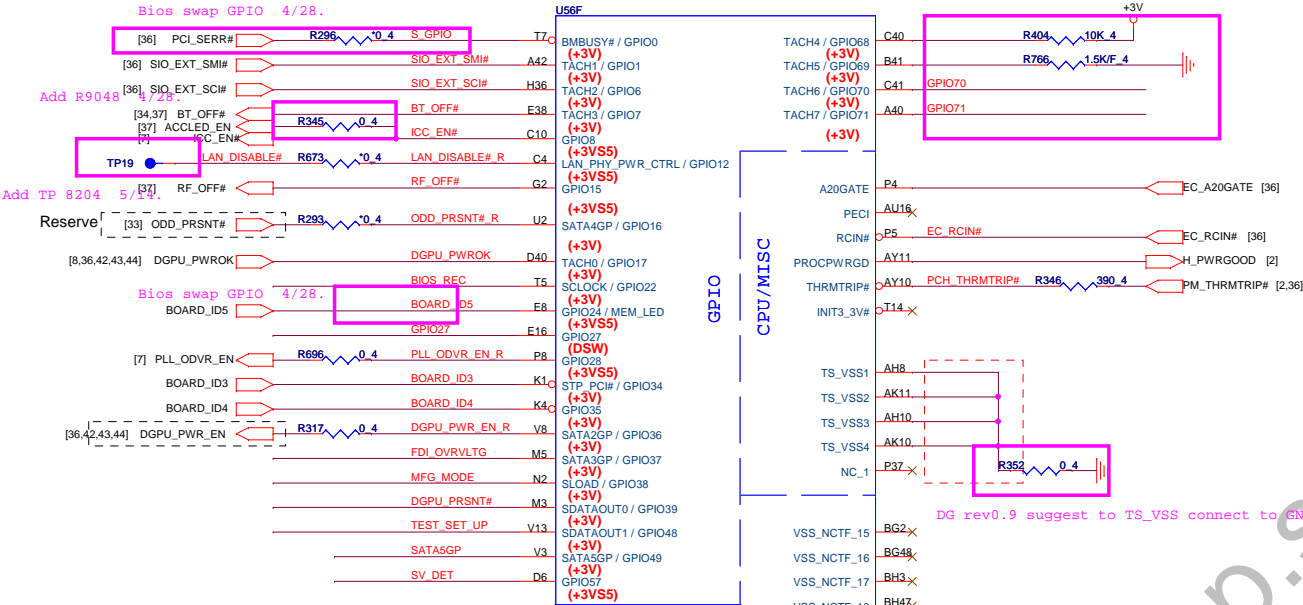
SMBus/Pull-up(CLG)



PROJECT : SP9 (Huron River) Quanta Computer Inc. Includes a table with columns: Size Custom, Document Number PCH 3/6 (PCIe/USB/CLK), Rev 1A, Date: Tuesday, August 10, 2010, Sheet 8 of 49.

Cougar Point (GPIO,VSS_NCTF,RSVD)

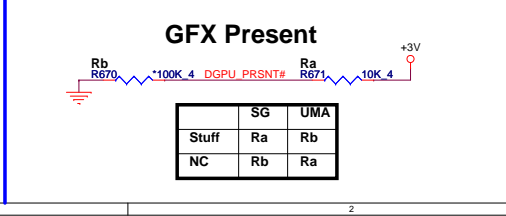
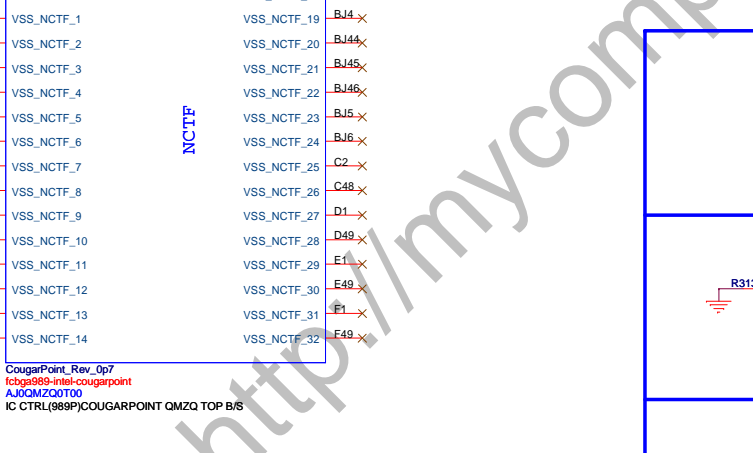
Clock Gen Power OK (CLG)



Legend:

- +3V55 [2,6,7,8,10,45]
- +3V [2,6,7,8,10,12,13,14,17,24,25,26,27,28,29,30,32,33,34,35,36,37,40,41,43,45,47]

Model	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
SP9 2D	0	0	0	0	0	0
SP9 3D	0	0	0	0	0	1



PROJECT : SP9 (Huron River)
Quanta Computer Inc.

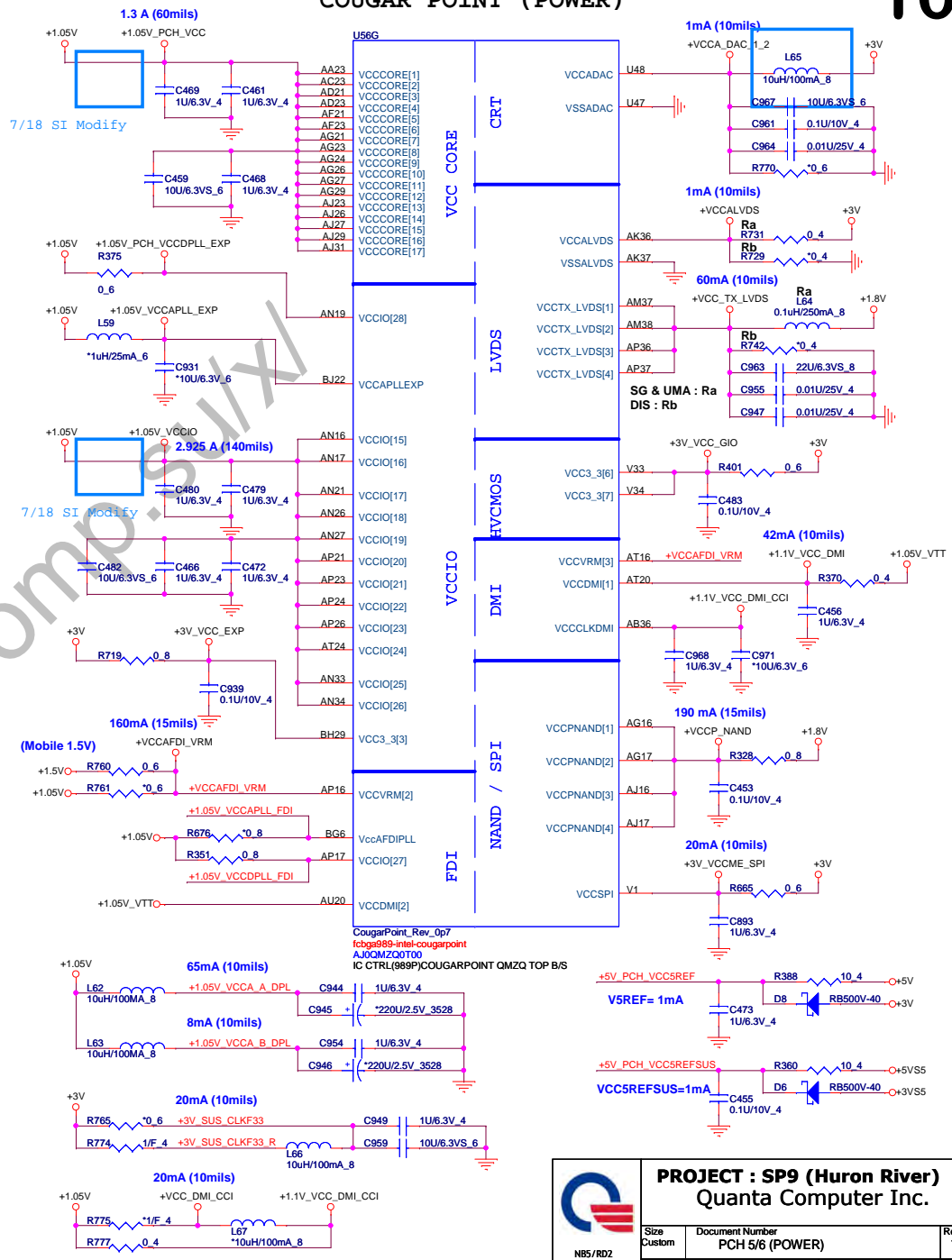
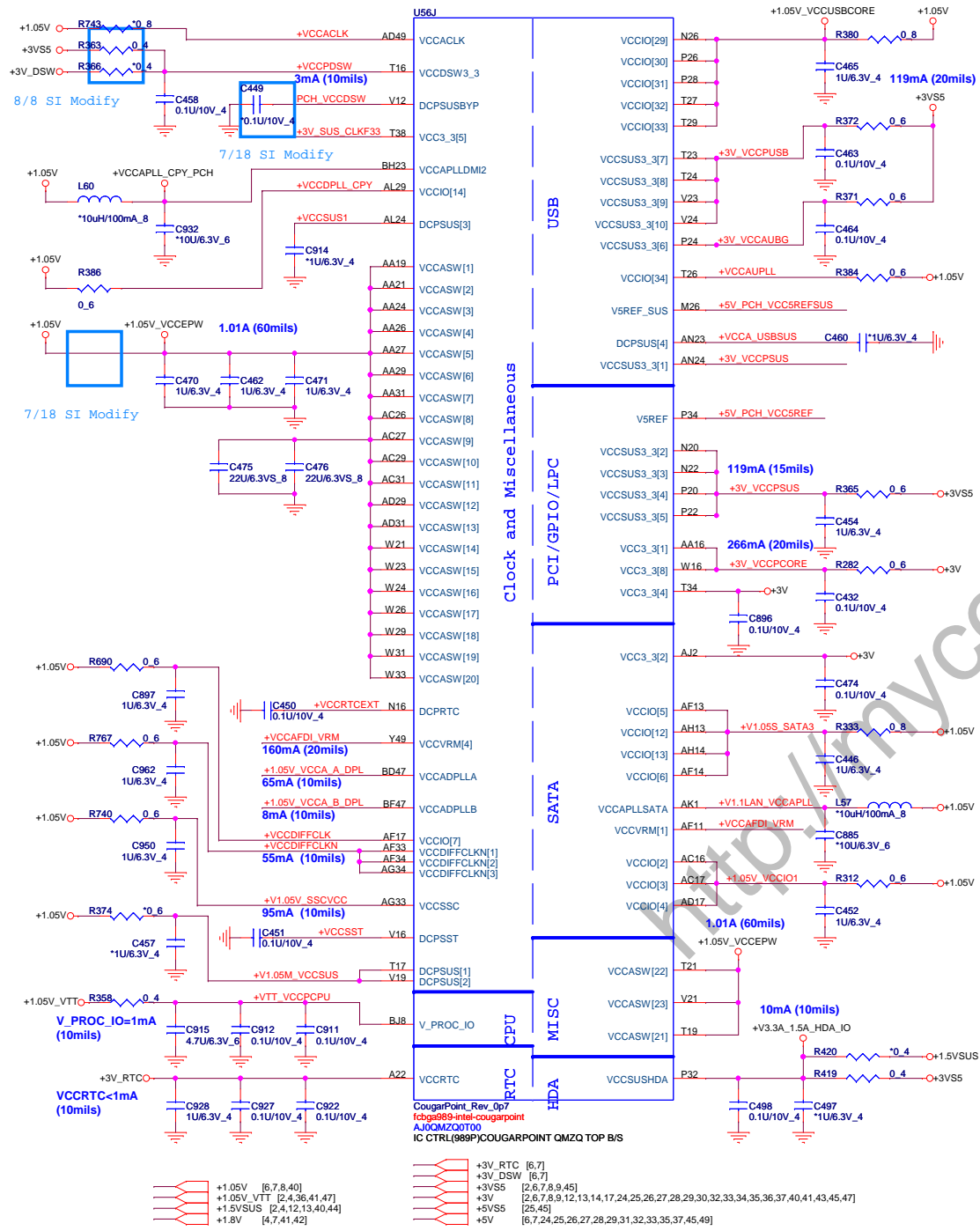
Size Custom Document Number PCH 4/6 (GPIO/MISC) Rev 1A

Date: Tuesday, August 10, 2010 Sheet 9 of 49

Cougar Point-M (POWER)

COUGAR POINT (POWER)

7/29 SI Modify for CRT noise



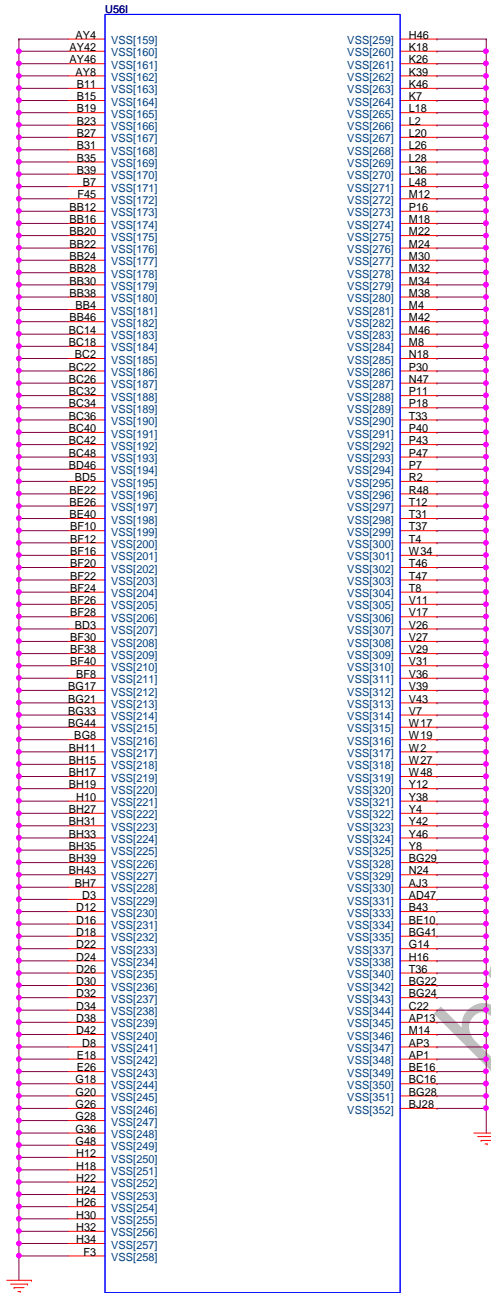
+1.05V [6,7,8,40]	+3V_RTC [6,7]
+1.05V_VTT [2,4,36,41,47]	+3V_DSW [6,7]
+1.5VSUS [2,4,12,13,40,44]	+3VSS [2,6,7,8,9,45]
+1.8V [4,7,41,42]	+3V [2,6,7,8,9,12,13,14,17,24,25,26,27,28,29,30,32,33,34,35,36,37,40,41,43,45,47]
	+5VS5 [25,45]
	+5V [6,7,24,25,26,27,28,29,31,32,33,35,37,45,49]

PROJECT : SP9 (Huron River)
Quanta Computer Inc.

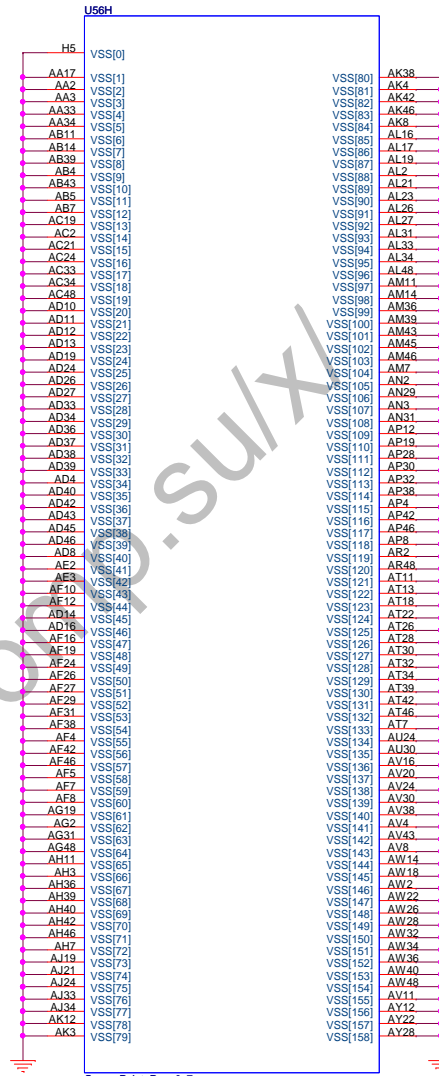
Size	Document Number	Rev
Custom	PCH 5/6 (POWER)	1A
Date: Tuesday, August 10, 2010 Sheet 10 of 49		

IBEX PEAK-M (GND)


IBEX PEAK-M (GND)

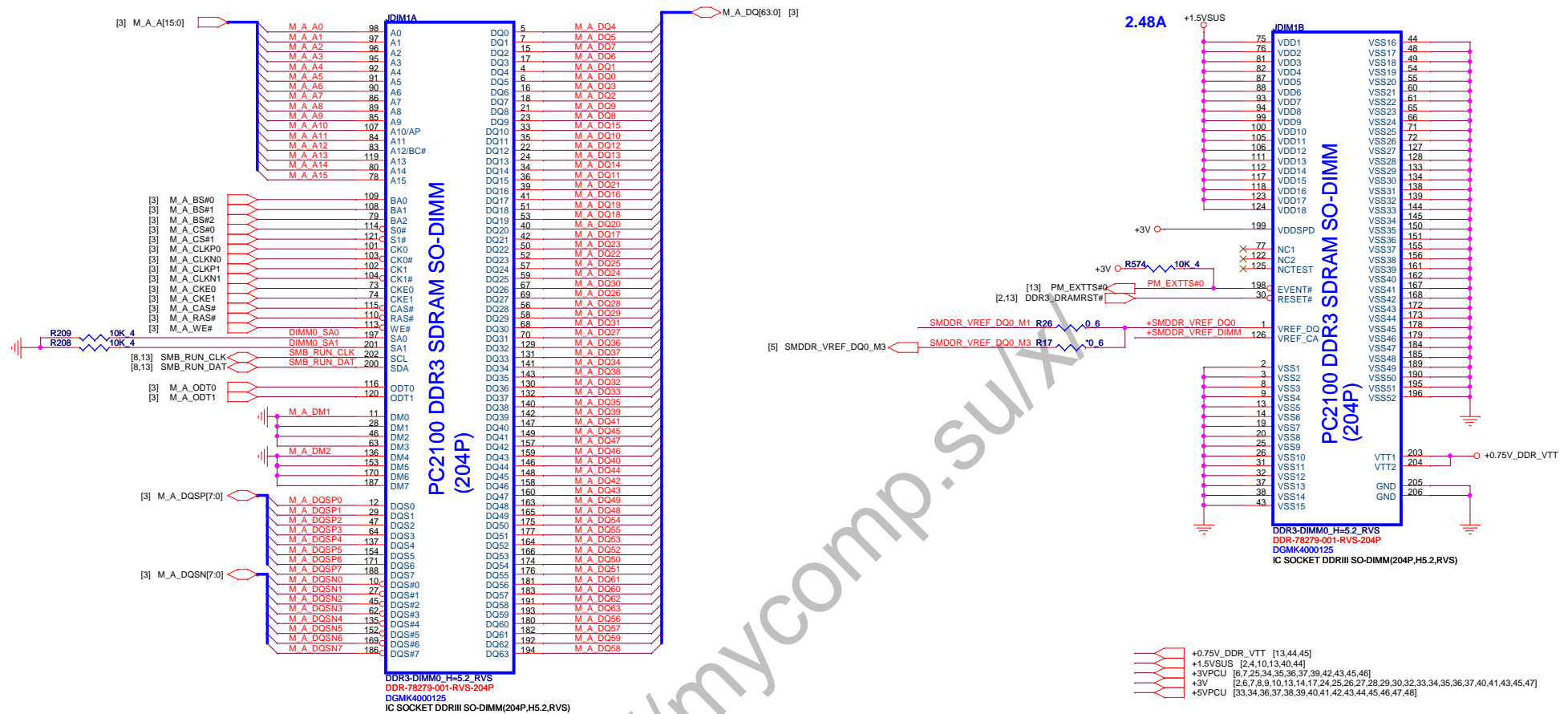


CougarPoint_Rev_0p7



CougarPoint_Rev_0p7

 NBS/RD2	PROJECT : SP9 (Huron River)		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number PCH 6/6 (GND)	
Date: Tuesday, August 10, 2010		Sheet 11 of 49	



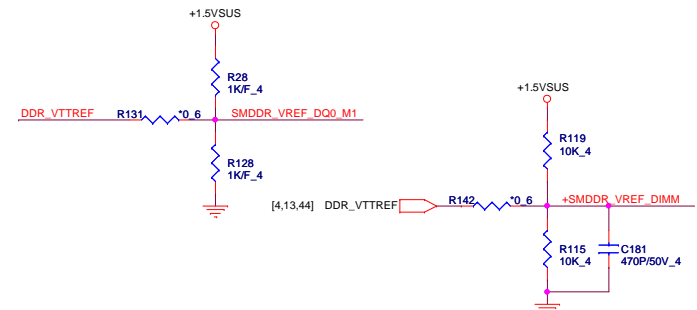
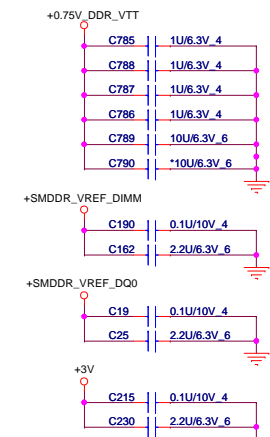
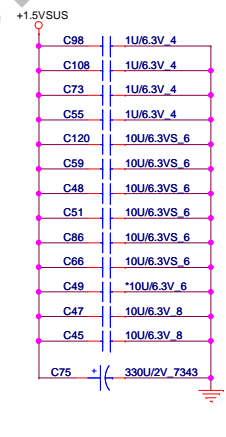
- +0.75V_DDR_VTT [13,44,45]
- +1.5VSUS [2,4,10,13,40,44]
- +3VPCU [6,7,25,34,35,36,37,39,42,43,45,46]
- +3V [2,6,7,8,9,10,13,14,17,24,25,26,27,28,29,30,32,33,34,35,36,37,40,41,43,45,47]
- +5VPCU [33,34,36,37,38,39,40,41,42,43,44,45,46,47,48]

VREF DQ0 M2 Solution

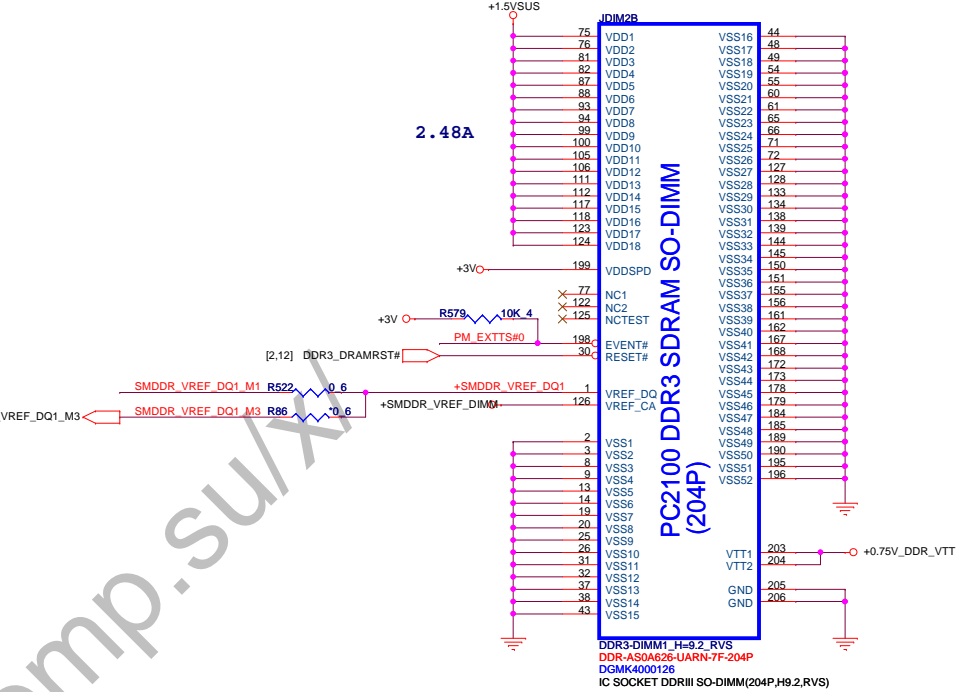
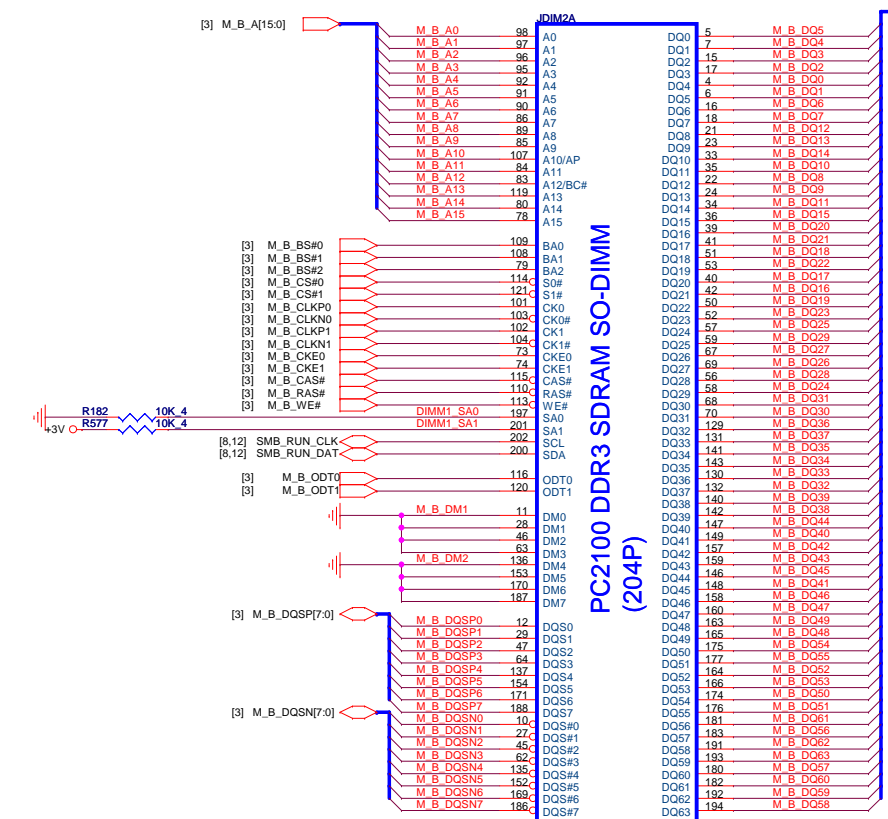
Place these Caps near So-Dimm0.

VREF DQ0 M1 Solution

7/18 : Del M2 solution

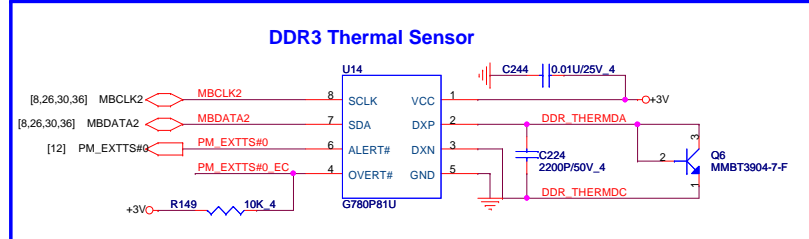


	PROJECT : SP9 (Huron River)		Rev 1A
	Quanta Computer Inc.		
Size Custom	Document Number DDR3 DIMM0-RVS (5.2H)		
Date: Tuesday, August 10, 2010	Sheet 12	of 49	



- +0.75V_DDR_VTT [12,44,45]
- +1.5VSUS [2,4,10,12,40,44]
- +3VPCU [8,7,25,34,35,36,37,39,42,43,45,46]
- +3V [2,6,7,8,9,10,12,14,17,24,25,26,27,28,29,30,32,33,34,35,36,37,40,41,43,45,47]
- +5VPCU [33,34,36,37,38,39,40,41,42,43,44,45,46,47,48]

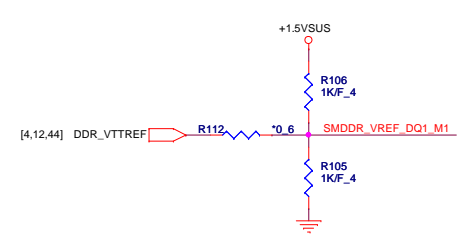
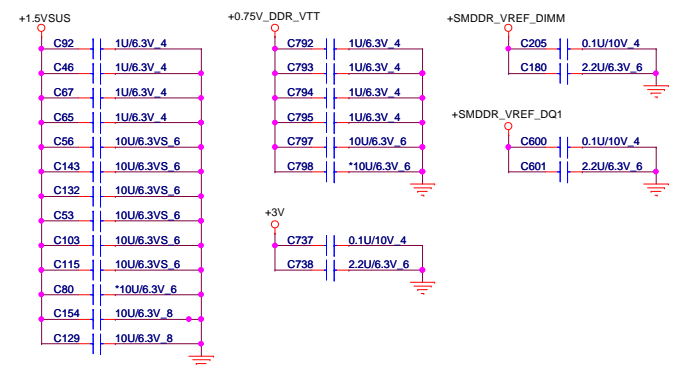
DDR3-DIMM1_H=9.2_RV5
 DDR-AS0A626-UARN-7F-204P
 DGMK4000126
 IC SOCKET DDRIII SO-DIMM(204P,H9.2,RV5)



VREF DQ1 M2 Solution

Place these Caps near So-Dimm1.

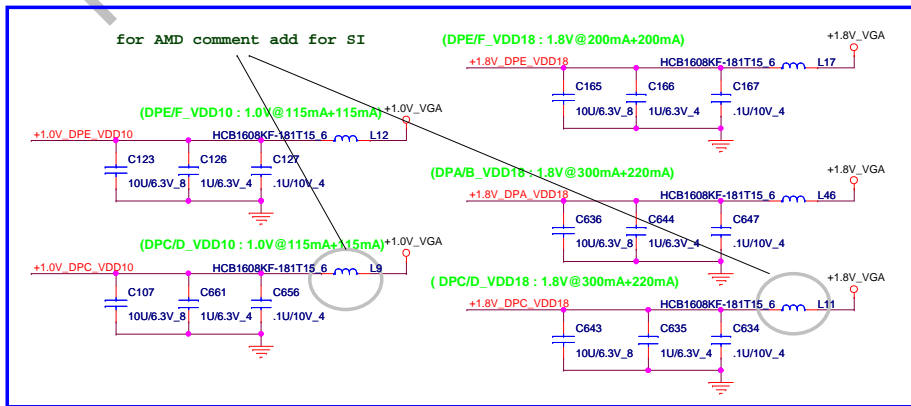
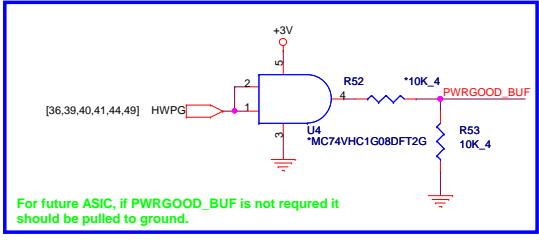
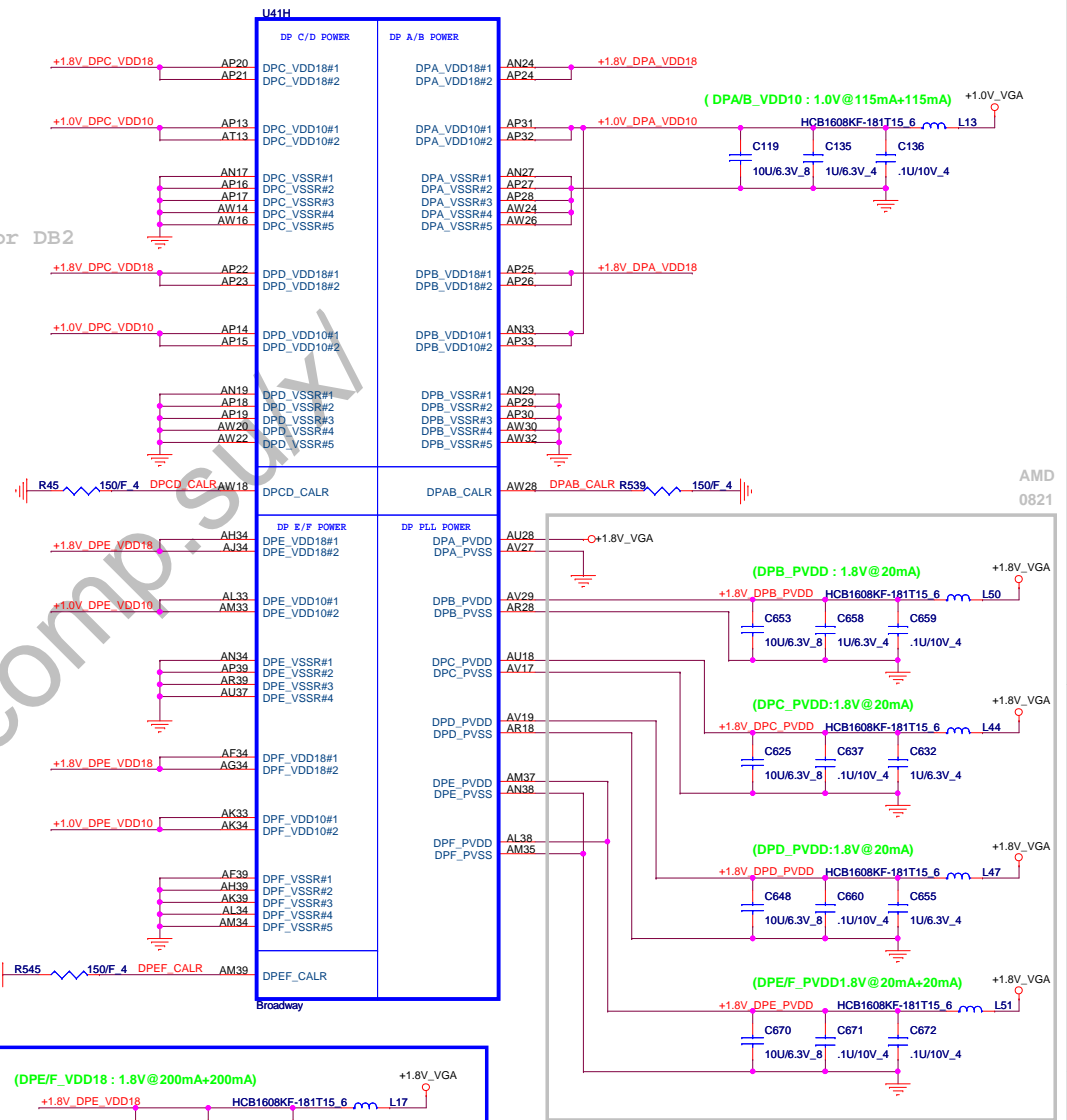
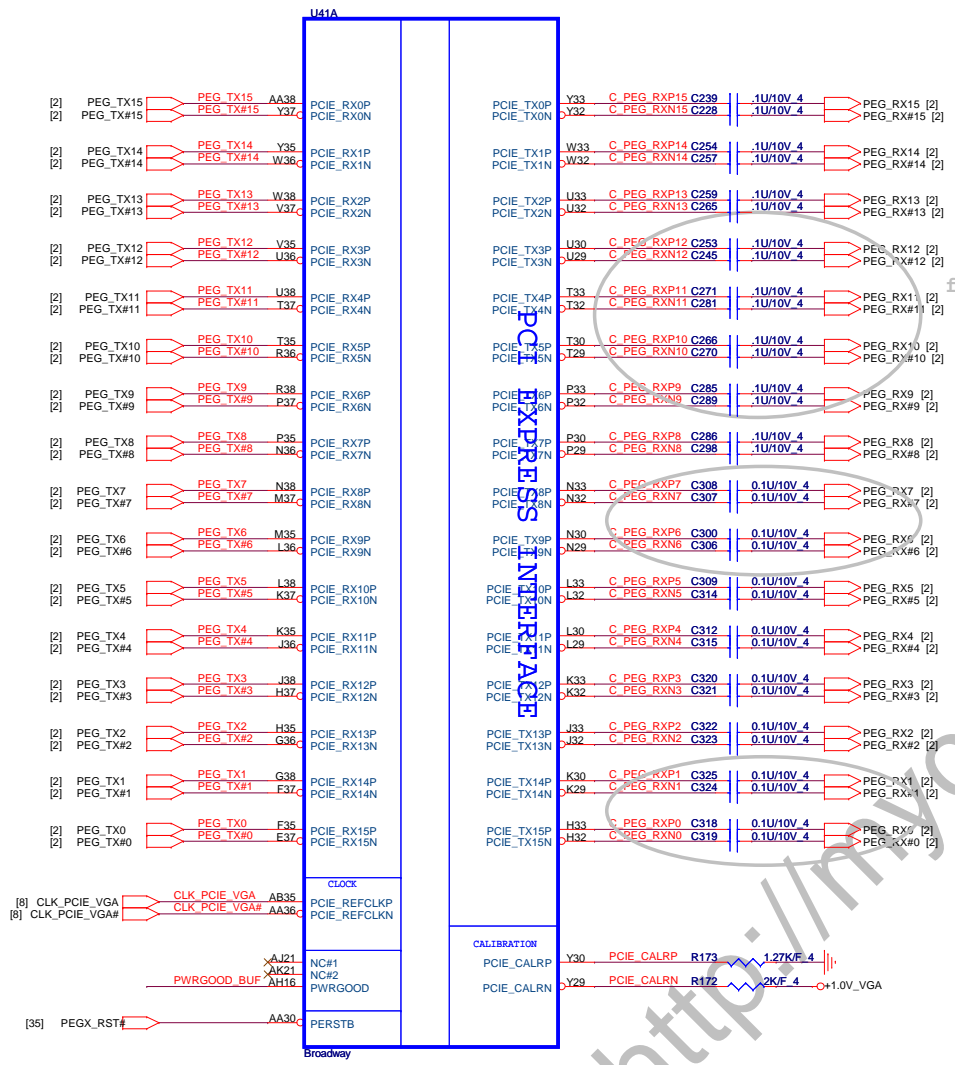
VREF DQ1 M1 Solution

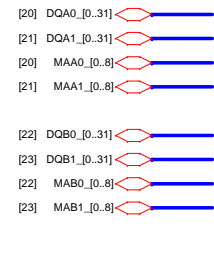


7/18 : Del M2 solution

PROJECT : SP9 (Huron River)
Quanta Computer Inc.

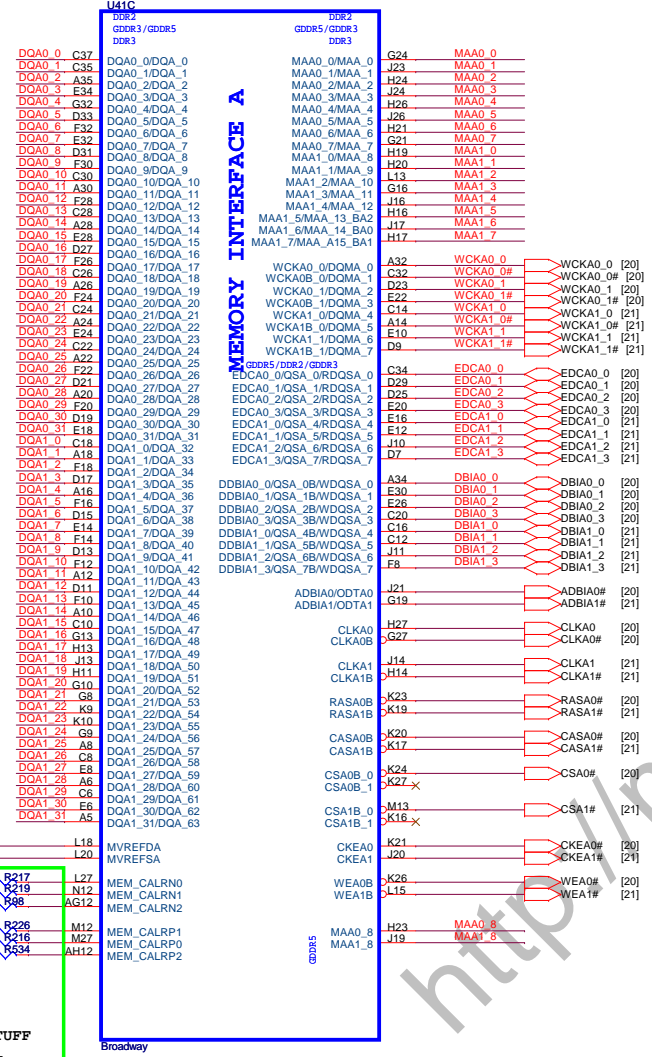
Size Custom	Document Number	Rev 1A
	DDR3 DIMM1-RV5 (9.2H)	
Date: Tuesday, August 10, 2010	Sheet 13 of 49	



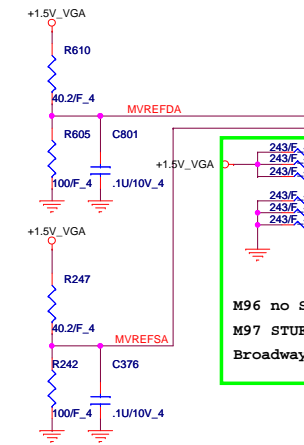
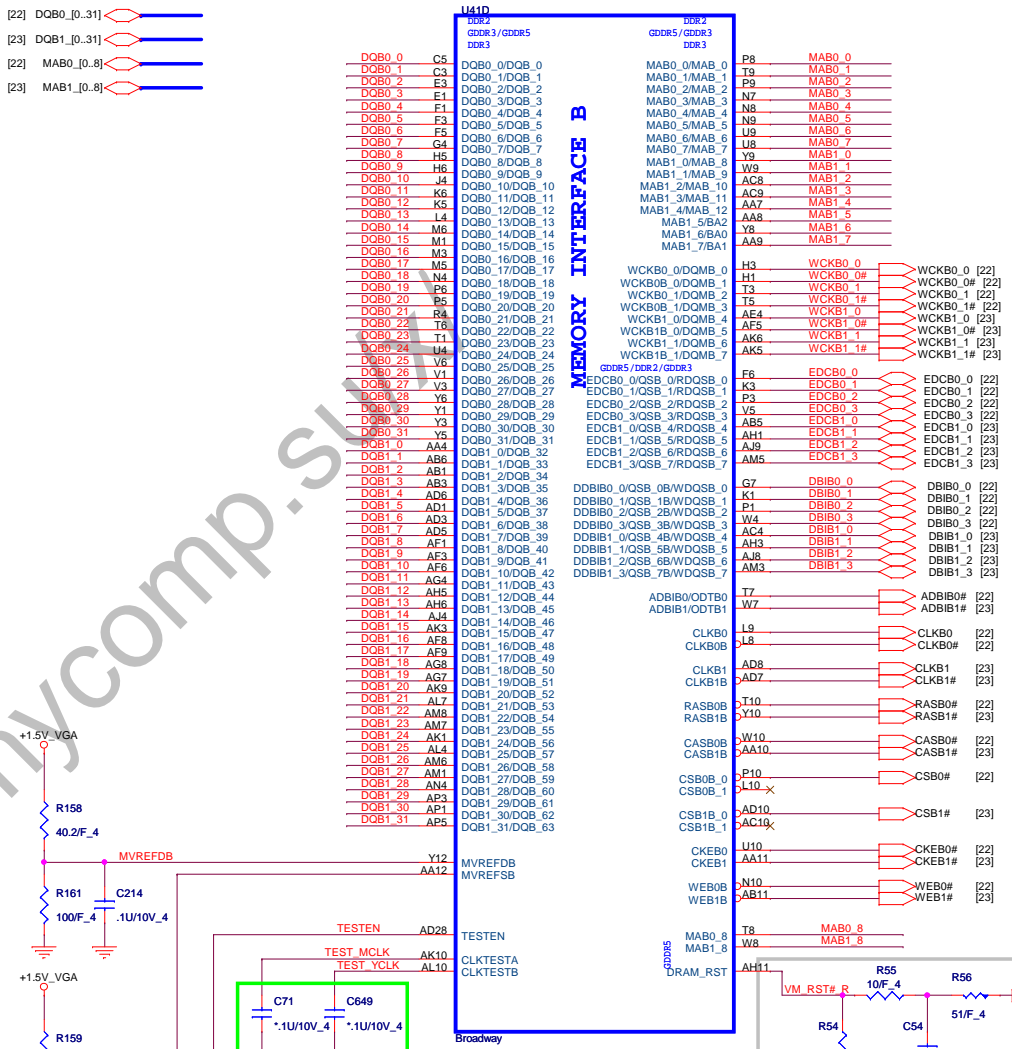


[18,20,21,22,23,42] +1.5V_VGA

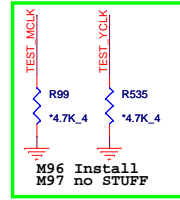
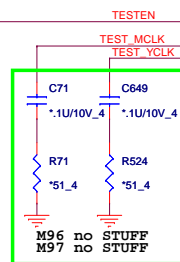
MEMORY INTERFACE A



MEMORY INTERFACE B



M96 no STUFF
M97 STUFF
Broadway STUFF

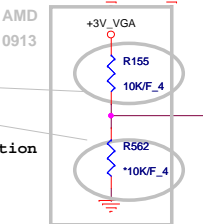


Location	B-W	Value
R32	10R	
R34	5K	
R33	51R	
C29	120PF	

DB 20100428 (ref 137-12)

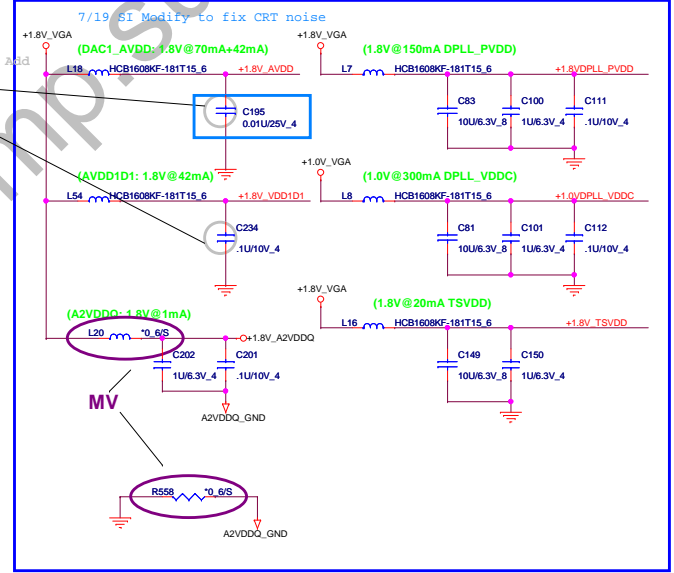
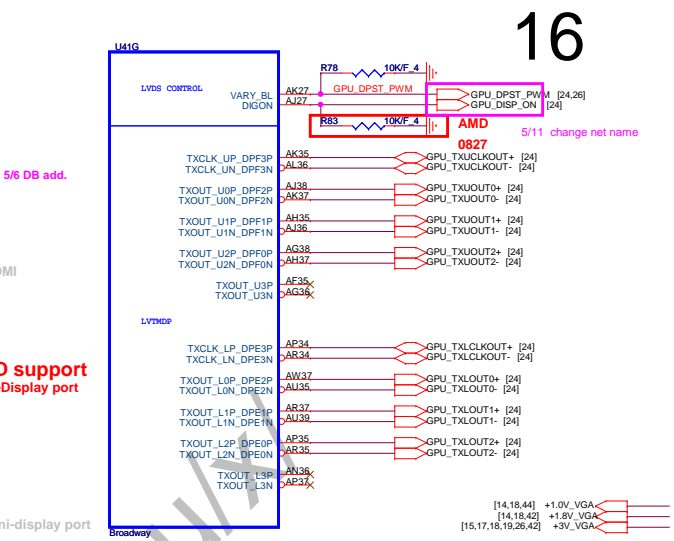
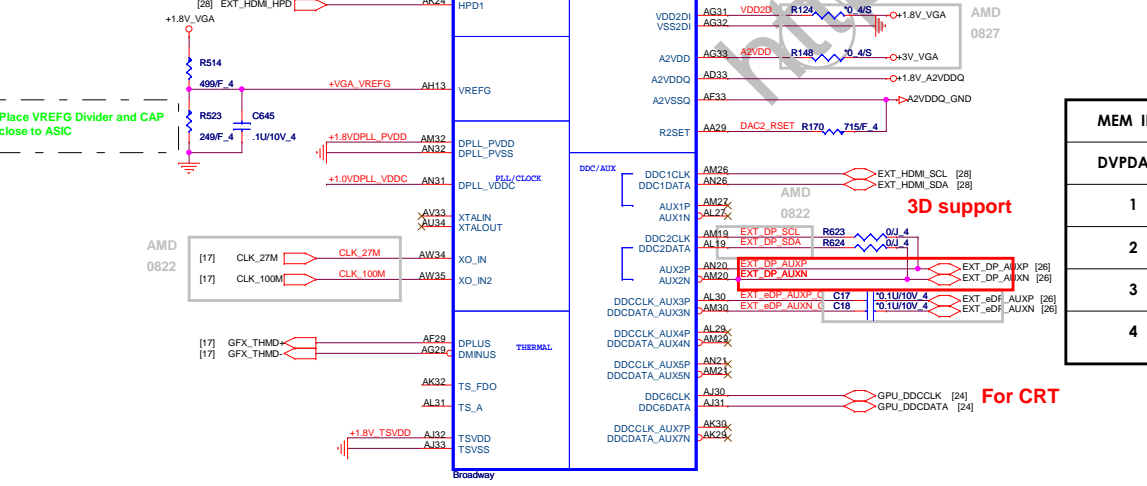
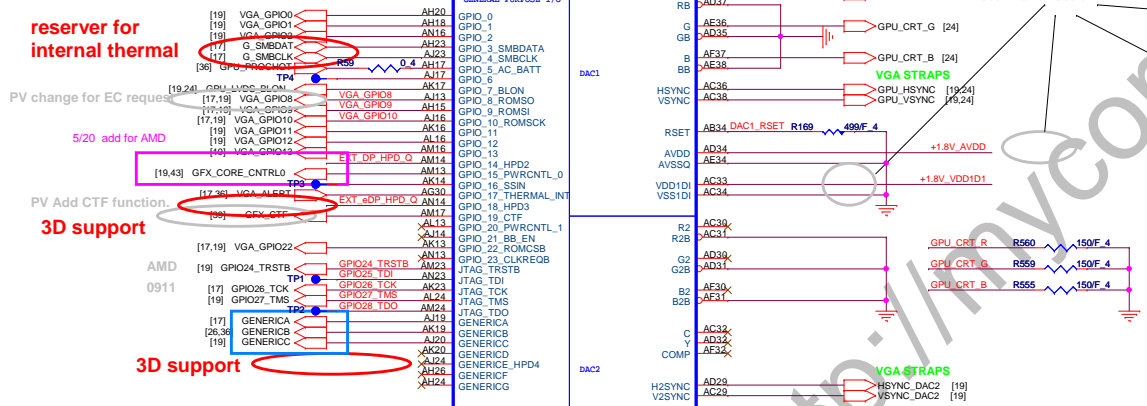
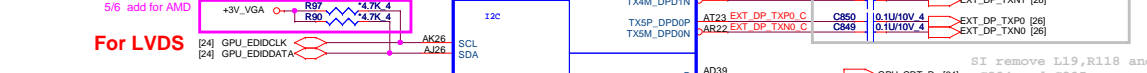
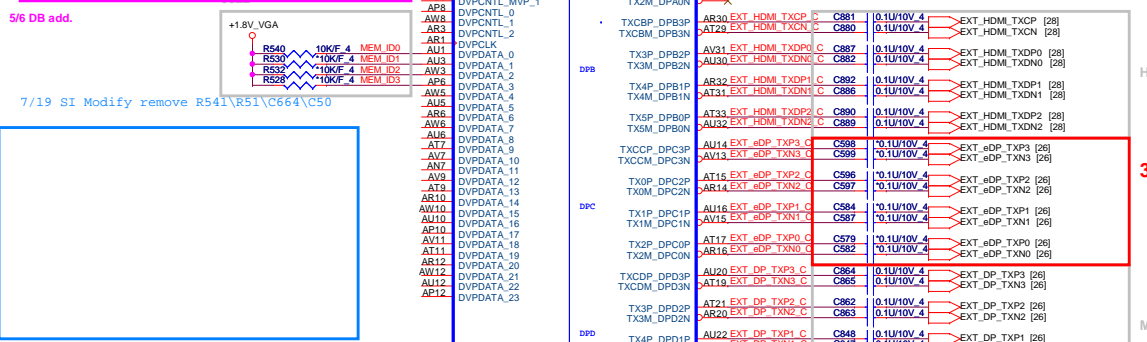
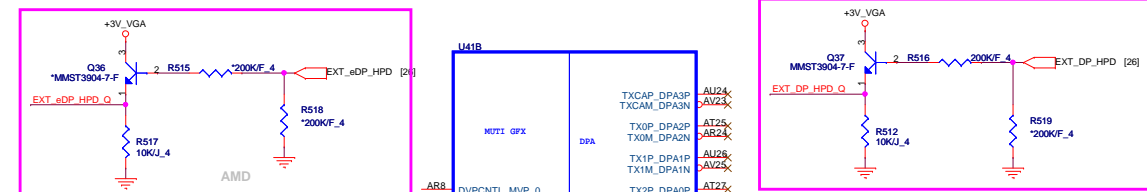
PV stuff R111
non-stuff R373

JTAG enable function



PROJECT : SP9 (Huron River)
Quanta Computer Inc.

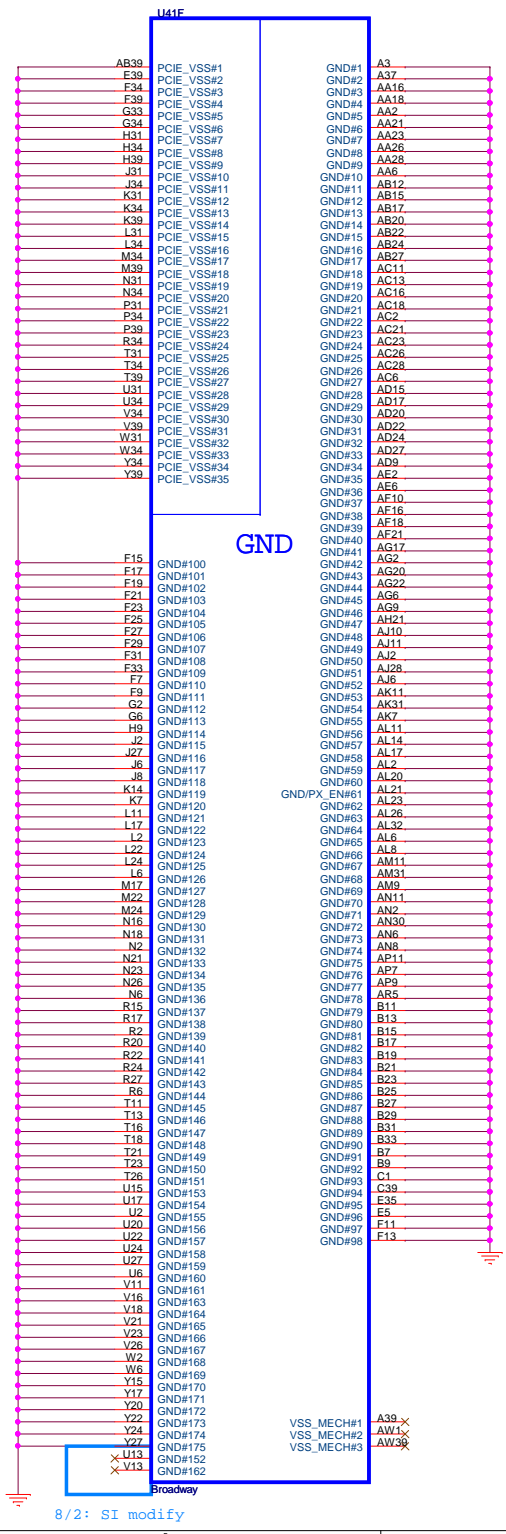
Size Custom	Document Number ATI M97-M2 (MEM I/F) 2/5	Rev 1A
Date: Tuesday, August 10, 2010	Sheet 15 of 49	



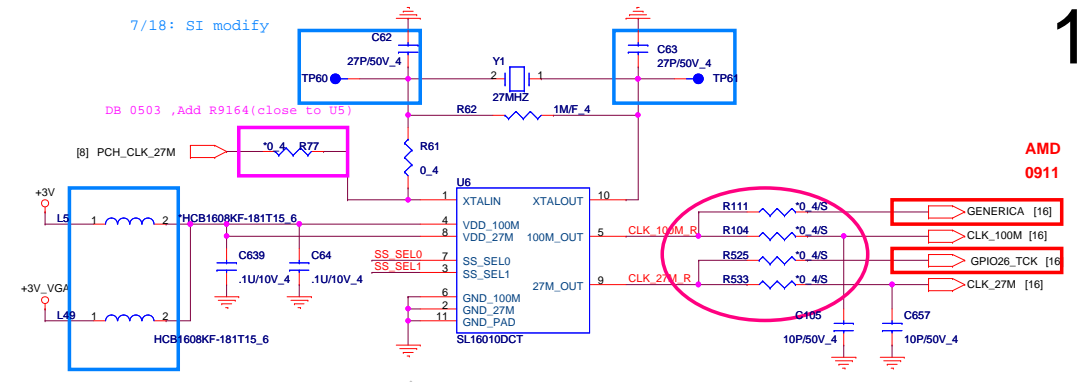
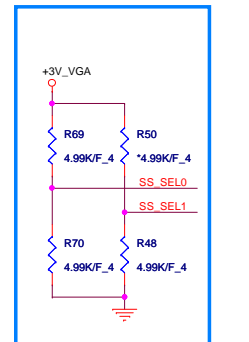
MEM ID	3	2	1	0	Verona		
DVPDATA	3	2	1	0	GDDR5 Type	Configuration	Size
1	0	0	0	1	Samsung K4G10325FE-HC05 (4.0Gbps)	32*32 or 64*16 x 8 pcs	1G
2	0	0	1	0	Hynix H5GQ1H24AFR-TOC BGA (4.0Gbps)	32*32 or 64*16 x 8 pcs	1G
3	0	0	1	1	Hynix H5GQ2H24MFR-TOC BGA (4.0Gbps)	64*32 or 128*16 x 8 pcs	2G
4	0	1	0	0	Samsung K4G20325FC-HC05 (4.0Gbps)	64*32 or 128*16 x 8 pcs	2G

PROJECT : SP9 (Huron River)
Quanta Computer Inc.

Size Custom Document Number **ATI M97-M2 (DISPLAY) 3/5** Rev 1A
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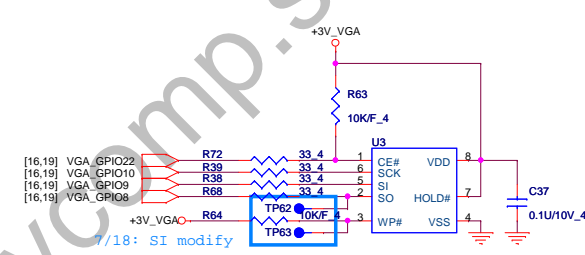


27MHz + 100MHz OSC Option

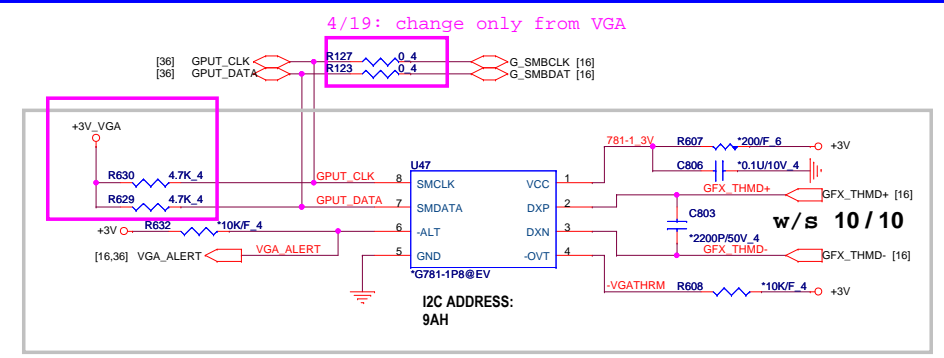


AMD
0911

Ext EEPROM



Thermal Sensor

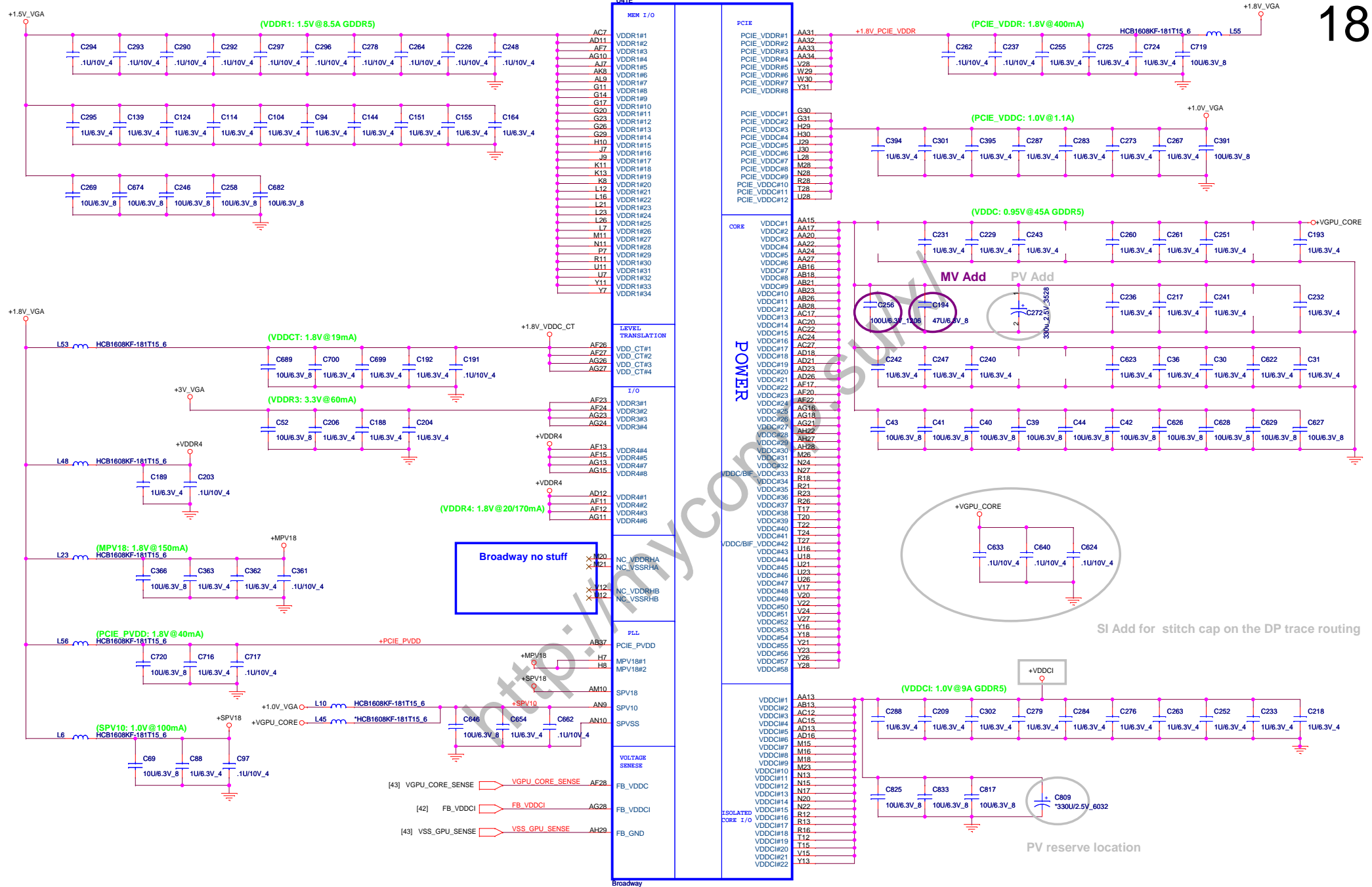


8/2: SI modify

[2,6,7,8,9,10,12,13,14,24,25,26,27,28,29,30,32,33,34,35,36,37,40,41,43,45,47] +3V
[15,16,18,19,26,42] +3V_VGA

PROJECT : SP9 (Huron River)
Quanta Computer Inc.

Size Custom	Document Number ATI M97(GND&Str&Ther)4/5	Rev 1A
Date: Tuesday, August 10, 2010		Sheet 17 of 49



- [14,16,44] +1.0V_VGA
- [43] +VGPU_CORE
- [15,20,21,22,23,42] +1.5V_VGA
- [14,16,42] +1.8V_VGA
- [15,16,17,19,26,42] +3V_VGA

PROJECT : SP9 (Huron River)
Quanta Computer Inc.

Size Custom	Document Number ATI M97-M2 (POWER) 5/5	Rev 1A
Date: Tuesday, August 10, 2010		
Sheet	18	of 49

Straps

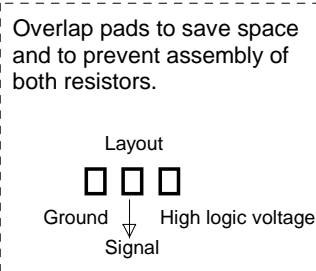
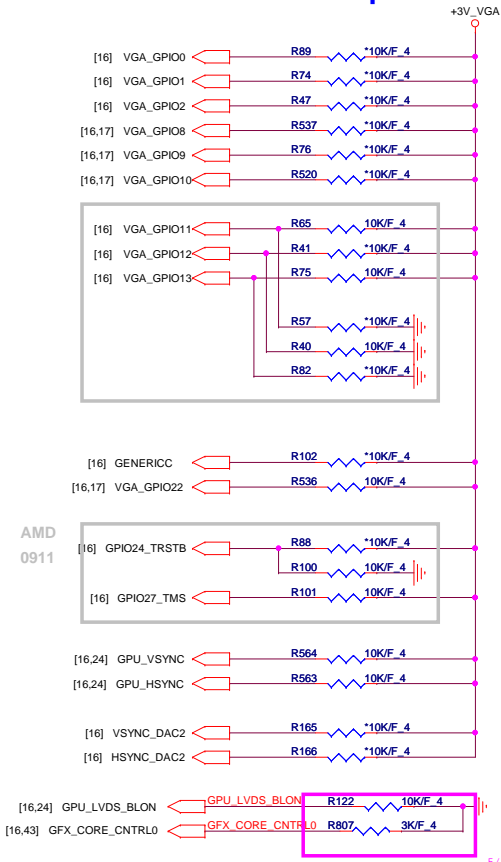


Table 3-34 ROM Configurations

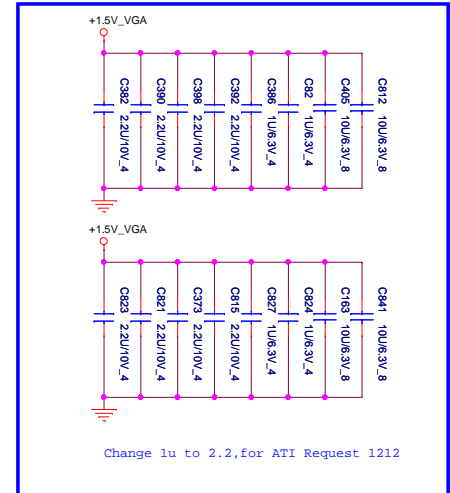
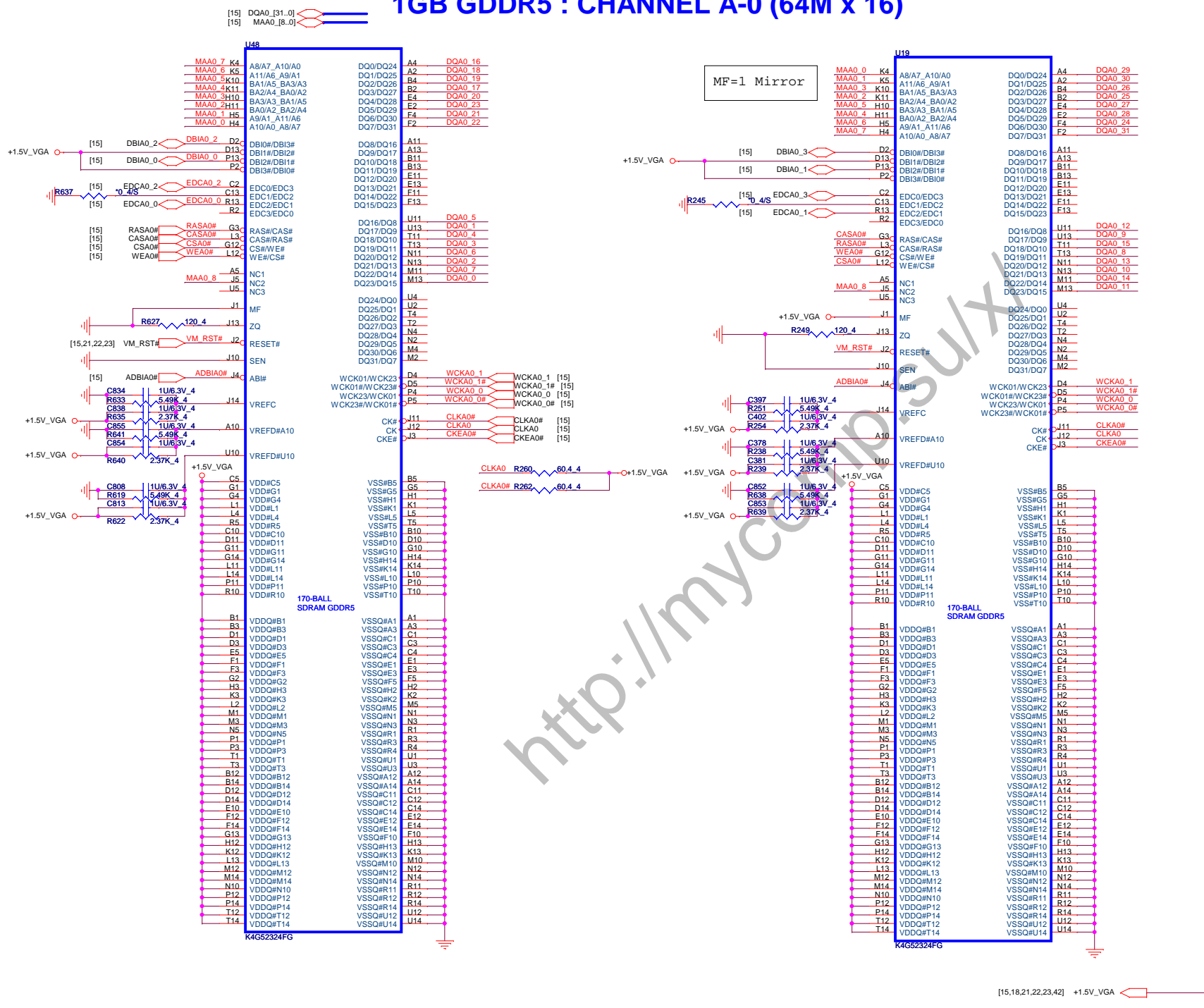
Manufacturer	Part Number	Size	CONFIG[2:0]
Atmel	AT25F512	512 kbit	001
	AT25F512A	512 kbit	010
	AT25F1024	1 Mbit	011
	AT25F1024A	1 Mbit	011
	AT25F2048	2 Mbit	011
	AT25F4096	4 Mbit	011
ST Microelectronics	M25P05A	512 kbit	100
	M25P10A	1 Mbit	101
	M25P20	2 Mbit	101
	M25P40	4 Mbit	101
	M25P80	8 Mbit	101
Silicon Storage Technology	SST25VF512	512 kbit	010
	SST25VF010	1 Mbit	011
	SST25VF020	2 Mbit	011
	SST25VF040	4 Mbit	011
Winbond Electronics Corporation	W45B512	512 kbit	110
	W45B012	1 Mbit	111
YMC	Y25LF05	512 kbit	010
	SA25C020	2 Mbit	011
PMC	Pm25LV512	512 kbit	100
	Pm25LV010	1 Mbit	101

Default

Strap Name	Pin Straps	Description	Default Value
TX_PWRS_ENB	GPIO0	GPIO[1:0]:Recommend to pulling up for PICE setting. GPIO_0:PCIE full TX output swing	
TX_DEEMPH_EN	GPIO1	GPIO_1:PCIE Transmitter DE-EMPHASIS enabled	
BIF_GEN2_EN	GPIO2	GPIO_2:System is using PCIE GEN1 can be let it NC(ASIC internal pull down) if Gen2 just pull up for PCIE 5GT/s support. (0=PCIE GNE1,2.5GT/s ; 1=PCIE GNE2,5GT/s)	
STRAP_BIF_CLK_PM_EN	GPIO8		
CONFIG[3]	GPIO9		
CONFIG[2]	GPIO13		
CONFIG[1]	GPIO12		
CONFIG[0]	GPIO11		
BIOS_ROM_EN	GPIO22	BIOS_ROM_EN(GPIO22)=1, then Config[2:0]=GPIO[13:12:11] defines the ROM type. (See table as below)	
AUDIO[0]	VSYNC		
AUD(1)	HSYNC		
VSYNC_DAC2	V2SYNC		
HSYNC_DAC2	H2SYNC		
	GENERICC		

	PROJECT : SP9 (Huron River) Quanta Computer Inc.		
	Size Custom NBS/RD2	Document Number VGA Core/+1.8VGFx/1.0VGFx	Rev 1A
Date: Tuesday, August 10, 2010 Sheet 19 of 49			

1GB GDDR5 : CHANNEL A-0 (64M x 16)



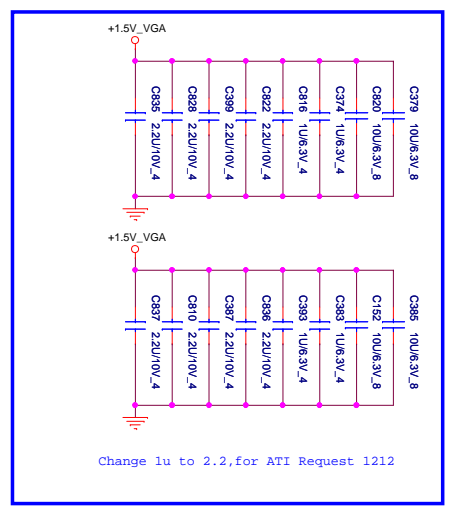
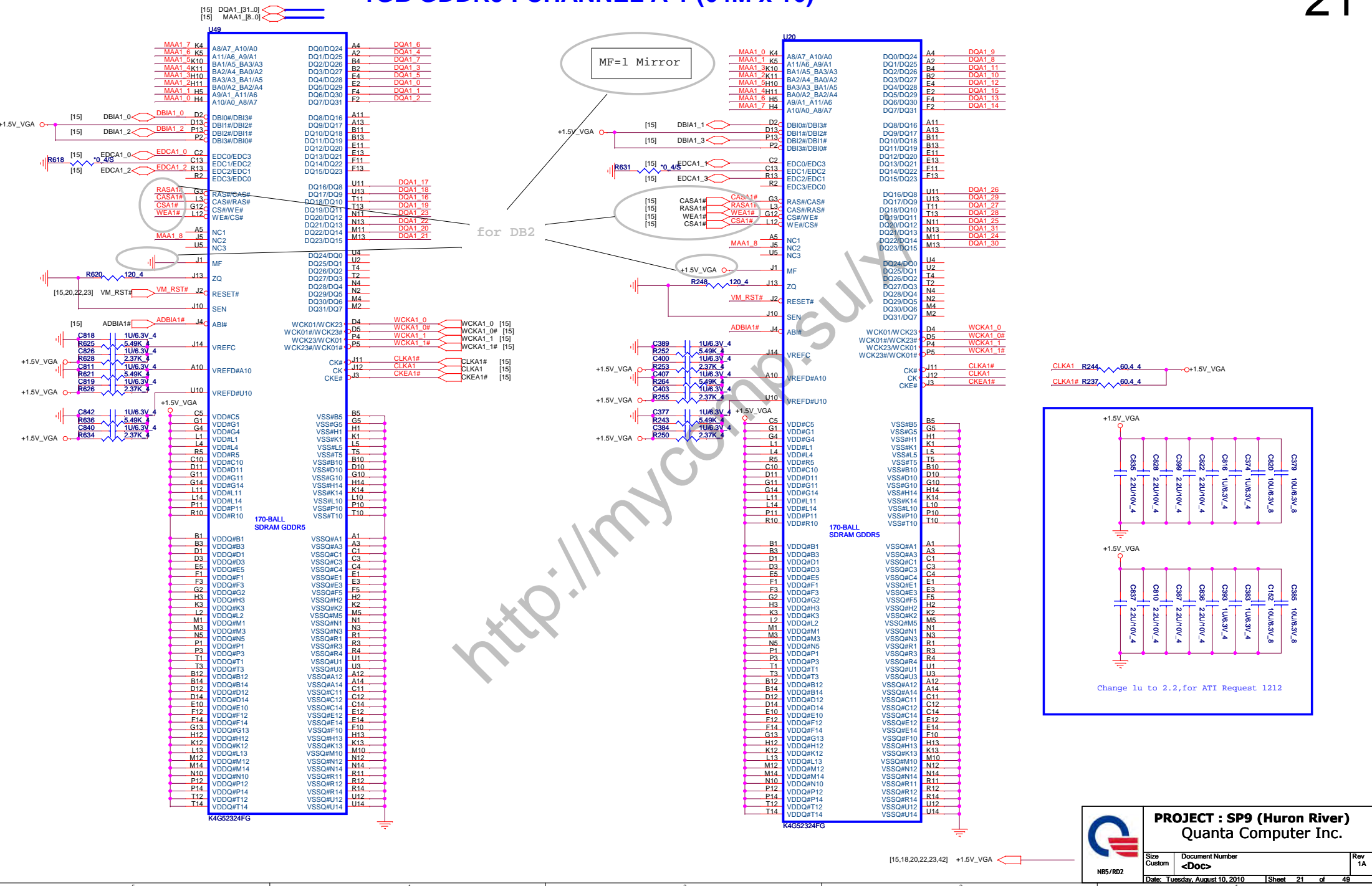
PROJECT : SP9 (Huron River)
Quanta Computer Inc.

Size Custom	Document Number <Doc>	Rev 1A
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NBS/RD2

[15,18,21,22,23,42] +1.5V_VGA

1GB GDDR5 : CHANNEL A-1 (64M x 16)

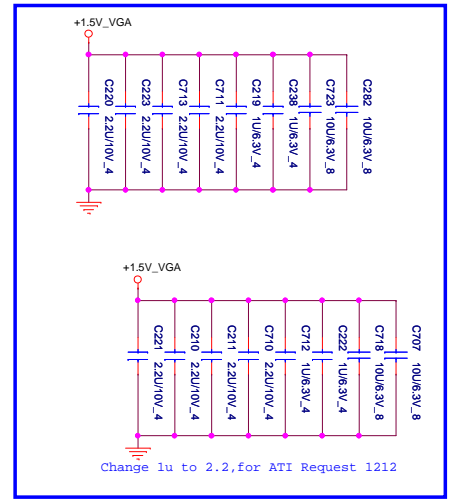
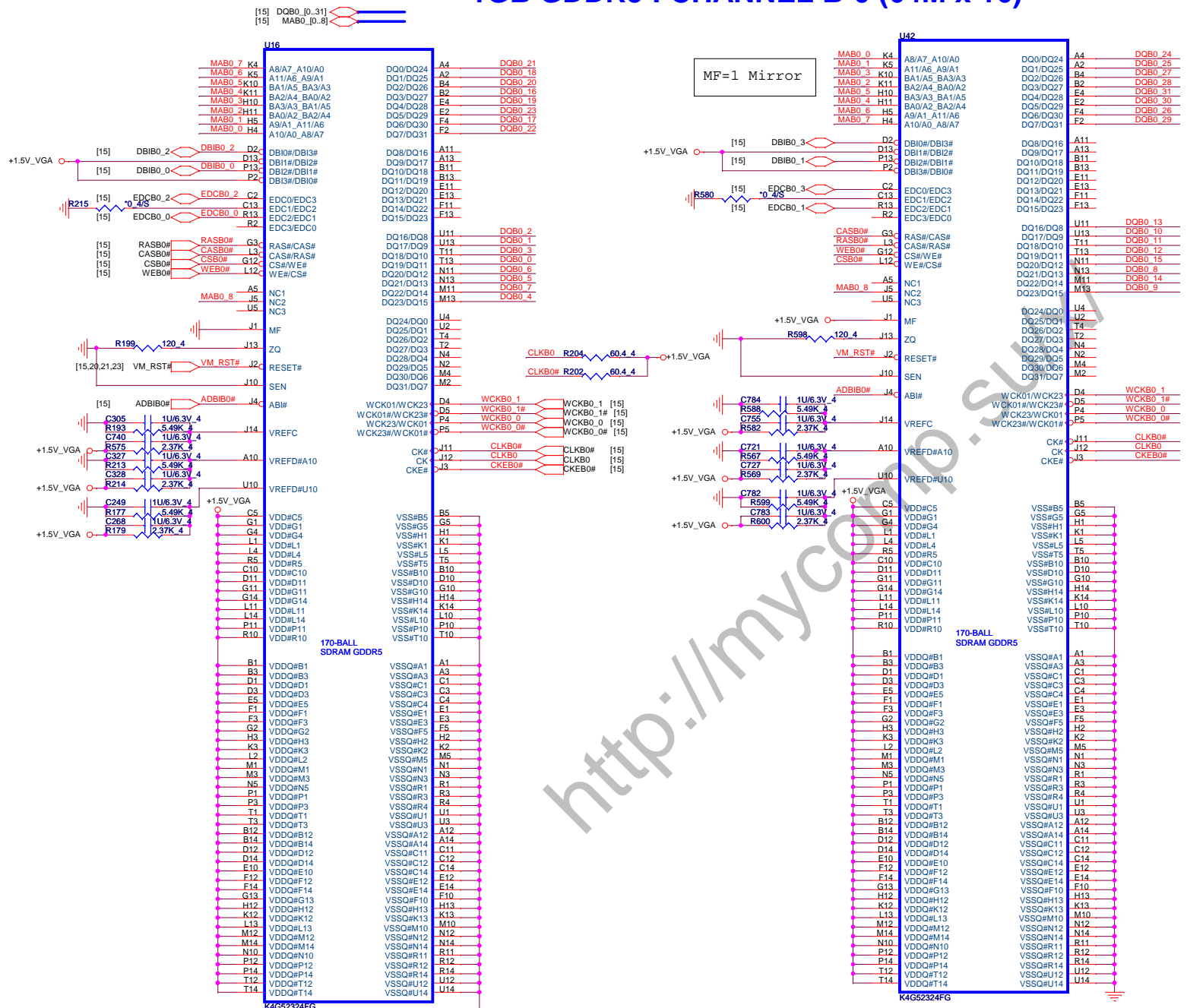


PROJECT : SP9 (Huron River)
Quanta Computer Inc.

Size Custom	Document Number <Doc>	Rev 1A
Date: Tuesday, August 10, 2010		Sheet 21 of 49

<http://mycomp.com/su/>

1GB GDDR5 : CHANNEL B-0 (64M x 16)

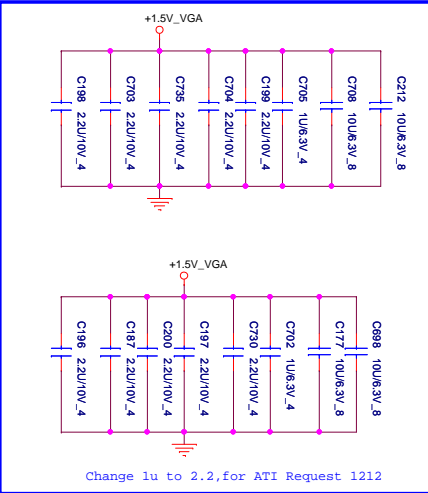
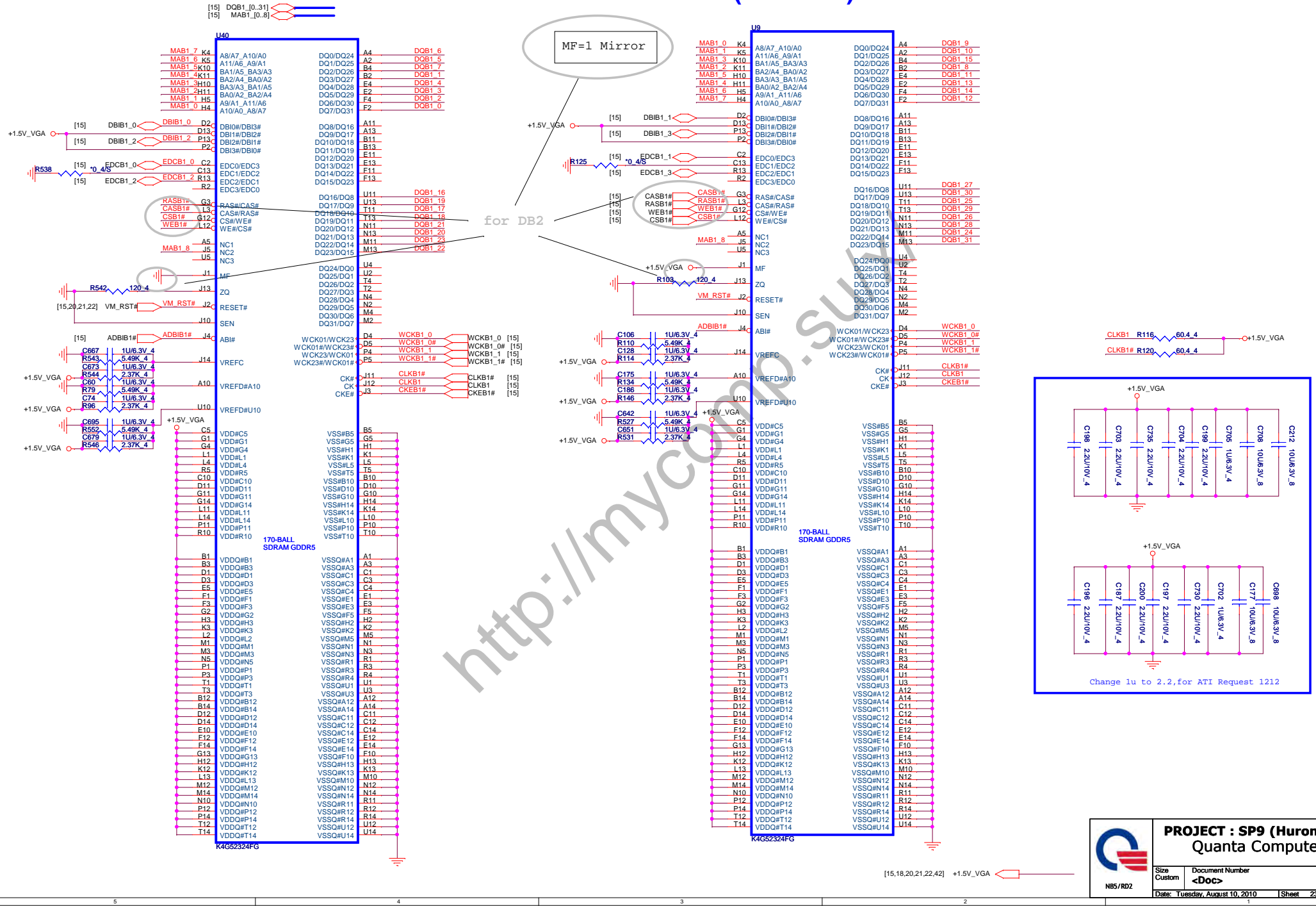


PROJECT : SP9 (Huron River)
Quanta Computer Inc.

Size Custom	Document Number <Doc>	Rev 1A
Date: Tuesday, August 10, 2010	Sheet 22 of 49	

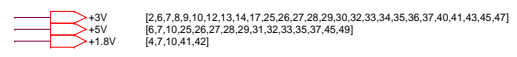
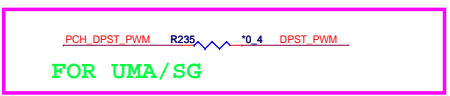
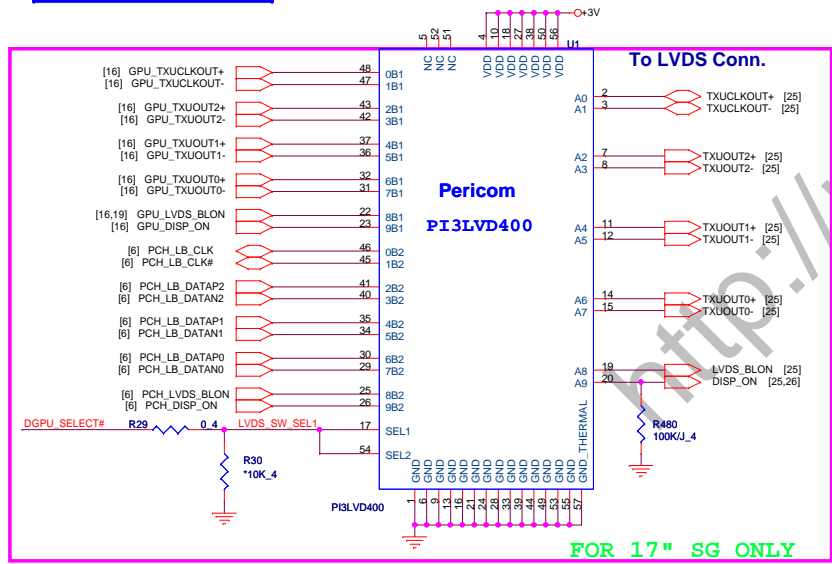
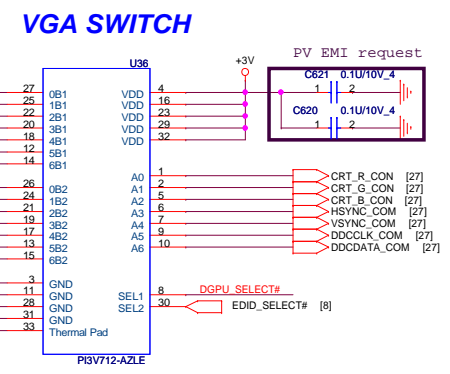
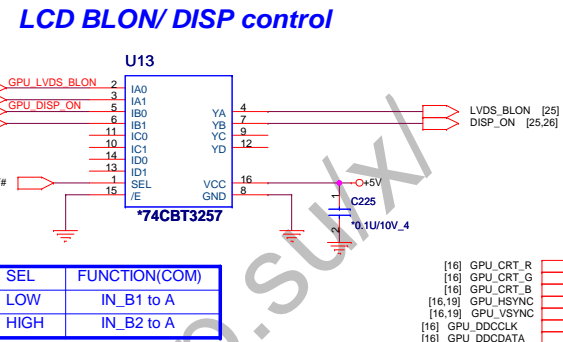
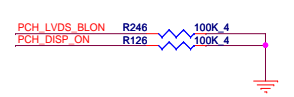
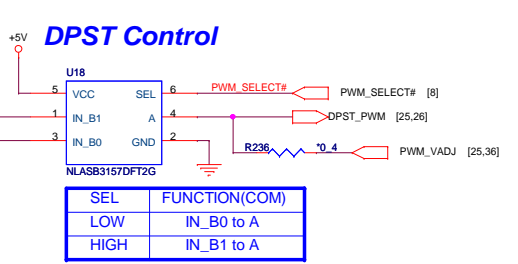
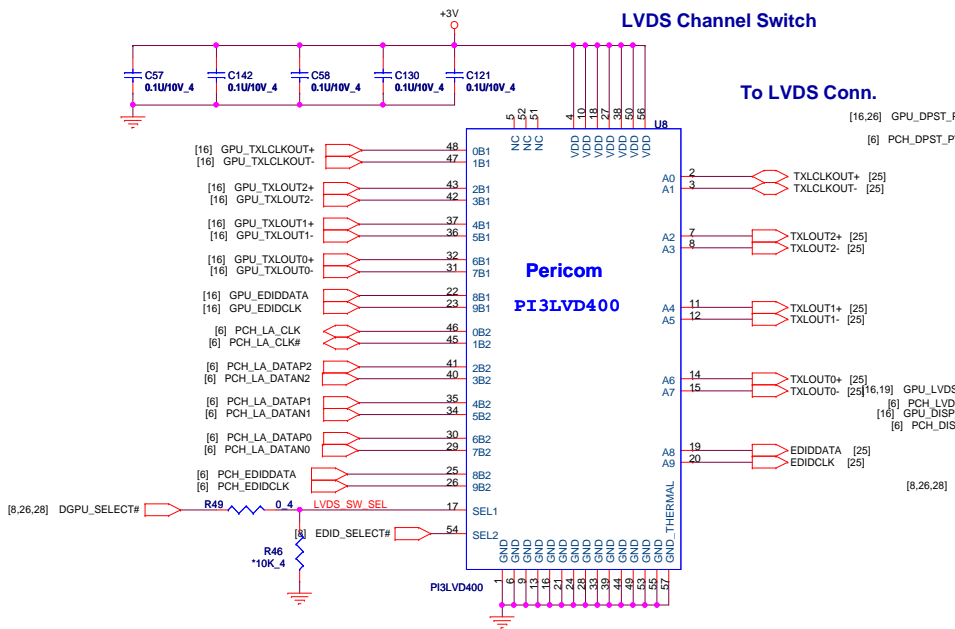
[15,18,20,21,23,42] +1.5V_VGA

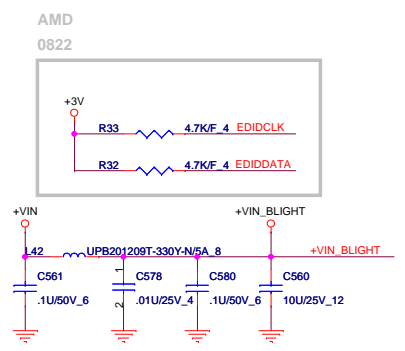
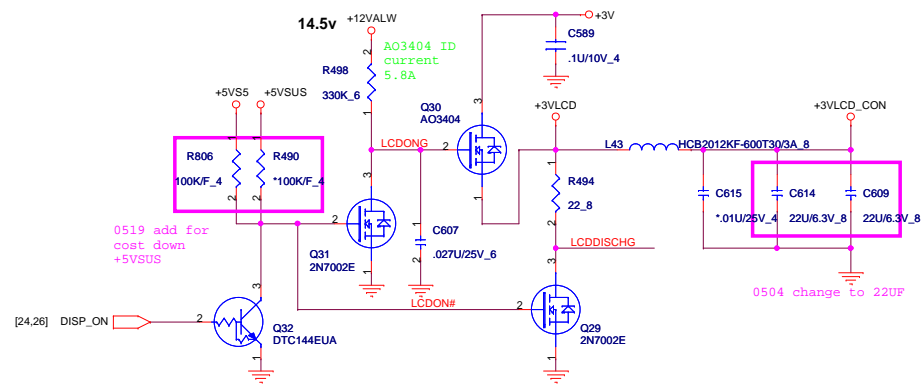
1GB GDDR5 : CHANNEL B-1 (64M x 16)



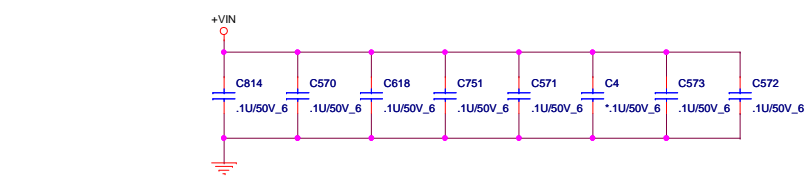
PROJECT : SP9 (Huron River)
Quanta Computer Inc.

Size Custom	Document Number <Doc>	Rev 1A
Date: Tuesday, August 10, 2010 Sheet 23 of 49		

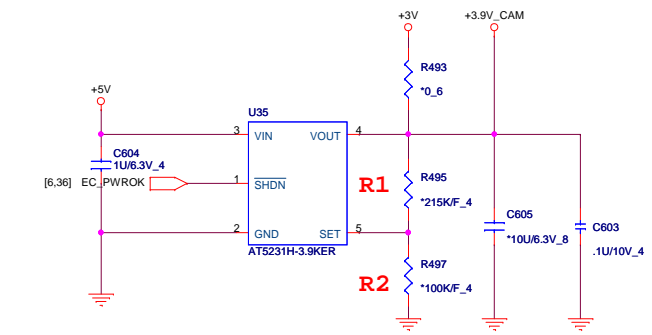
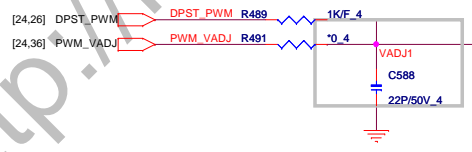
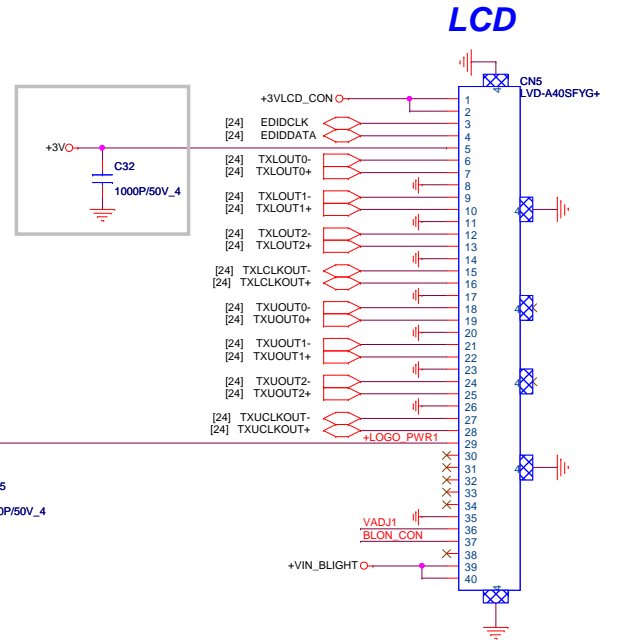
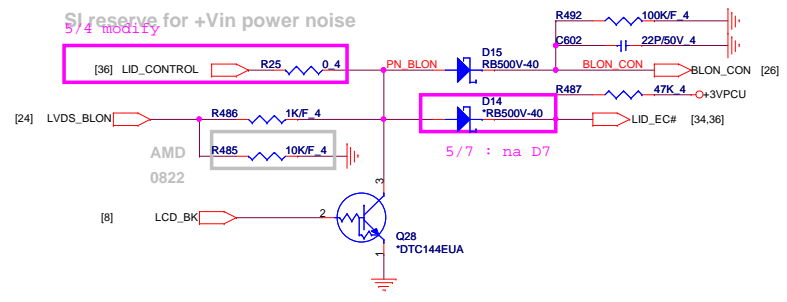
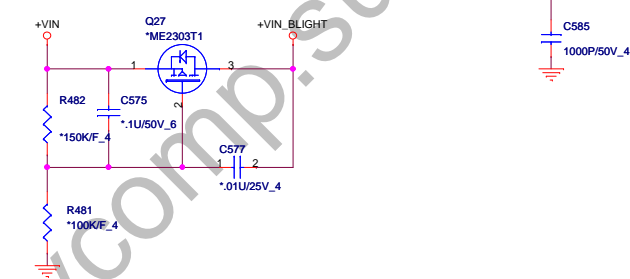




- [2,6,7,8,9,10,12,13,14,17,24,26,27,28,29,30,32,33,34,35,36,37,40,41,43,45,47]
- [6,7,10,24,26,27,28,29,31,32,33,35,37,45,49]
- [31,39,40,41,42,43,44,45,46,48]
- [6,7,34,35,36,37,39,42,43,45,46]

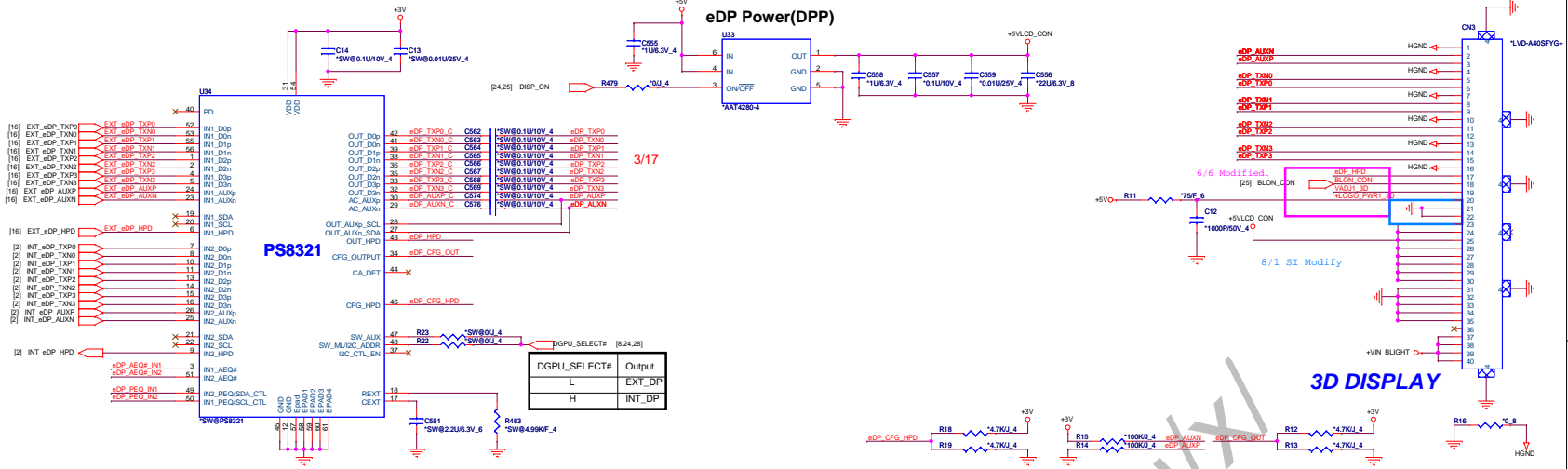


SI reserve for LCD soft start circuit



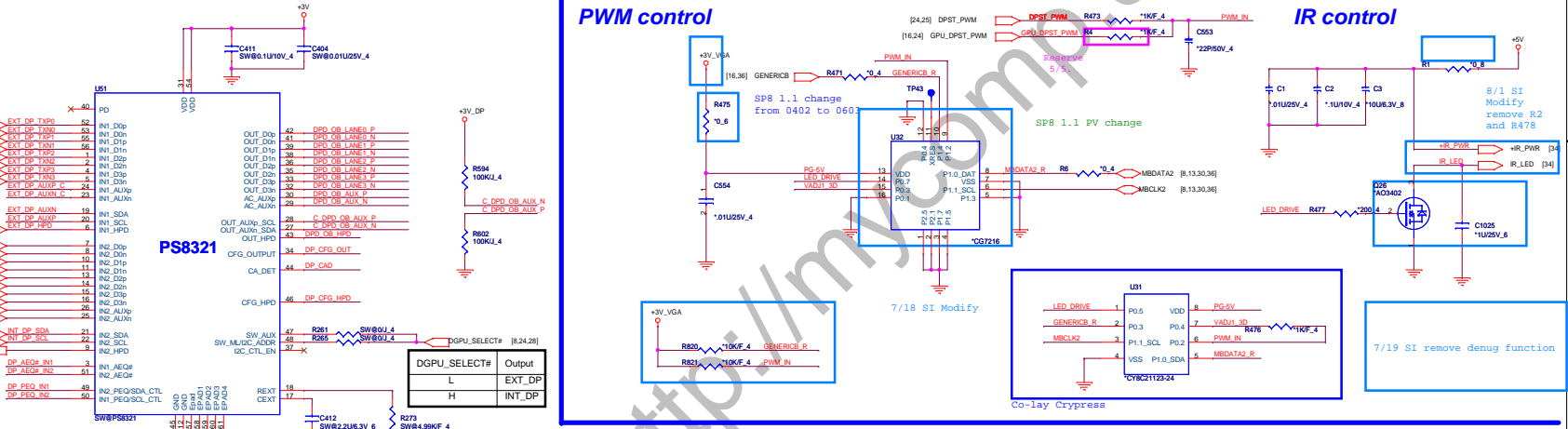
$V_{out} = 1.25(1 + R1/R2)$

eDP Power(DPP)

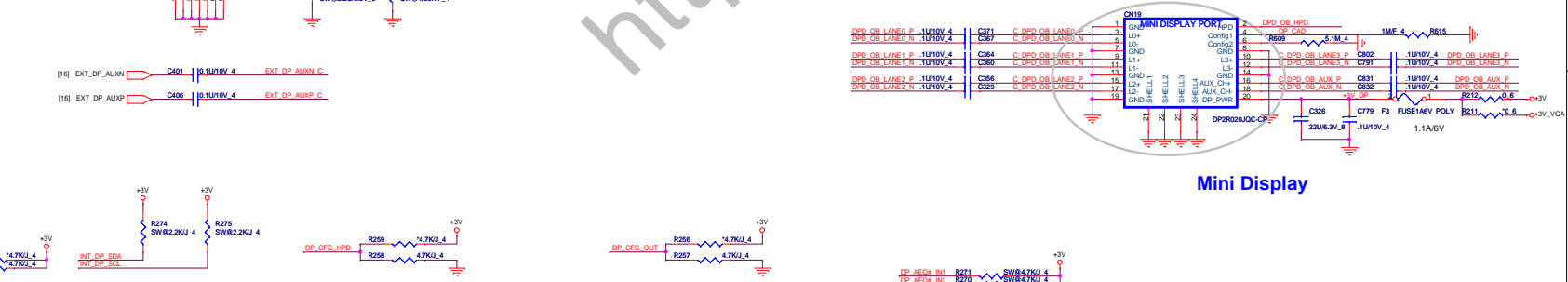


PWM control

IR control



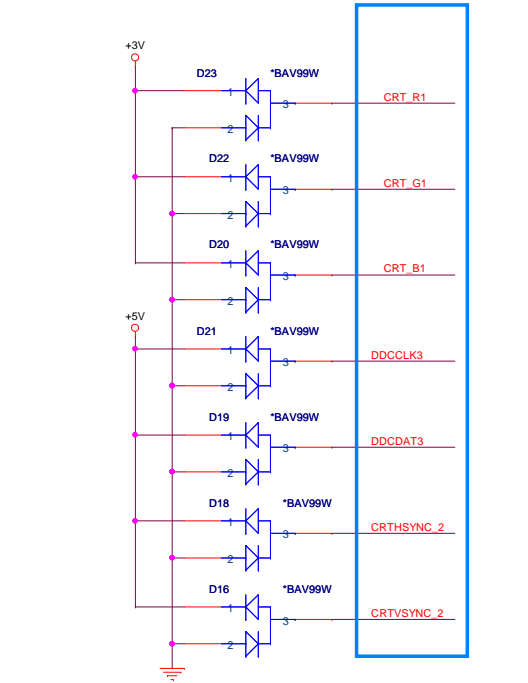
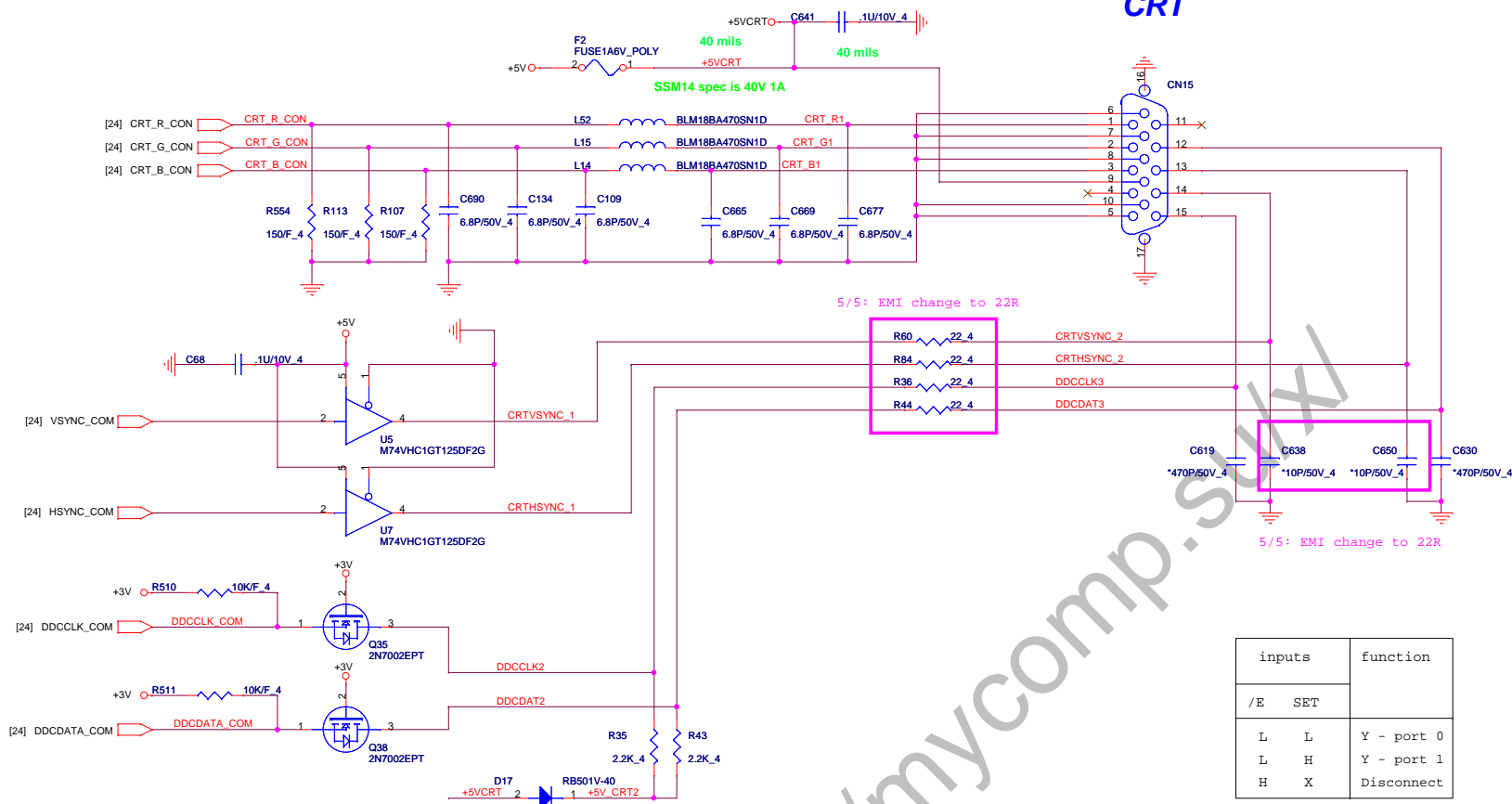
Mini Display



PROJECT : SP9 (Huron River) Quanta Computer Inc.

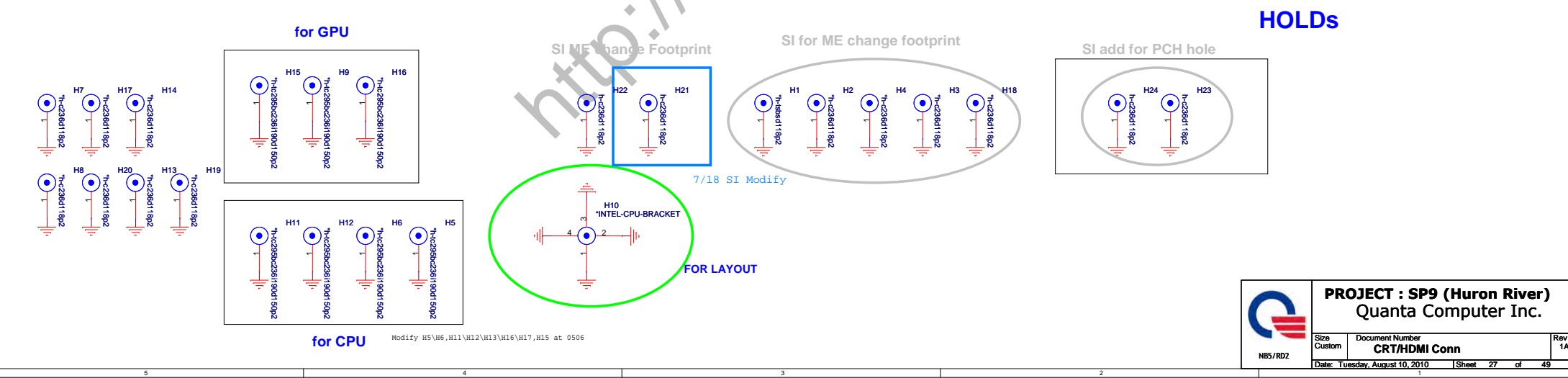
Site Custom Document Number Rev
3D eDP/Switchable DP 1A
 Date: Tuesday, August 10, 2010 1 Sheet 26 of 49

CRT



inputs		function
/E	SET	
L	L	Y - port 0
L	H	Y - port 1
H	X	Disconnect

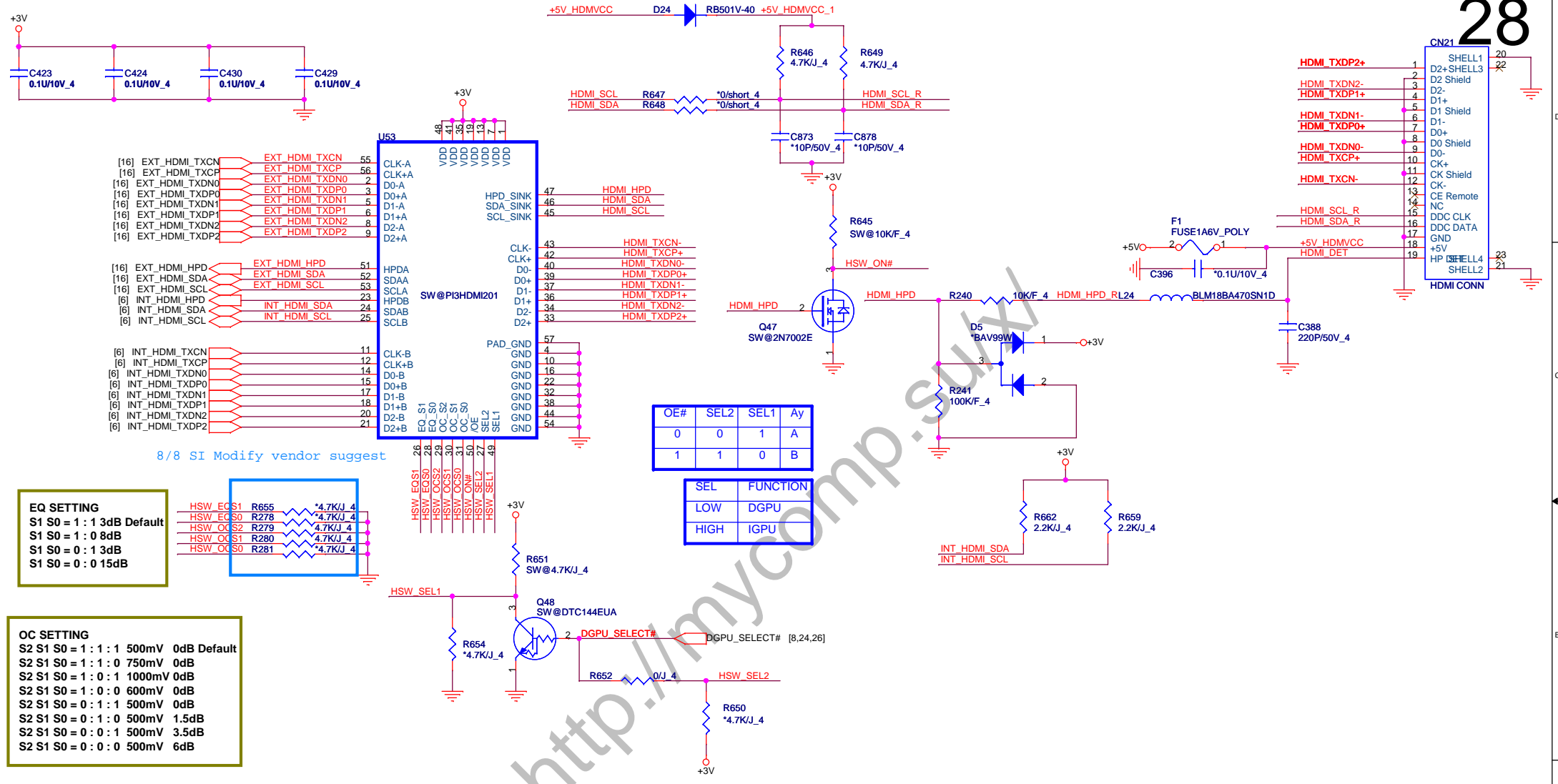
- +5V [6,7,10,24,25,26,28,29,31,32,33,35,37,45,49]
- +3V [2,6,7,8,9,10,12,13,14,17,24,25,26,28,29,30,32,33,34,35,36,37,40,41,43,45,47]
- +3V_VGA [15,16,17,18,19,26,42]



PROJECT : SP9 (Huron River)
Quanta Computer Inc.

Size Custom	Document Number CRT/HDMI Conn	Rev 1A
Date: Tuesday, August 10, 2010		Sheet 27 of 49

NB5/RD2



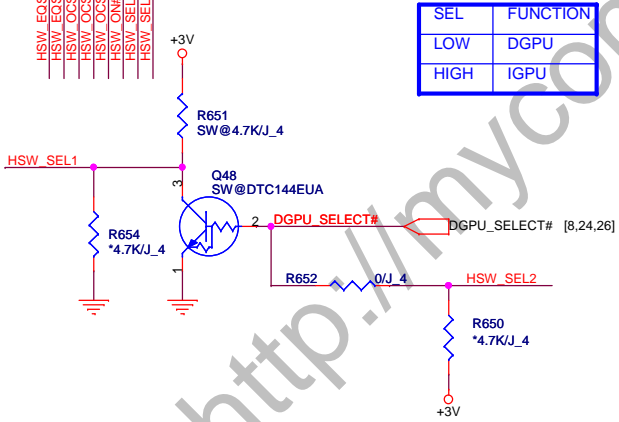
- [16] EXT_HDMI_TXCN EXT HDMI TXCN 55
- [16] EXT_HDMI_TXCP EXT HDMI TXCP 56
- [16] EXT_HDMI_TXDN0 EXT HDMI TXDN0 2
- [16] EXT_HDMI_TXDP0 EXT HDMI TXDP0 3
- [16] EXT_HDMI_TXDN1 EXT HDMI TXDN1 5
- [16] EXT_HDMI_TXDP1 EXT HDMI TXDP1 6
- [16] EXT_HDMI_TXDN2 EXT HDMI TXDN2 8
- [16] EXT_HDMI_TXDP2 EXT HDMI TXDP2 9
- [16] EXT_HDMI_HPDA EXT HDMI HPDA 51
- [16] EXT_HDMI_SDA EXT HDMI SDA 52
- [16] EXT_HDMI_SCL EXT HDMI SCL 53
- [6] INT_HDMI_HPDA INT HDMI HPDA 23
- [6] INT_HDMI_SDA INT HDMI SDA 24
- [6] INT_HDMI_SCL INT HDMI SCL 25
- [6] INT_HDMI_TXCN INT HDMI TXCN 11
- [6] INT_HDMI_TXCP INT HDMI TXCP 12
- [6] INT_HDMI_TXDN0 INT HDMI TXDN0 14
- [6] INT_HDMI_TXDP0 INT HDMI TXDP0 15
- [6] INT_HDMI_TXDN1 INT HDMI TXDN1 17
- [6] INT_HDMI_TXDP1 INT HDMI TXDP1 18
- [6] INT_HDMI_TXDN2 INT HDMI TXDN2 20
- [6] INT_HDMI_TXDP2 INT HDMI TXDP2 21

8/8 SI Modify vendor suggest

EQ SETTING
 S1 S0 = 1 : 1 3dB Default
 S1 S0 = 1 : 0 8dB
 S1 S0 = 0 : 1 3dB
 S1 S0 = 0 : 0 15dB



OC SETTING
 S2 S1 S0 = 1 : 1 : 1 500mV 0dB Default
 S2 S1 S0 = 1 : 1 : 0 750mV 0dB
 S2 S1 S0 = 1 : 0 : 1 1000mV 0dB
 S2 S1 S0 = 1 : 0 : 0 600mV 0dB
 S2 S1 S0 = 0 : 1 : 1 500mV 0dB
 S2 S1 S0 = 0 : 1 : 0 500mV 1.5dB
 S2 S1 S0 = 0 : 0 : 1 500mV 3.5dB
 S2 S1 S0 = 0 : 0 : 0 500mV 6dB



OE#	SEL2	SEL1	Ay
0	0	1	A
1	1	0	B

SEL	FUNCTION
LOW	DGPU
HIGH	IGPU

PROJECT : SP9 (Huron River)
Quanta Computer Inc.

Size Custom	Document Number SG HDMI Conn	Rev 1A
Date: Tuesday, August 10, 2010		
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[2,6,7,8,9,10,12,13,14,17,24,25,26,27,28,30,32,33,34,35,36,37,40,41,43,45,47] +3V
[30,31] +5V_AVDD
[6,7,10,24,25,26,27,28,31,32,33,35,37,45,49] +5V

SI change footprint from 0603 to 0805 for IDT comfirm

Close to CODEC

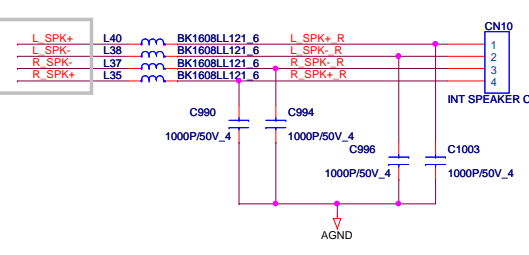
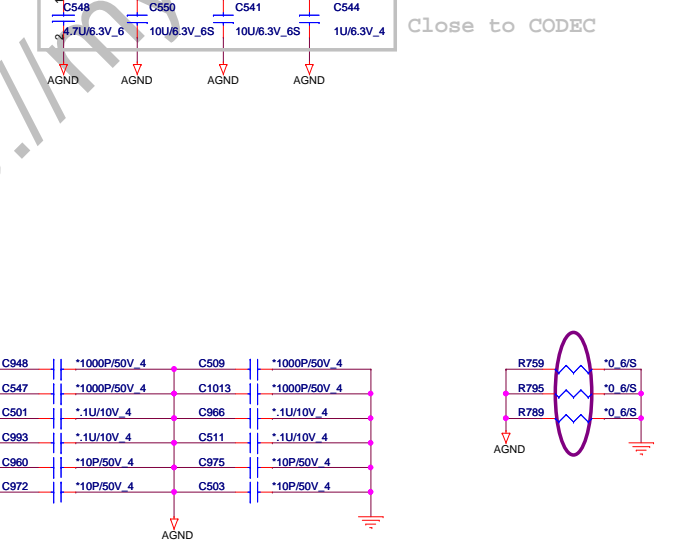
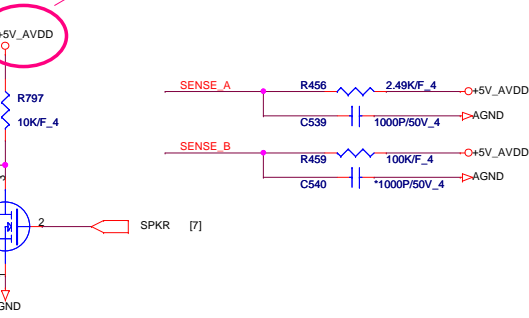
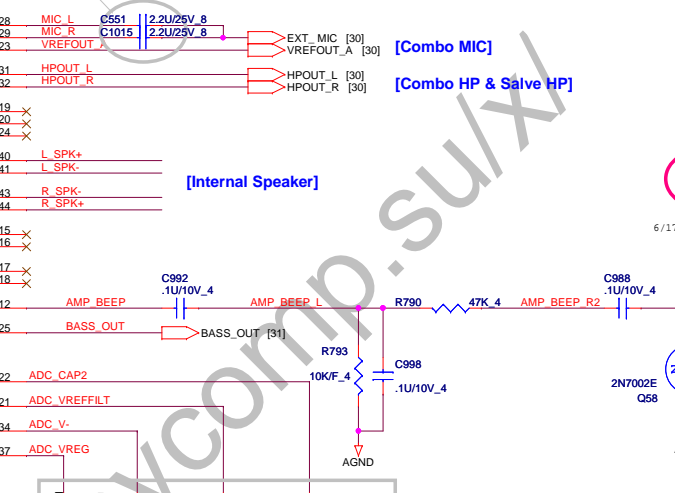
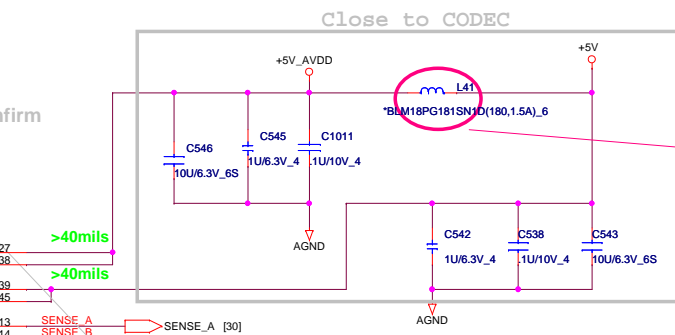
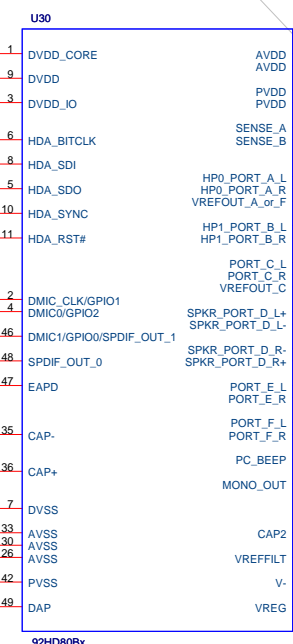
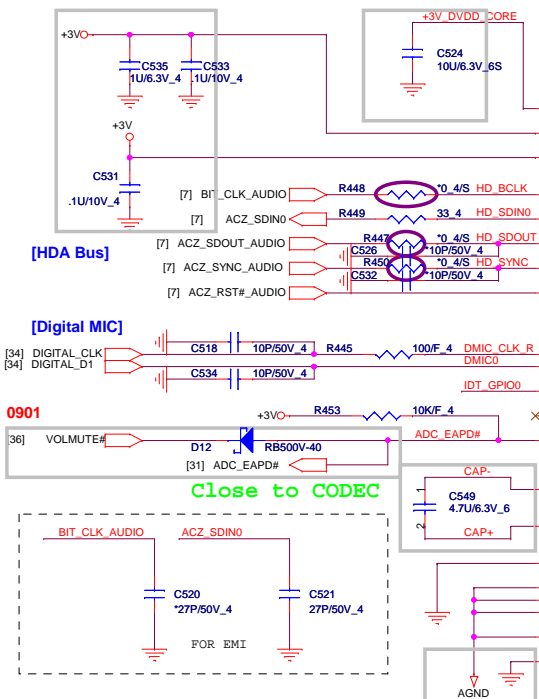
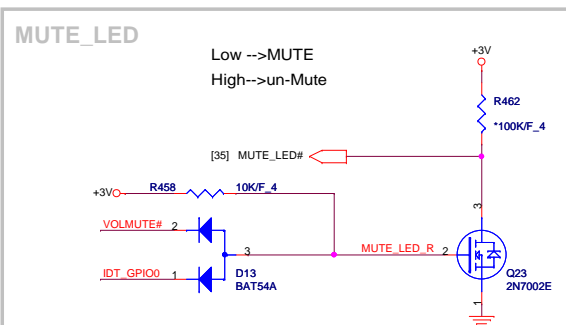
Close to CODEC

PV non-Staff

PV Change from +5V to +5V_ADD

Close to CODEC

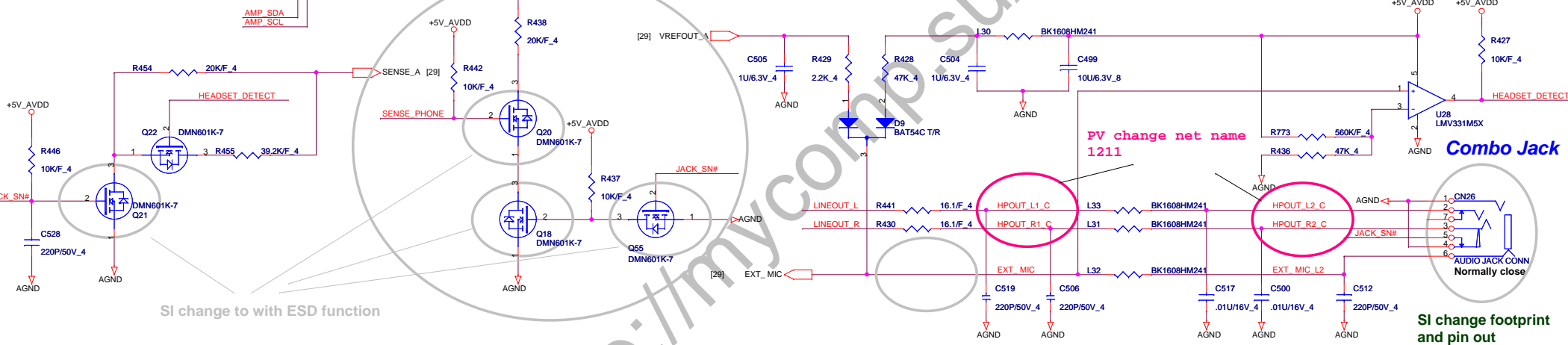
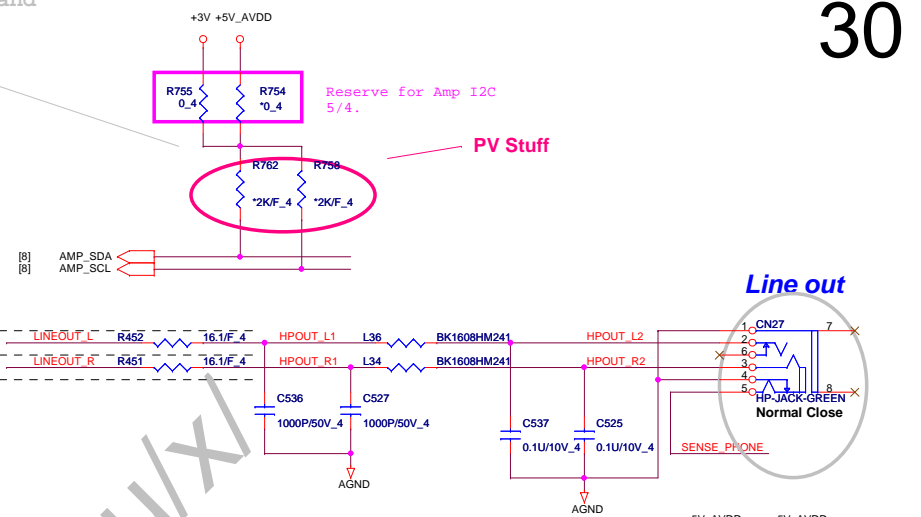
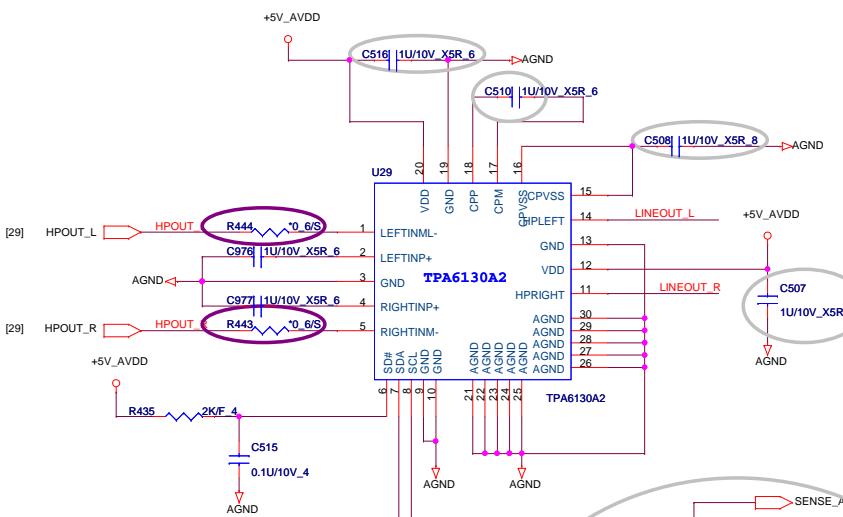
INT. SPEAKER



PROJECT : SP9 (Huron River)
Quanta Computer Inc.

Size Custom	Document Number Azalia 92HD80	Rev 1A
NBS/RD2	Date: Tuesday, August 10, 2010	Sheet 29 of 49

SI change to TPA6130A2 and modify sense circuit

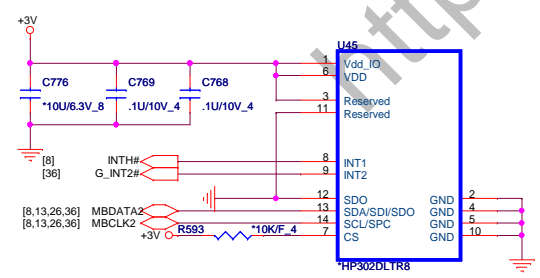


SI change to with ESD function

PV change net name 1211

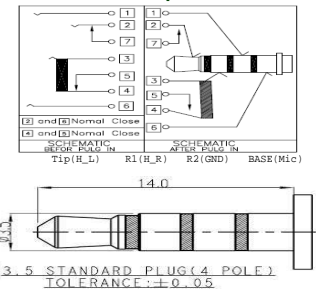
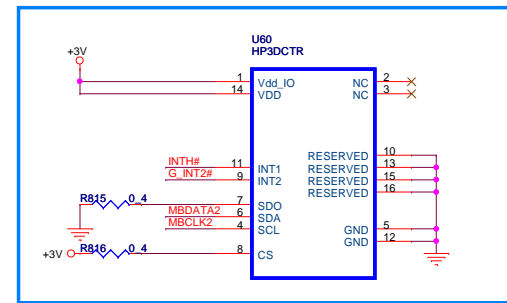
SI change footprint and pin out

Accelerometer Sensor



Pin 12: Low 38hex
 Pin 12: unconnected/floating 3Ahex

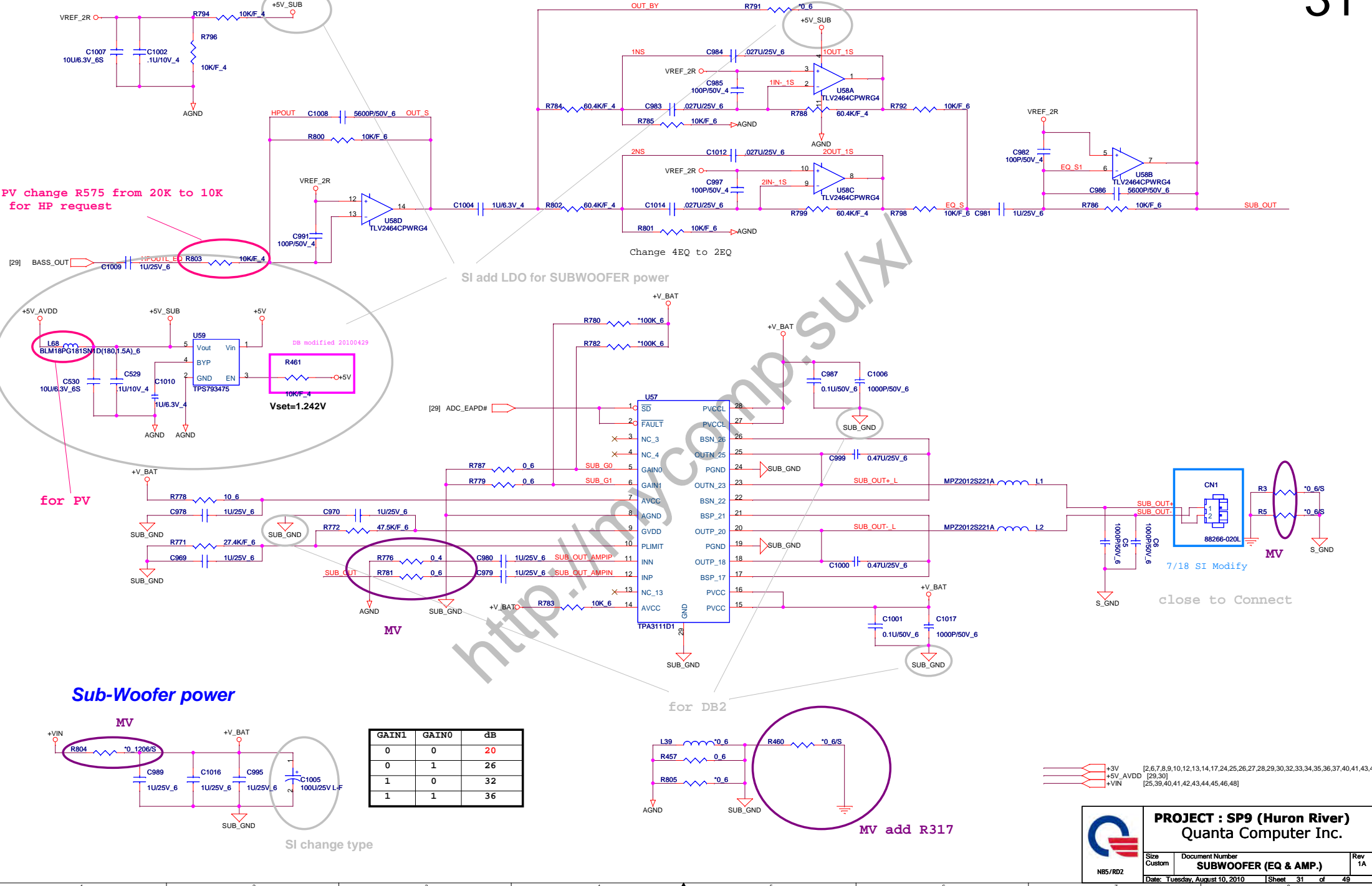
7/18: SI Add



PROJECT : SP9 (Huron River)
Quanta Computer Inc.

Size Custom	Document Number AMP_TPA6047/Accelerometer	Rev 1A
NBS/RD2	Date: Tuesday, August 10, 2010	Sheet 30 of 49

SUBWOOFER



PV change R575 from 20K to 10K for HP request

SI add LDO for SUBWOOFER power

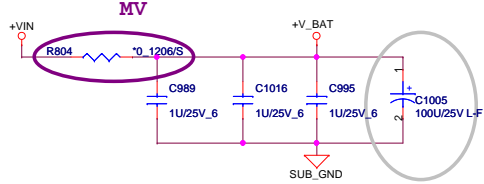
for PV

MV

MV

close to Connect

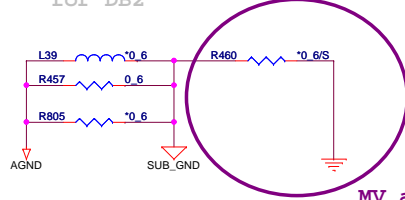
Sub-Woofer power



SI change type

GAIN1	GAIN0	dB
0	0	20
0	1	26
1	0	32
1	1	36

for DB2

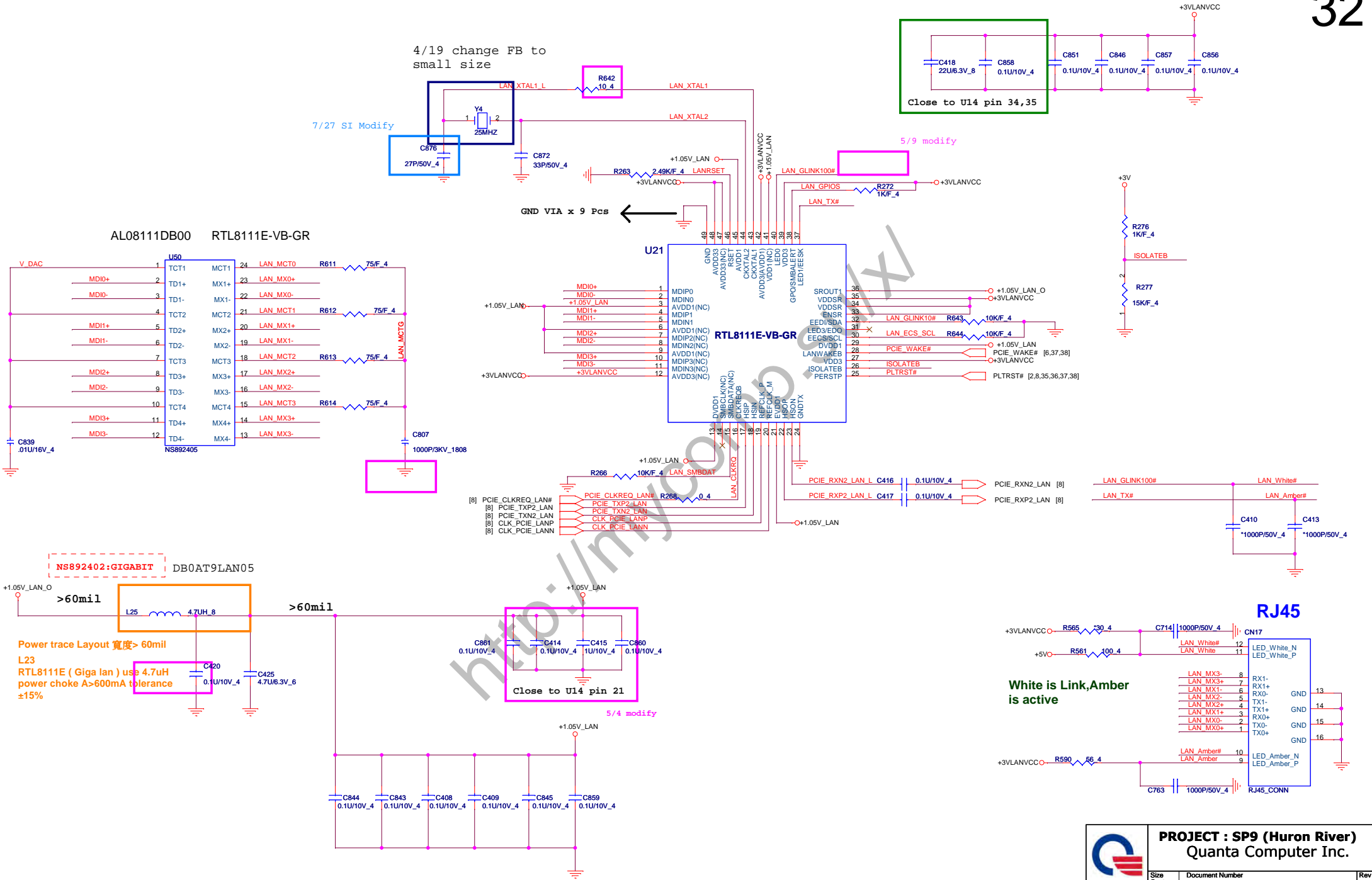


MV add R317

+3V [2,6,7,8,9,10,12,13,14,17,24,25,26,27,28,29,30,32,33,34,35,36,37,40,41,43,45,47]
 +5V_AVDD [29,30]
 +VIN [25,39,40,41,42,43,44,45,46,48]

PROJECT : SP9 (Huron River)
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
SUBWOOFER (EQ & AMP.)		
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4/19 change FB to small size

7/27 SI Modify

5/9 modify

GND VIA x 9 Pcs


NS892402: GIGABIT DB0AT9LAN05

Power trace Layout 宽度 > 60mil
 L23
 RTL8111E (Giga lan) use 4.7uH power choke A>600mA tolerance ±15%

Close to U14 pin 21

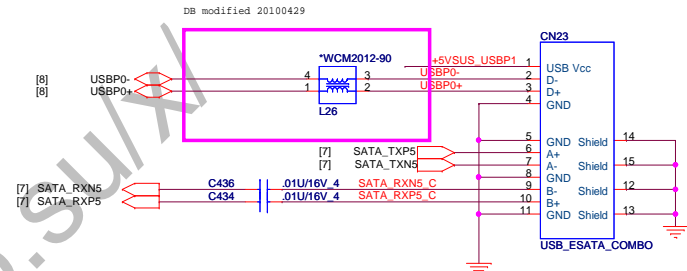
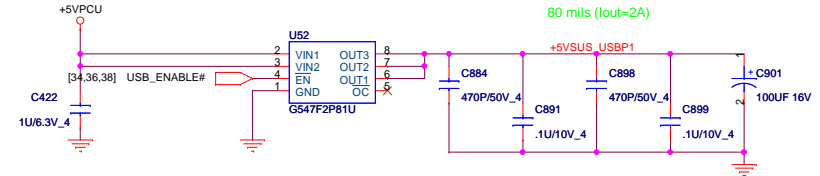
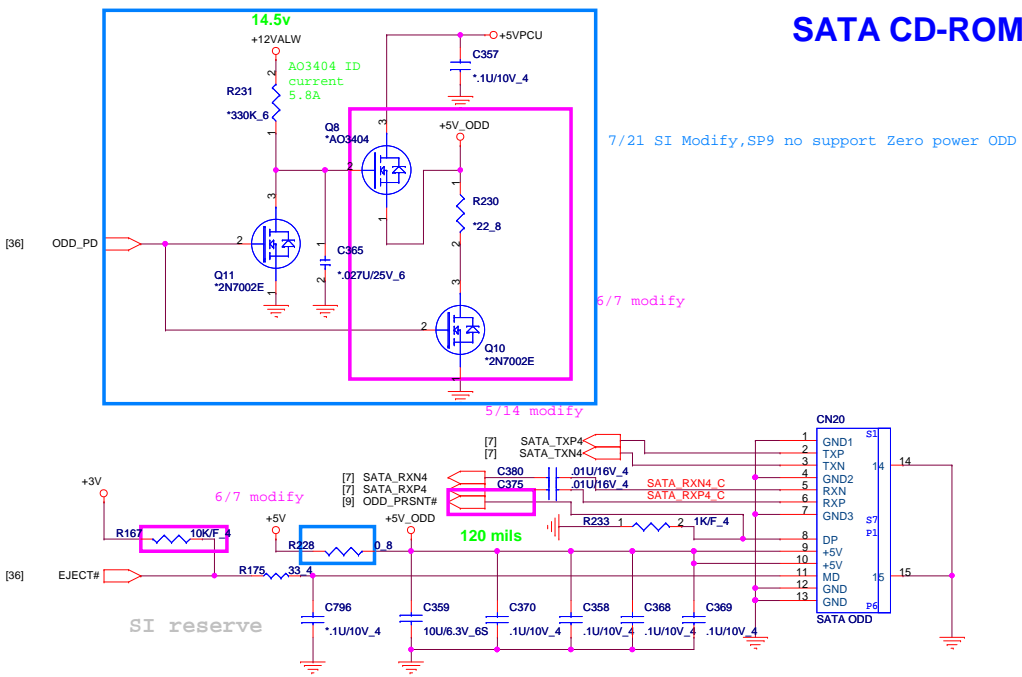
5/4 modify

White is Link, Amber is active

 PROJECT : SP9 (Huron River) Quanta Computer Inc.		
Size Custom	Document Number 8111E/RJ45	Rev 1A
Date: Tuesday, August 10, 2010 Sheet 32 of 49		

SATA CD-ROM

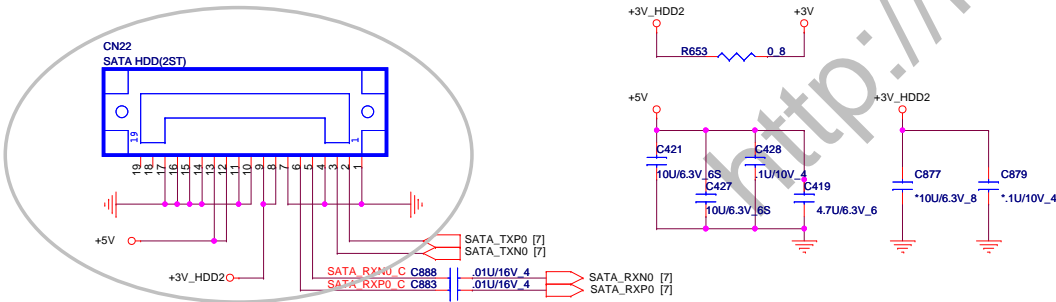
E-SATA



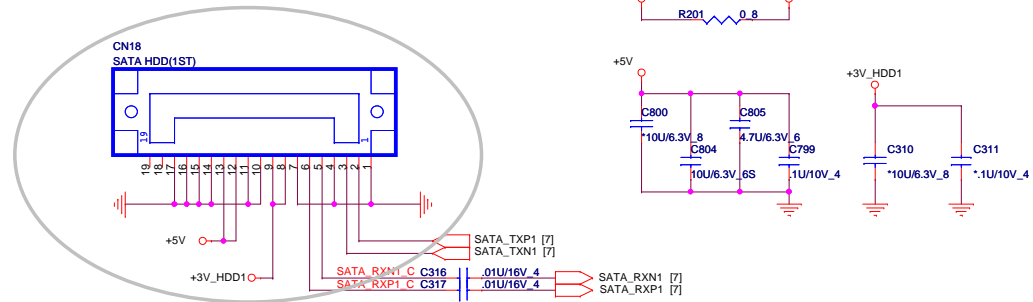
SATA HDD #1


SATA HDD #2

SI change pin define and footprint (the same AX)



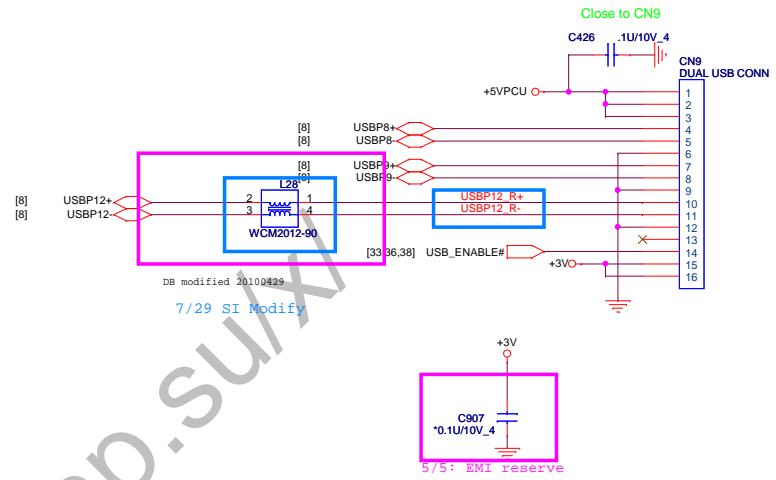
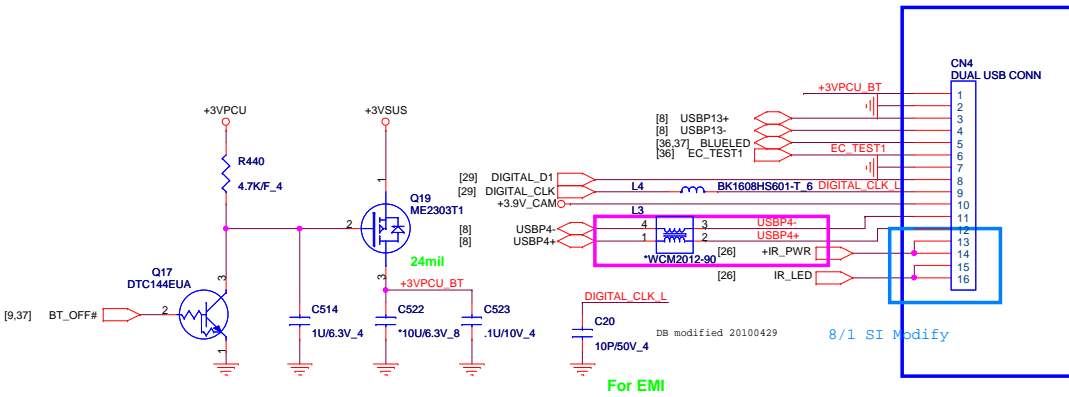
SI change pin define and footprint (the same AX)



 PROJECT : SP9 (Huron River) Quanta Computer Inc.		
Size Custom	Document Number	Rev 1A
ODD/HDD/ONFI		
Date: Tuesday, August 10, 2010 Sheet 33 of 49		

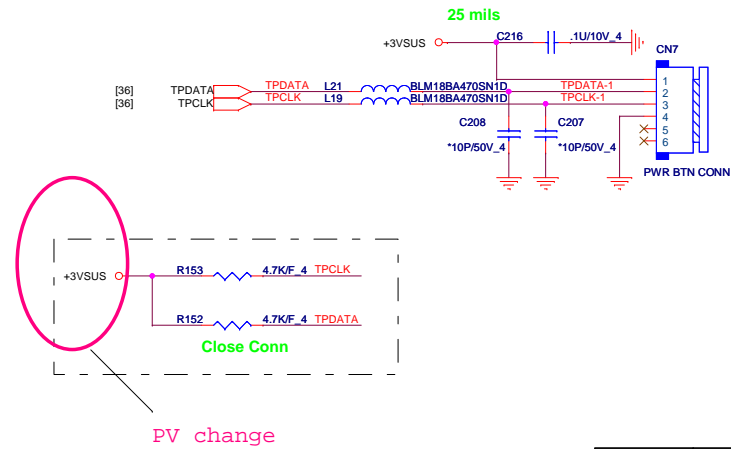
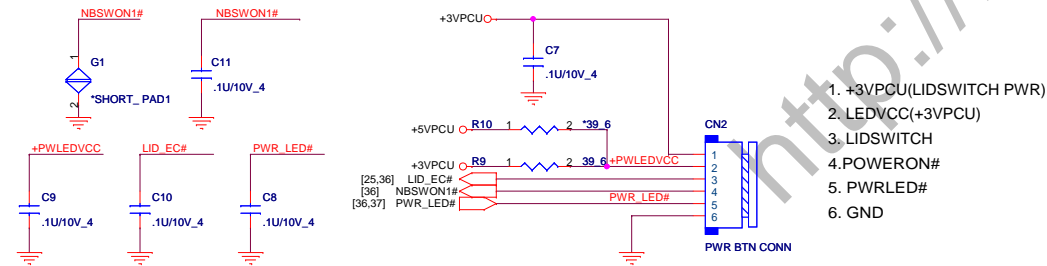
Bluetooth

Ext USB & Card Reader

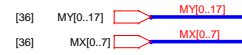


Power Button

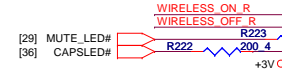
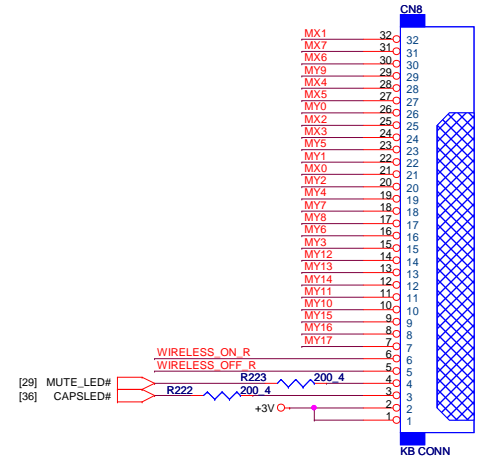
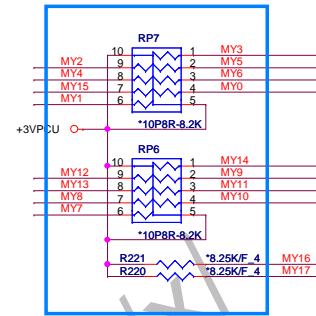
Touch Pad Button



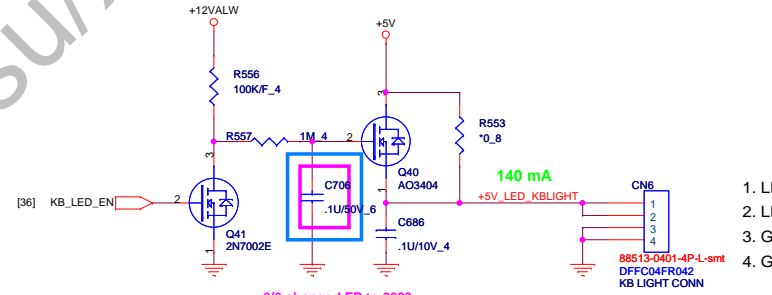
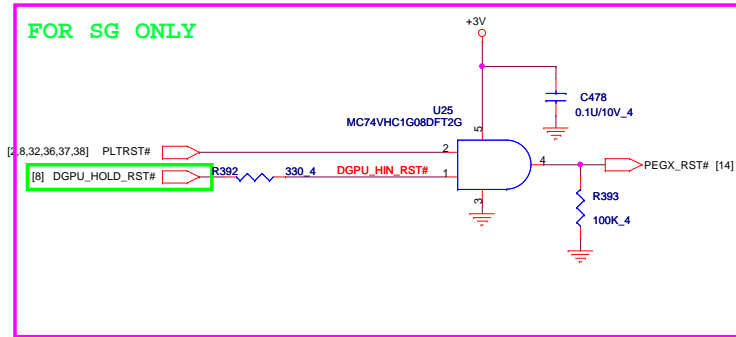
Mini Display



8/5 SI modify

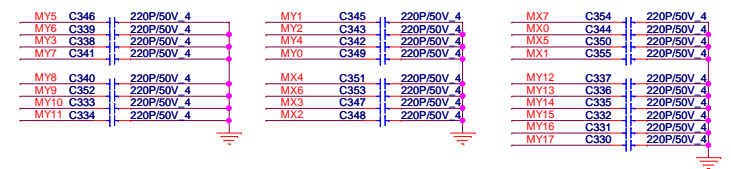


FOR SG ONLY

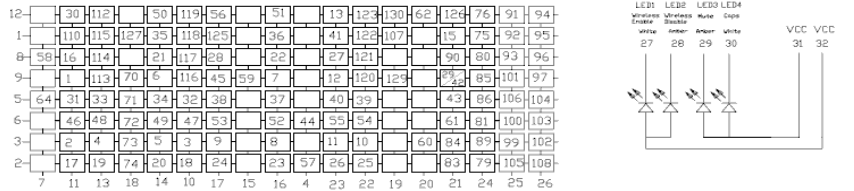
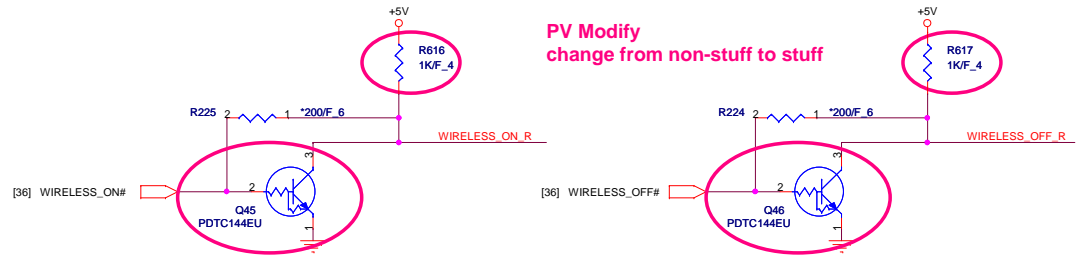


1. LEDVCC
2. LEDVCC
3. GND
4. GND

6/6 changed FP to 0603
 7/18 SI modify



PV Modify
 change from non-stuff to stuff

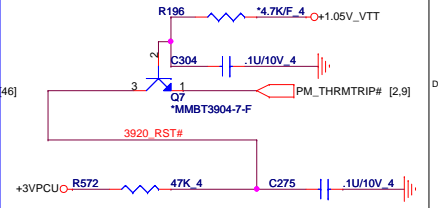


PROJECT : SP9 (Huron River)
Quanta Computer Inc.

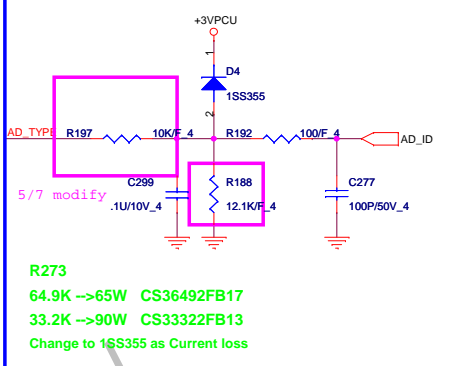
Size Custom	Document Number KB/LED/POWER CONN	Rev 1A
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http://mycomp.su/...

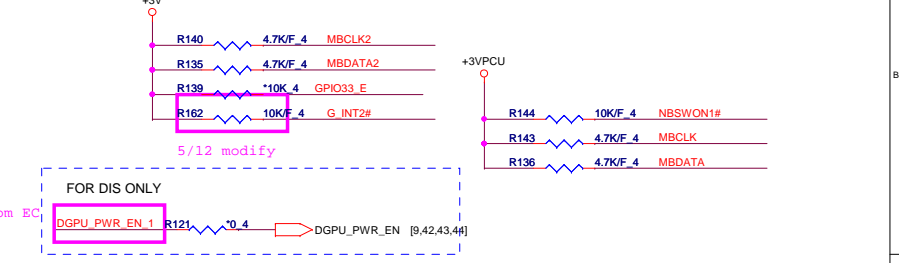
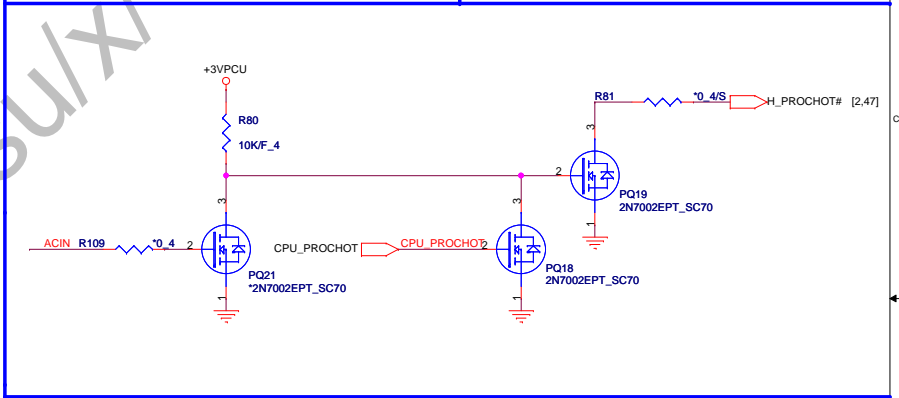
Thermal Shutdown



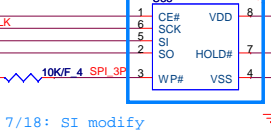
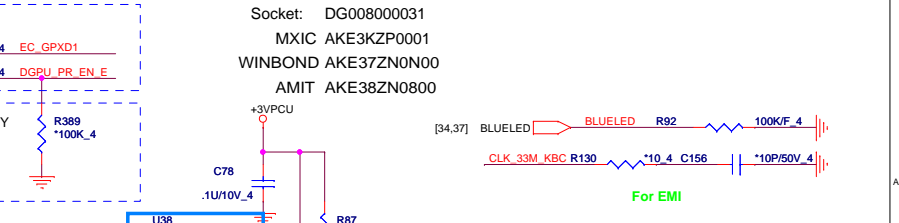
Adapter Type



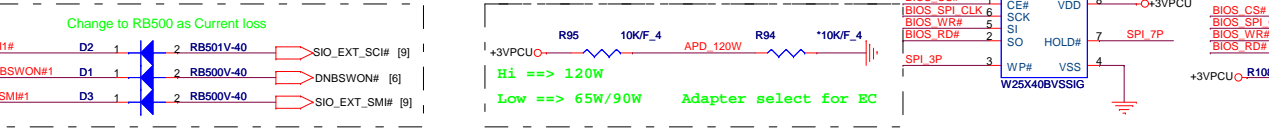
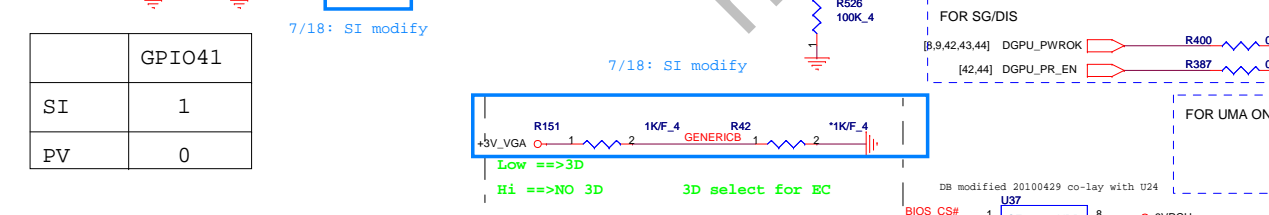
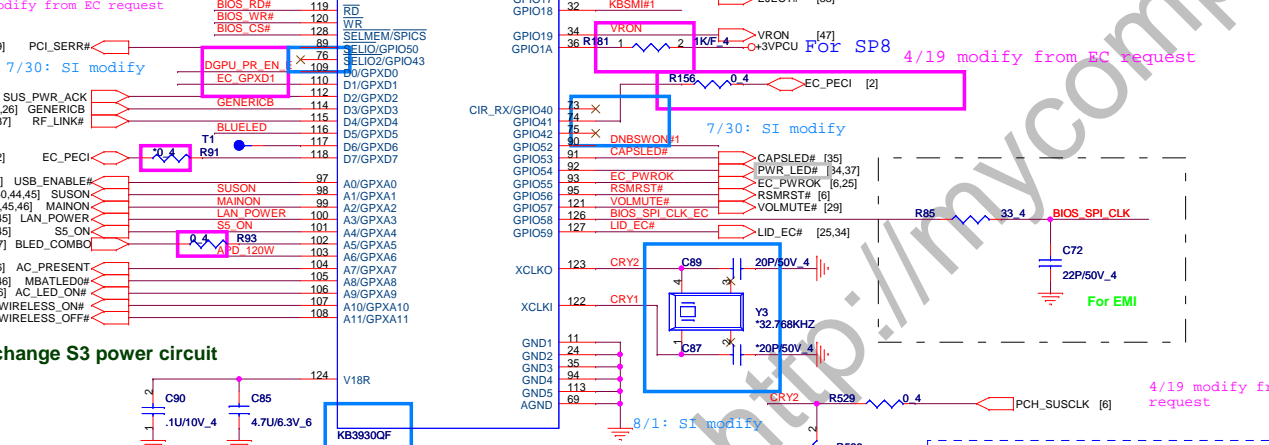
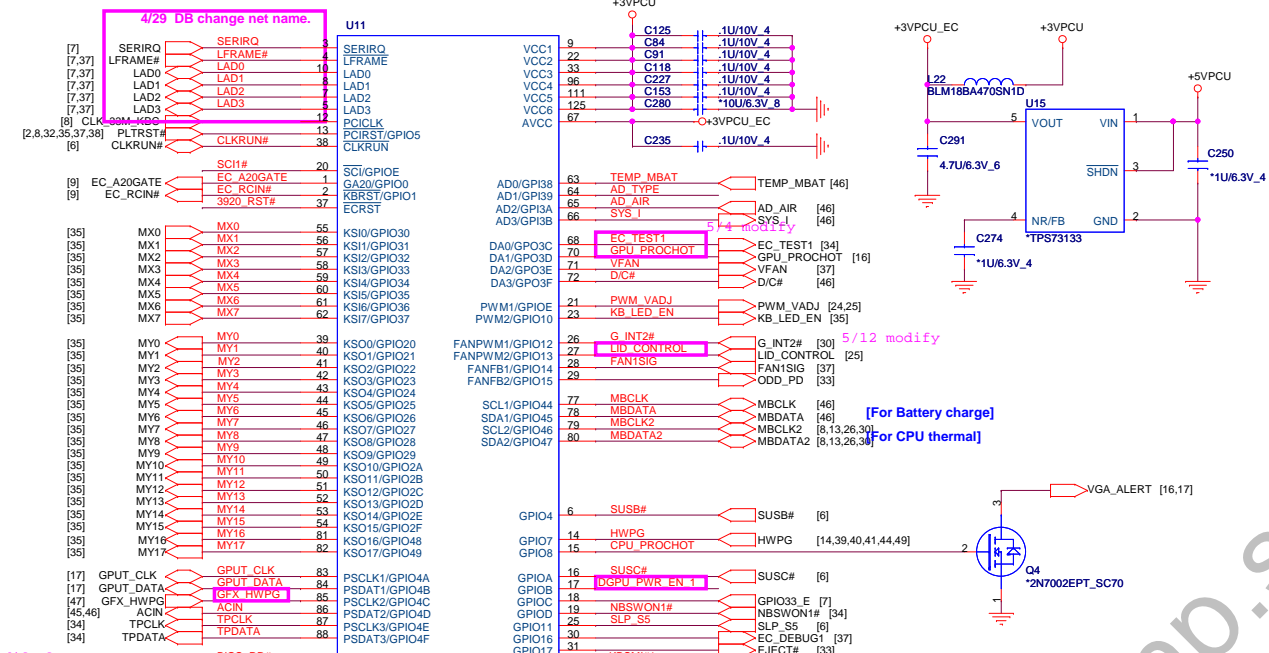
R273
64.9K -> 65W CS36492FB17
33.2K -> 90W CS33322FB13
Change to 1SS355 as Current loss



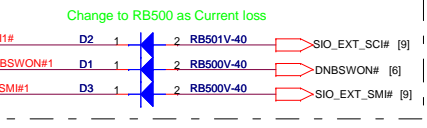
Socket: DG008000031
MXIC AKE3KZP0001
WINBOND AKE37ZN0N00
AMIT AKE38ZN0800



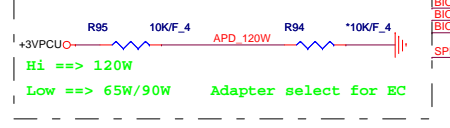
7/18: SI modify



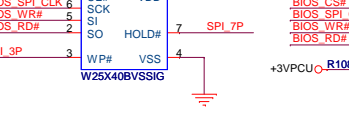
GPIO41	
SI	1
PV	0



Change to RB500 as Current loss



Hi ==> NO 3D
3D select for EC
Hi ==> 120W
Low ==> 65W/90W
Adapter select for EC



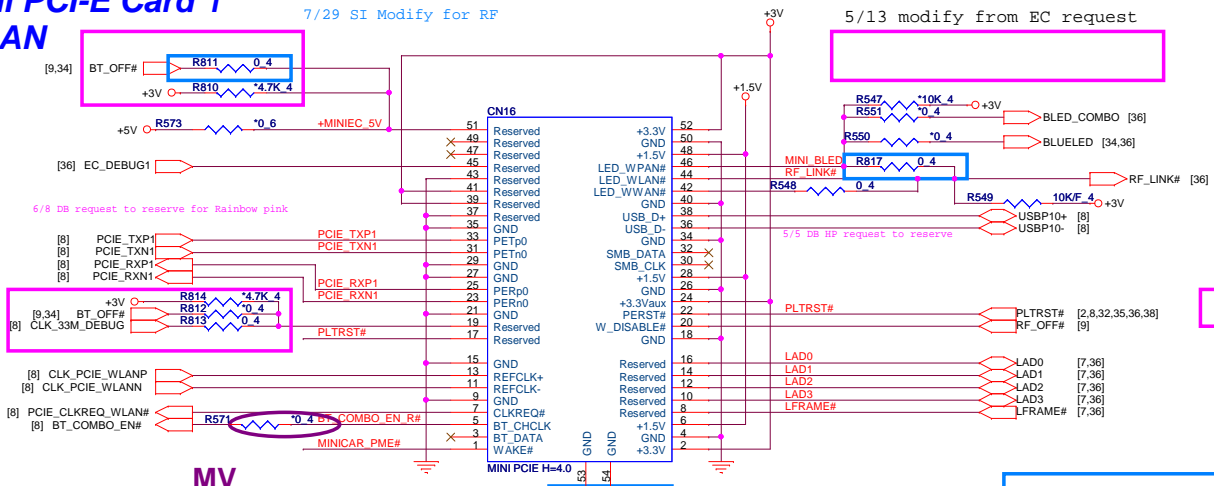
DB modified 20100429 co-lay with U24

PROJECT : SP9 (Huron River)
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
KB3926/ROM/TP		
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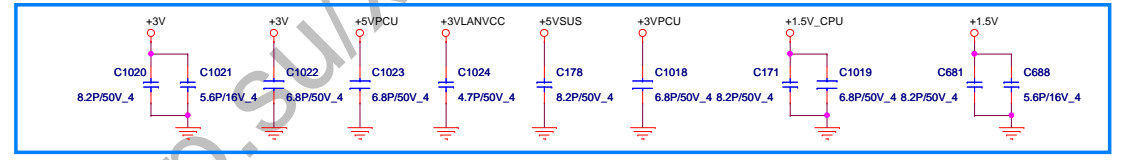
Mini PCI-E Card 1 WLAN

7/29 SI Modify for RF

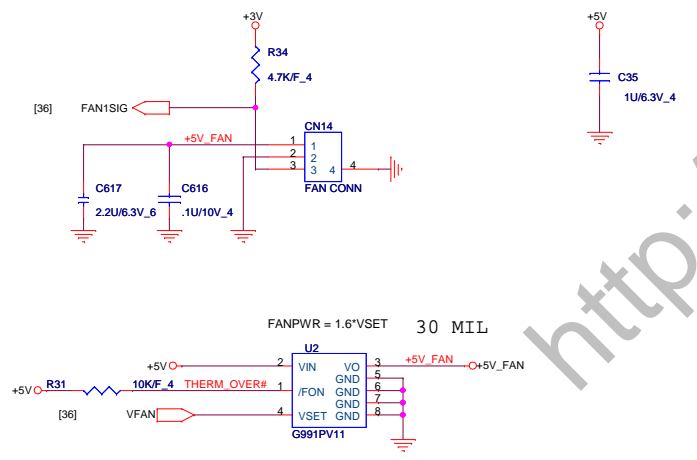


PV non-stuff

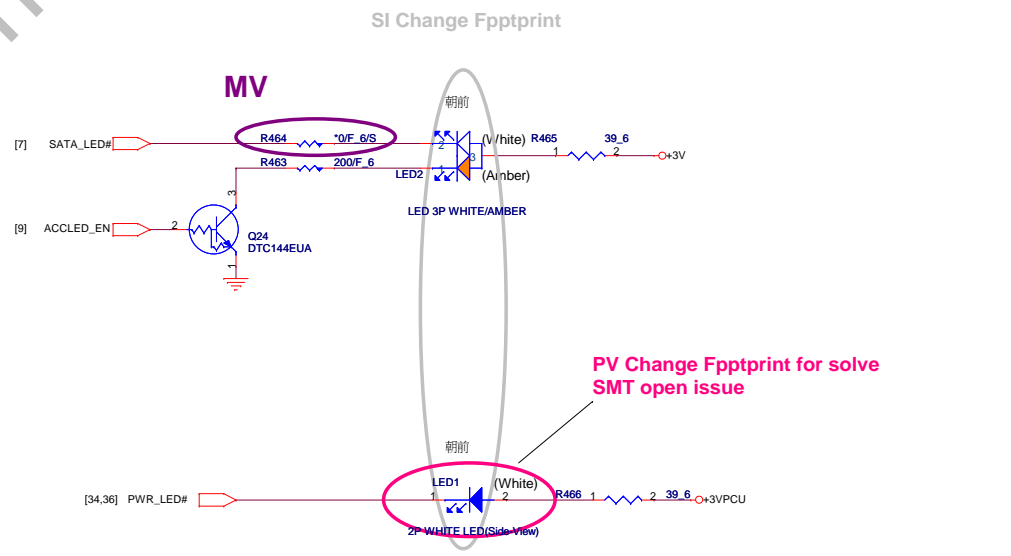
For EMI



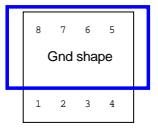
CPU FAN



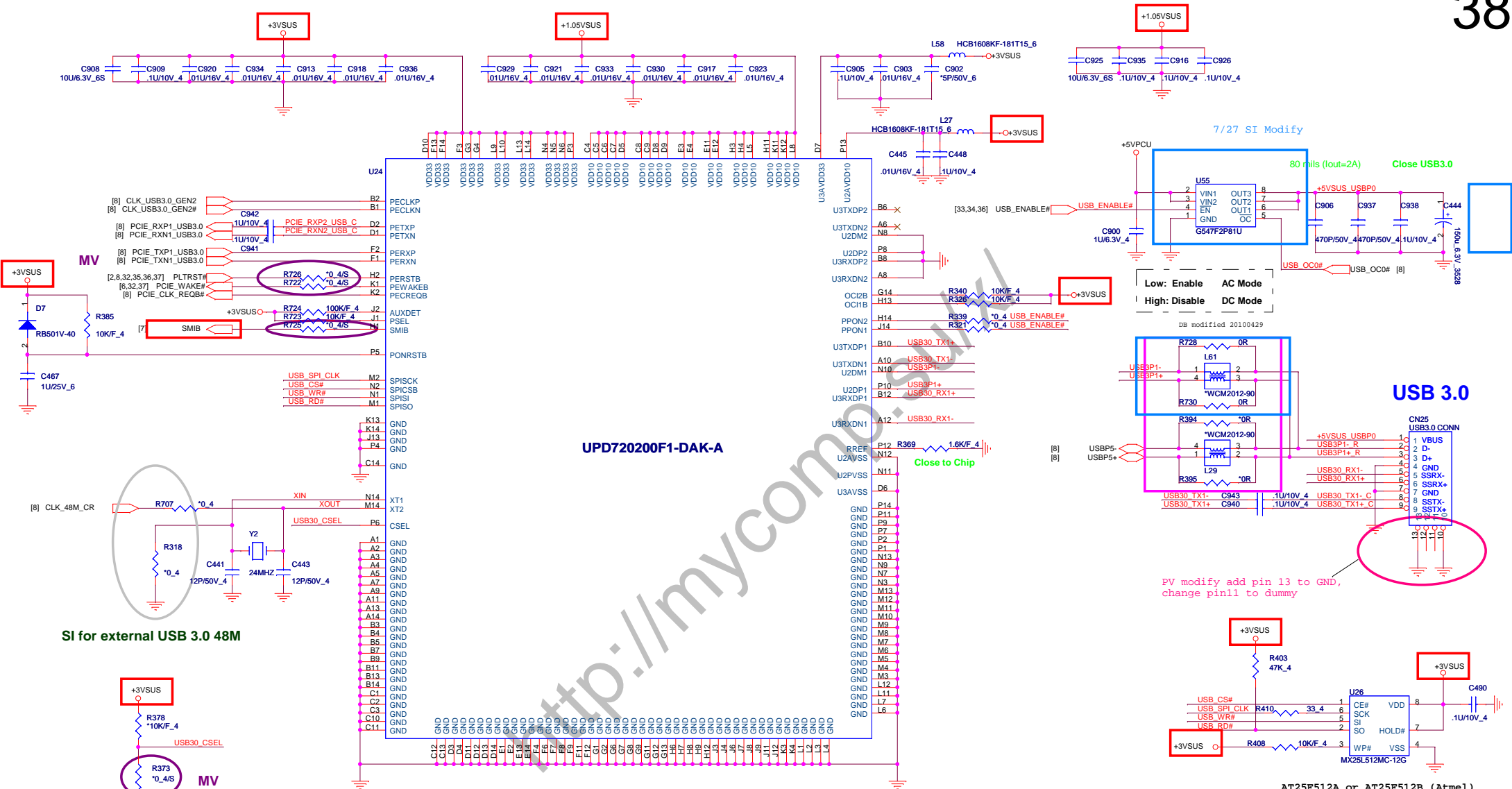
LED



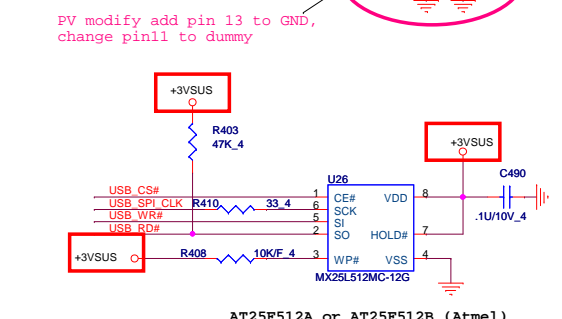
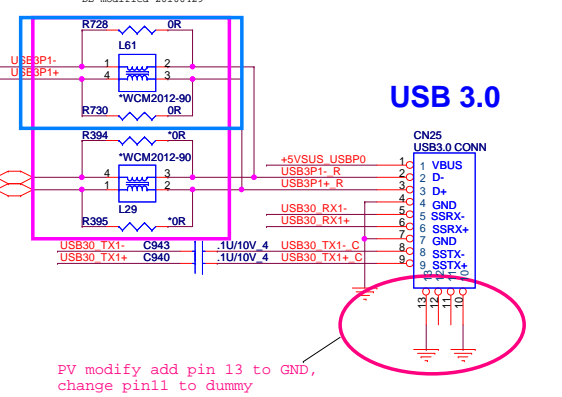
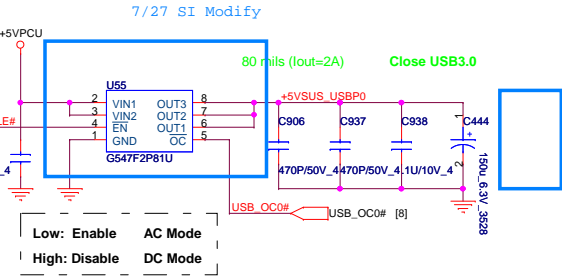
G995 layout notice



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	Quanta Computer Inc.		
Size Custom	Document Number	MINI PCI-E CONN X2	Sheet 37 of 49
NB5/RD2	Date: Tuesday, August 10, 2010		



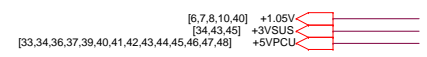
UPD720200F1-DAK-A



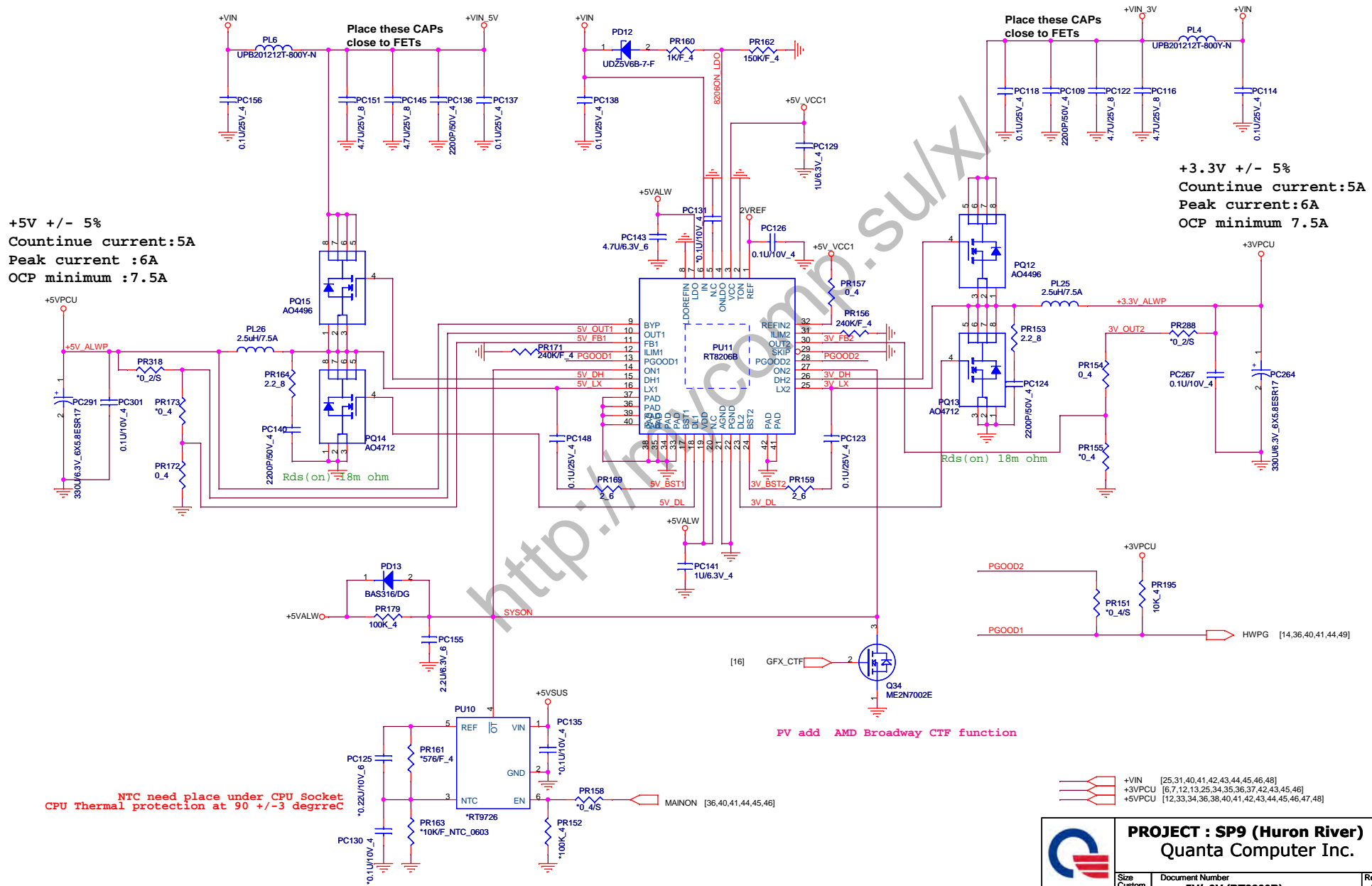
SI for external USB 3.0 48M


Clock select signal	
USB3.0_CSEL	High = External 48Mhz
	Low = 24MHz X'tal

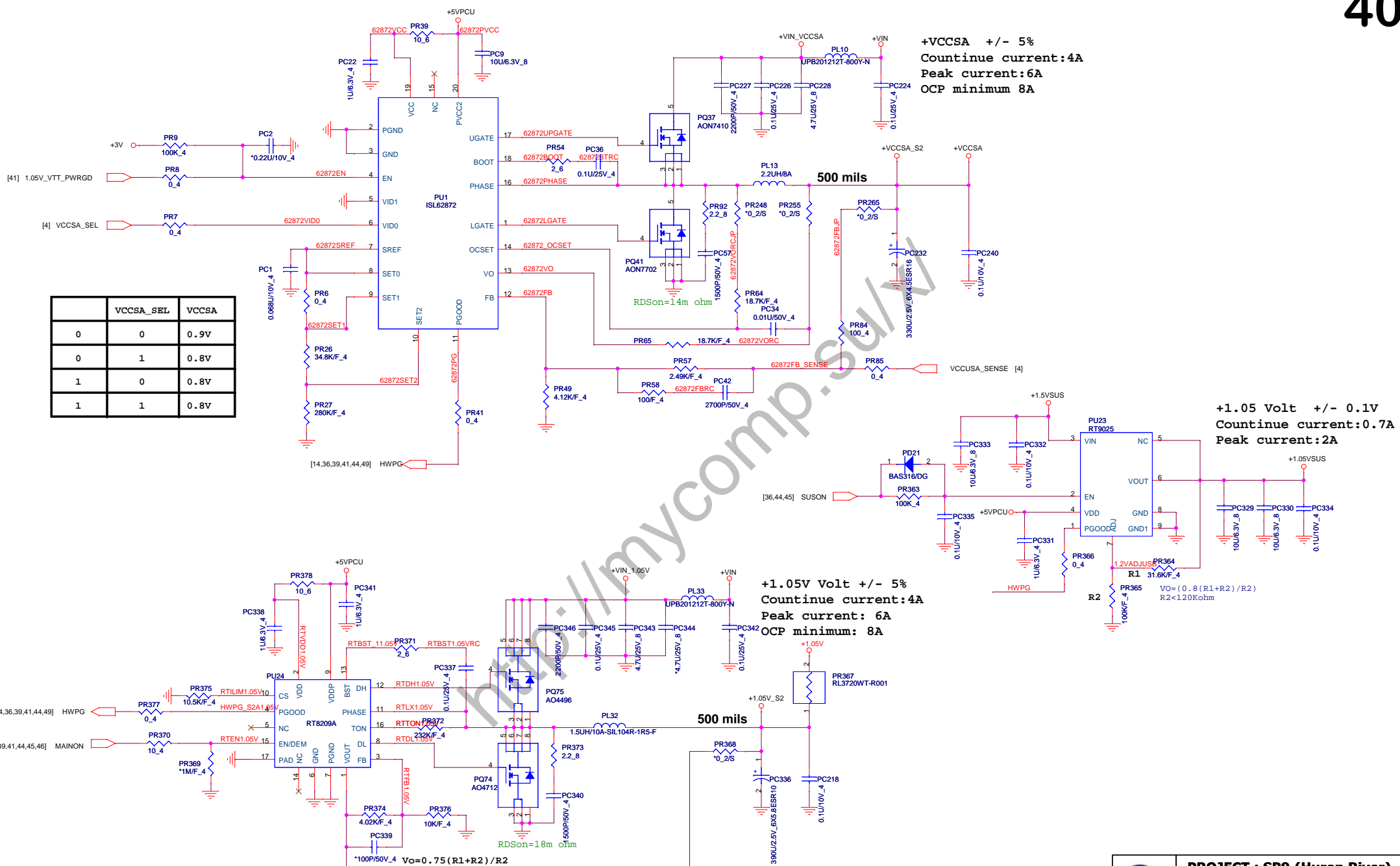
AT25F512A or AT25F512B (Atmel)
MX25L512 (Macronix)



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	VCCSA_SEL	VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.8V
1	1	0.8V

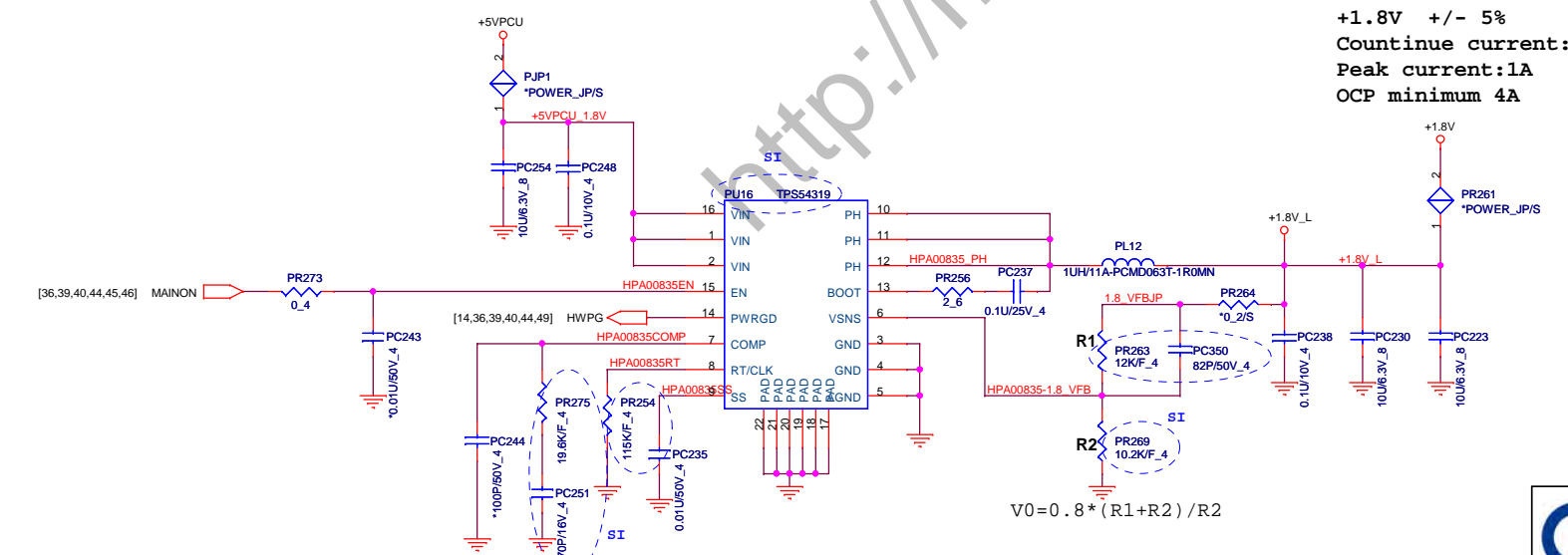
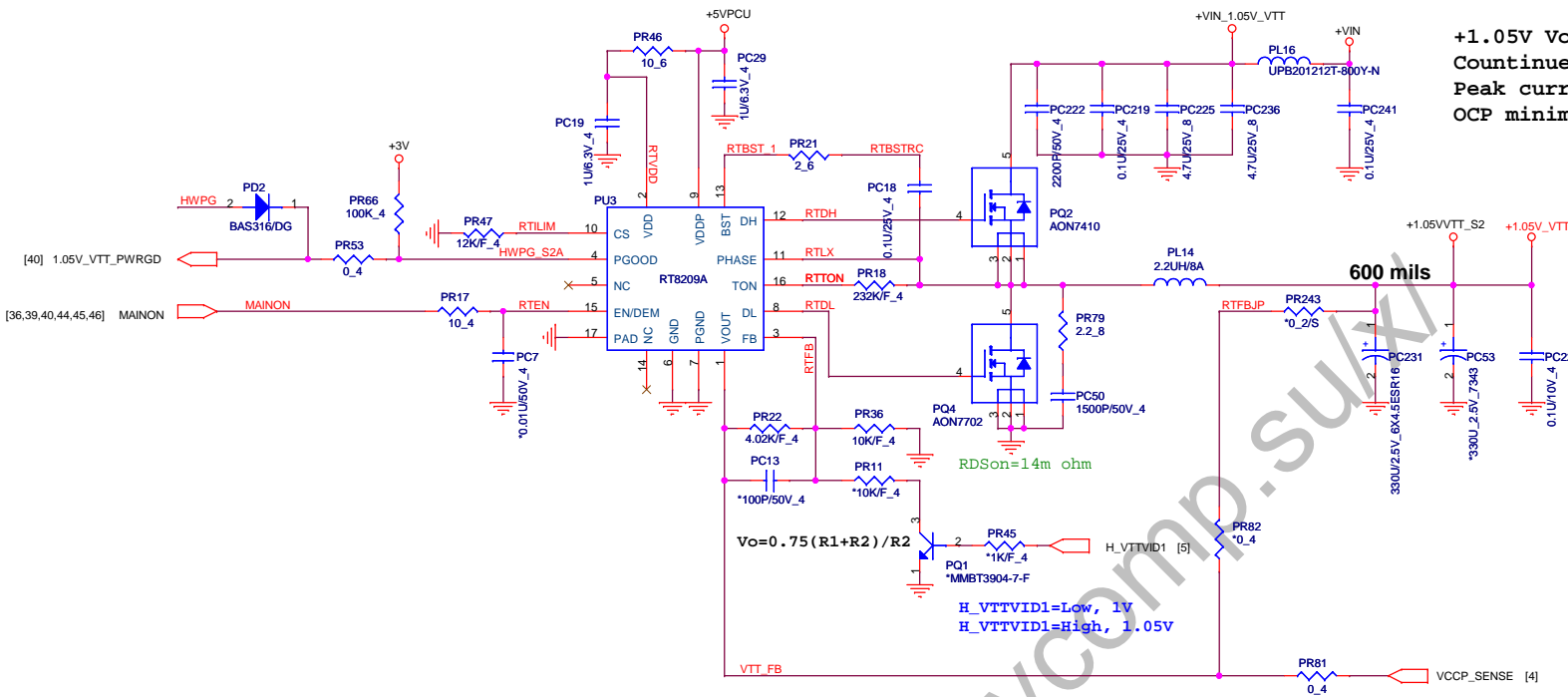
+VCCSA +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum 8A


+1.05 Volt +/- 0.1V
Countinue current:0.7A
Peak current:2A

+1.05V Volt +/- 5%
Countinue current:4A
Peak current: 6A
OCP minimum: 8A

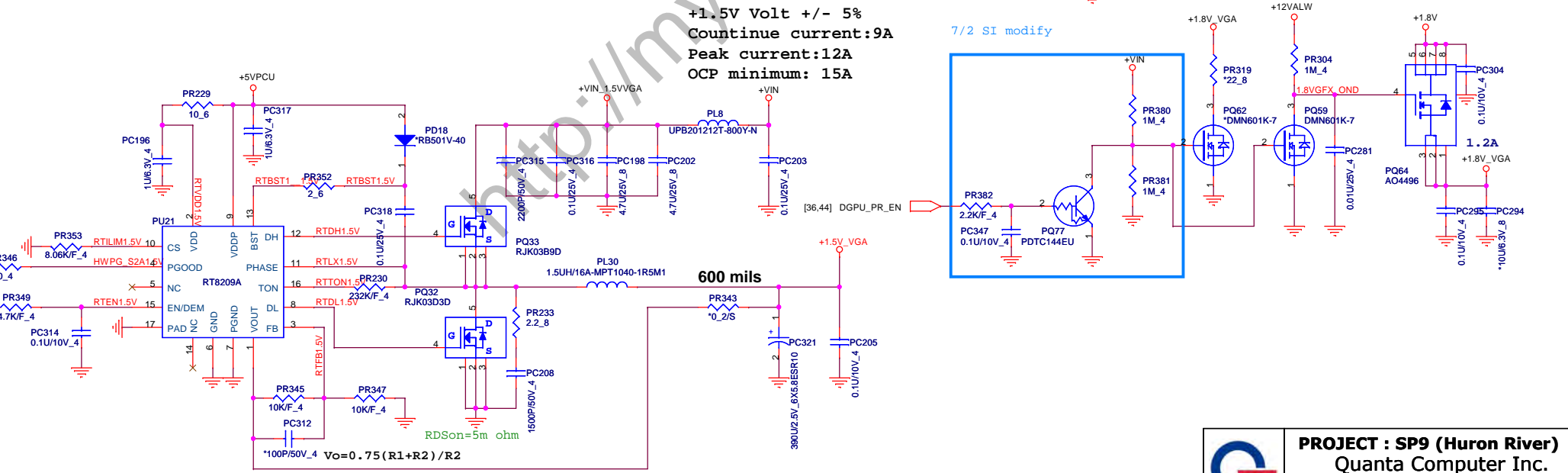
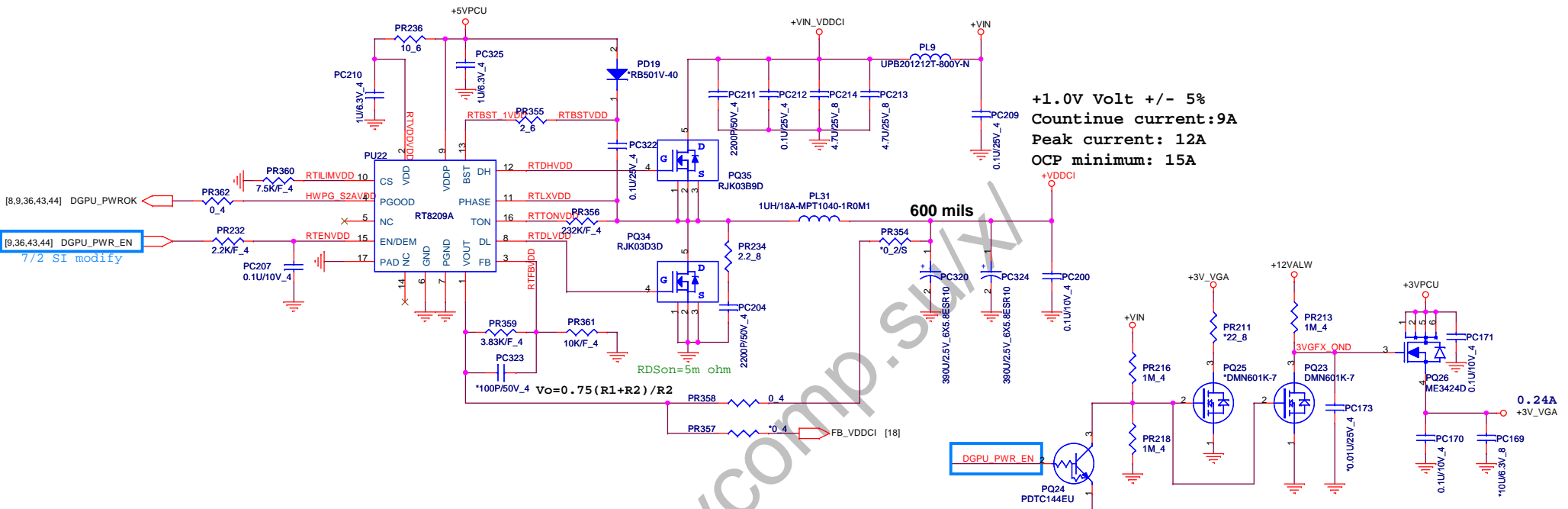
$V_O = (0.8(R1+R2) / R2)$
 $R2 < 120Kohm$

<p>NB5/RD2</p>	<p>PROJECT : SP9 (Huron River) Quanta Computer Inc.</p>		
	<p>Size Custom</p>	<p>Document Number +1.05V_VTT (VT358)</p>	<p>Rev 1A</p>
	<p>Date: Tuesday, August 10, 2010</p>		<p>Sheet 40 of 46</p>

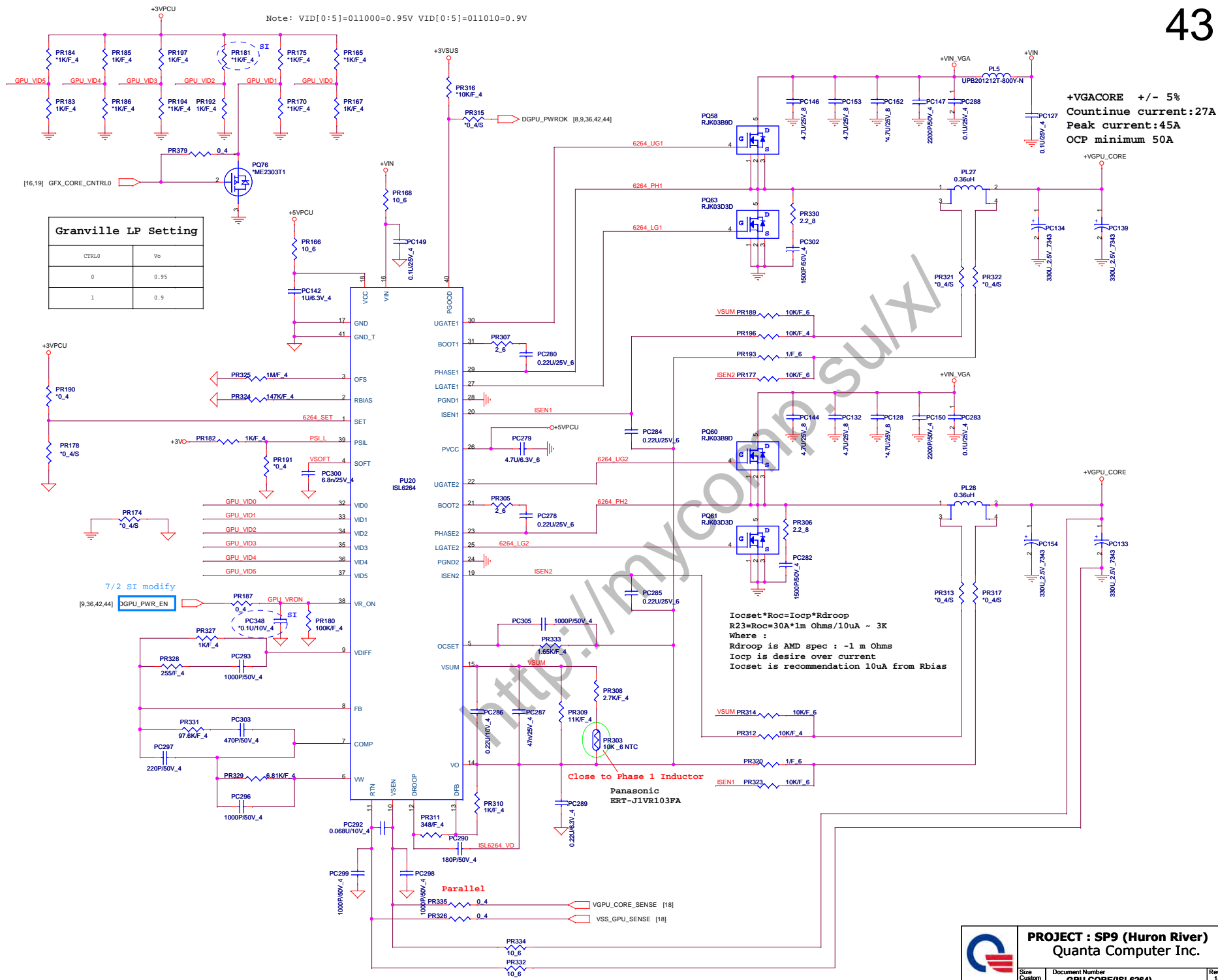


 NB5/RD2	PROJECT : SP9 (Huron River) Quanta Computer Inc.		Rev 1A
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http://mycomp.su.kz



Note: VID[0:5]=011000=0.95V VID[0:5]=011010=0.9V



Granville LP Setting

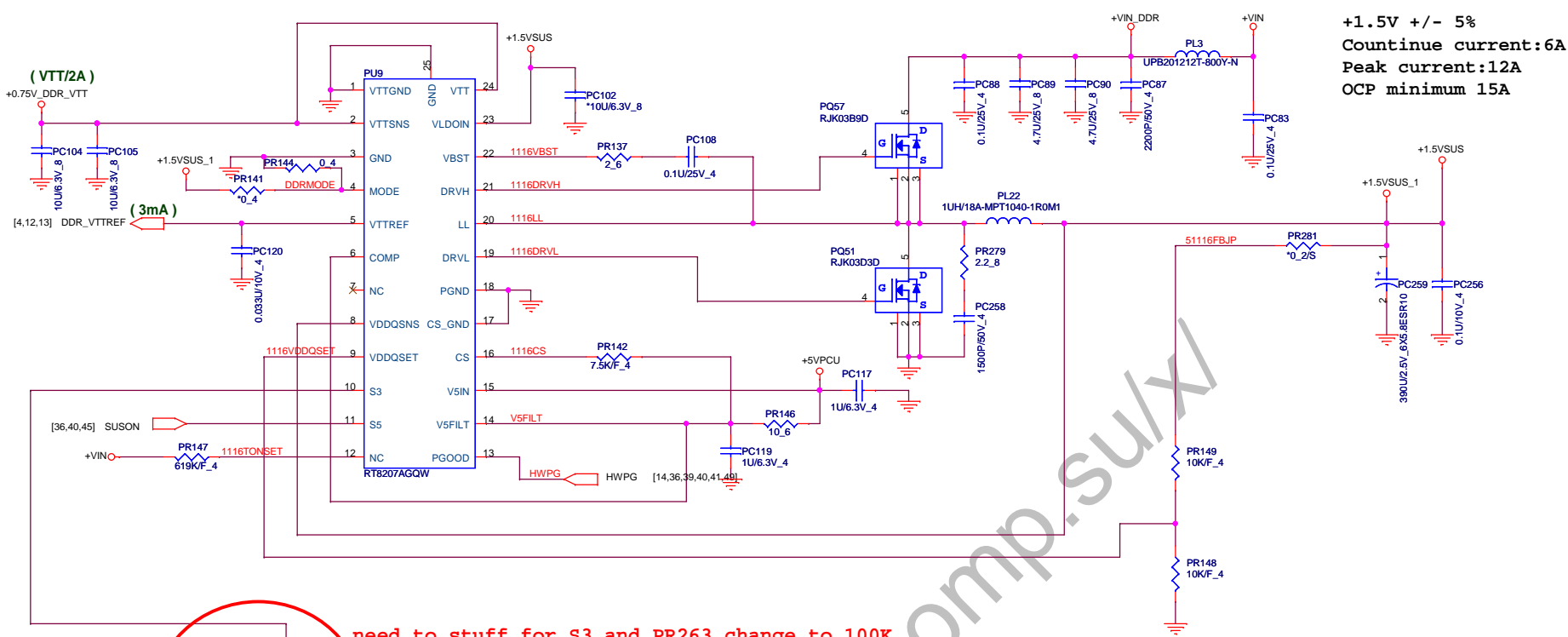
CTRL0	V0
0	0.95
1	0.9

$Iocset * R_{oc} = Iocp * R_{droop}$
 $R23 = R_{oc} = 30A * 1m \text{ Ohms} / 10uA \sim 3K$
 Where :
 R_{droop} is AMD spec : -1 m Ohms
 $Iocp$ is desire over current
 $Iocset$ is recommendation 10uA from Rbias

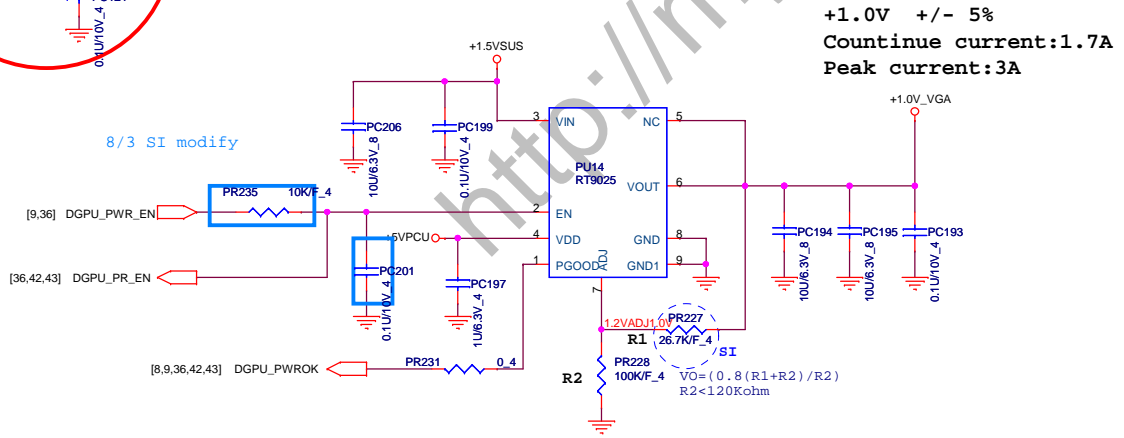
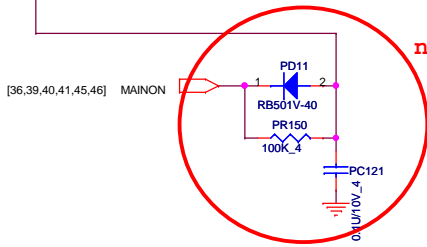
Close to Phase 1 Inductor
 Panasonic
 ERT-J1VR103FA

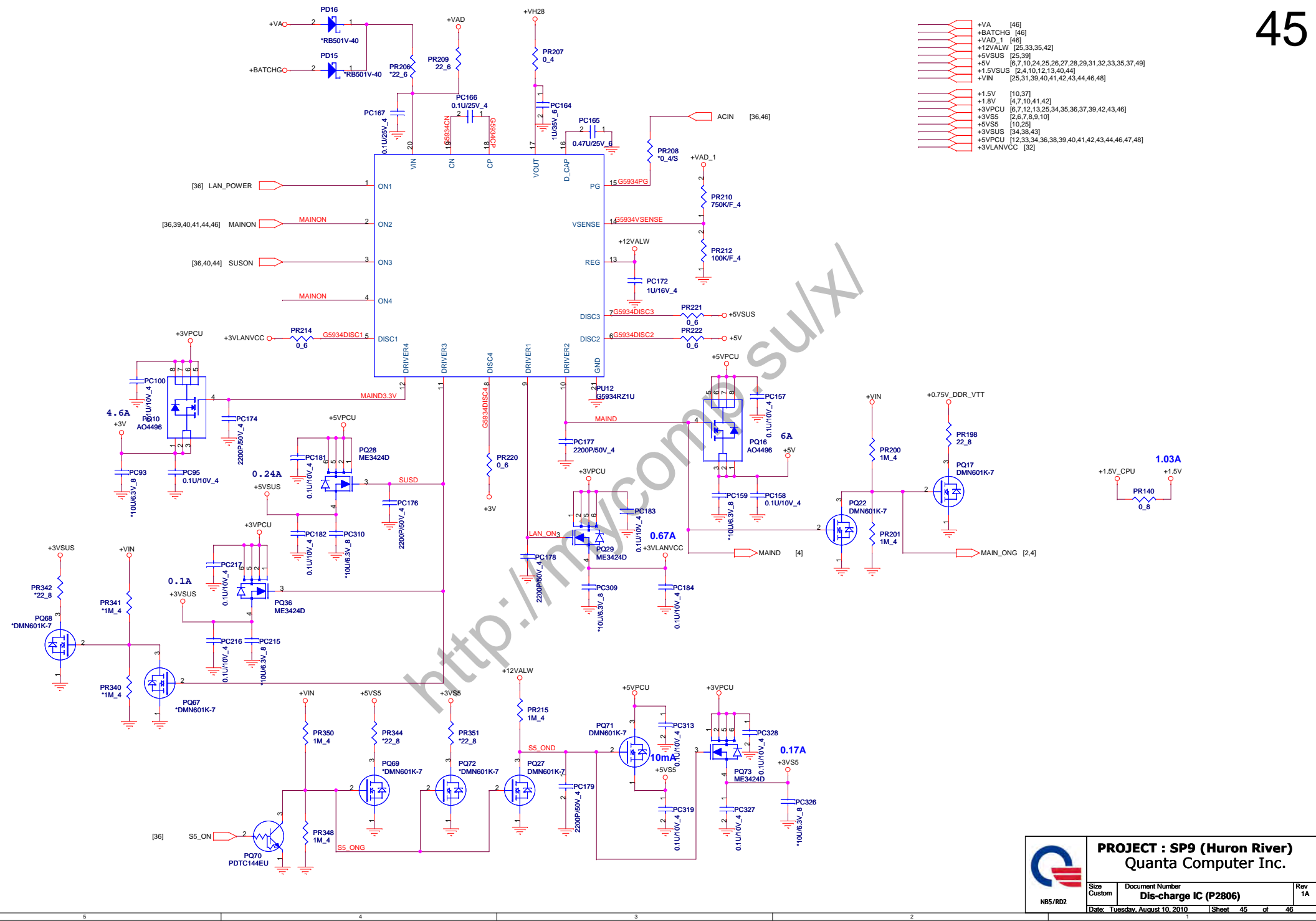
+VGACORE +/- 5%
Countinue current:27A
Peak current:45A
OCP minimum 50A

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need to stuff for S3 and PR263 change to 100K



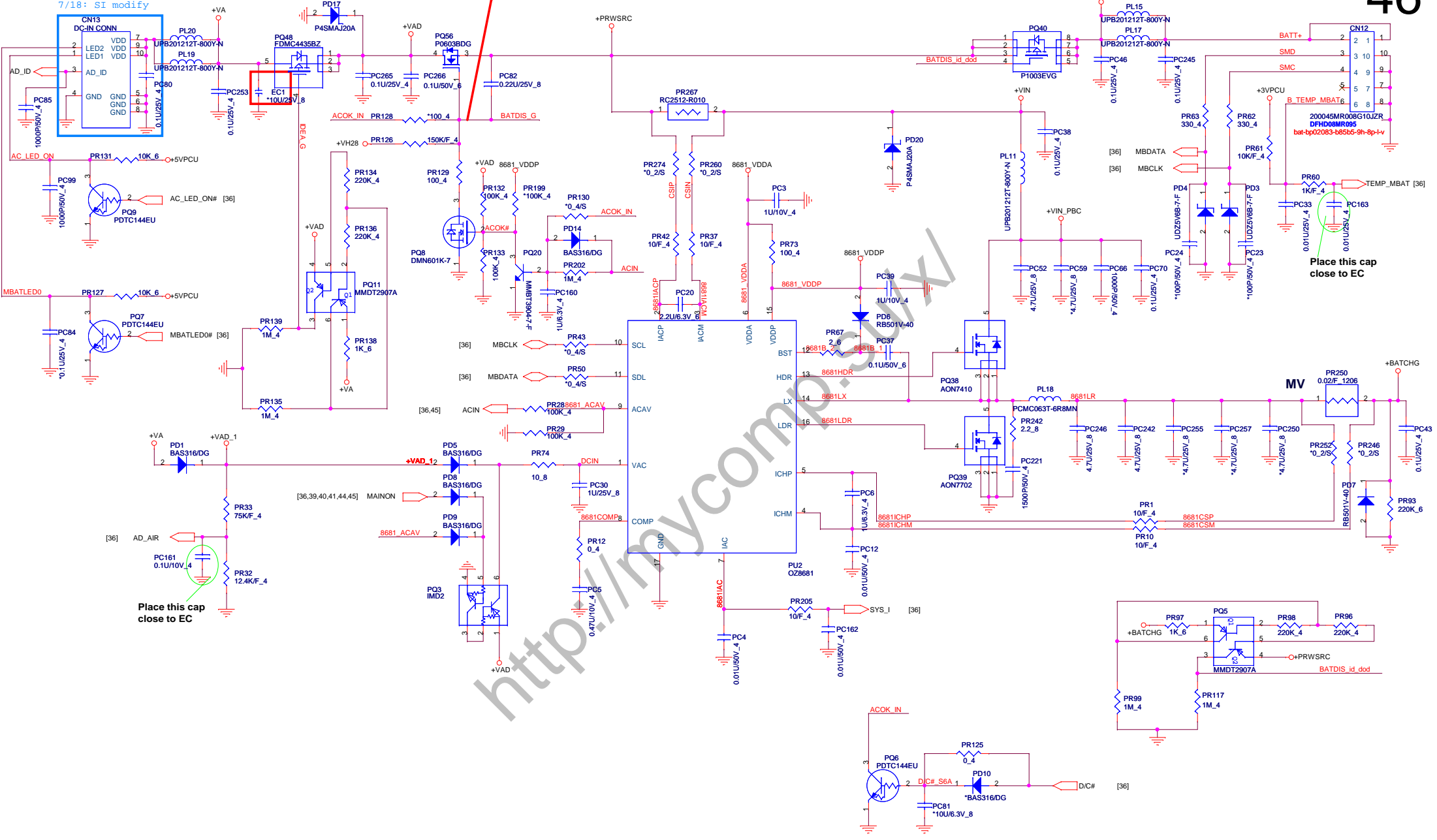


- +VA [46]
- +BATCHG [46]
- +VAD_1 [46]
- +12VALW [25,33,35,42]
- +5VSUS [25,39]
- +5V [6,7,10,24,25,26,27,28,29,31,32,33,35,37,49]
- +1.5VSUS [2,4,10,12,13,40,44]
- +VIN [25,31,39,40,41,42,43,44,46,48]
- +1.5V [10,37]
- +1.8V [4,7,10,41,42]
- +3VPCU [6,7,12,13,25,34,35,36,37,39,42,43,46]
- +3VSS [2,6,7,8,9,10]
- +5VSS [10,25]
- +3VSS [34,38,43]
- +5VPCU [12,33,34,36,38,39,40,41,42,43,44,46,47,48]
- +3VLNVCC [32]


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			Quanta Computer Inc.	
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TOP DC_JACK
65W/90W

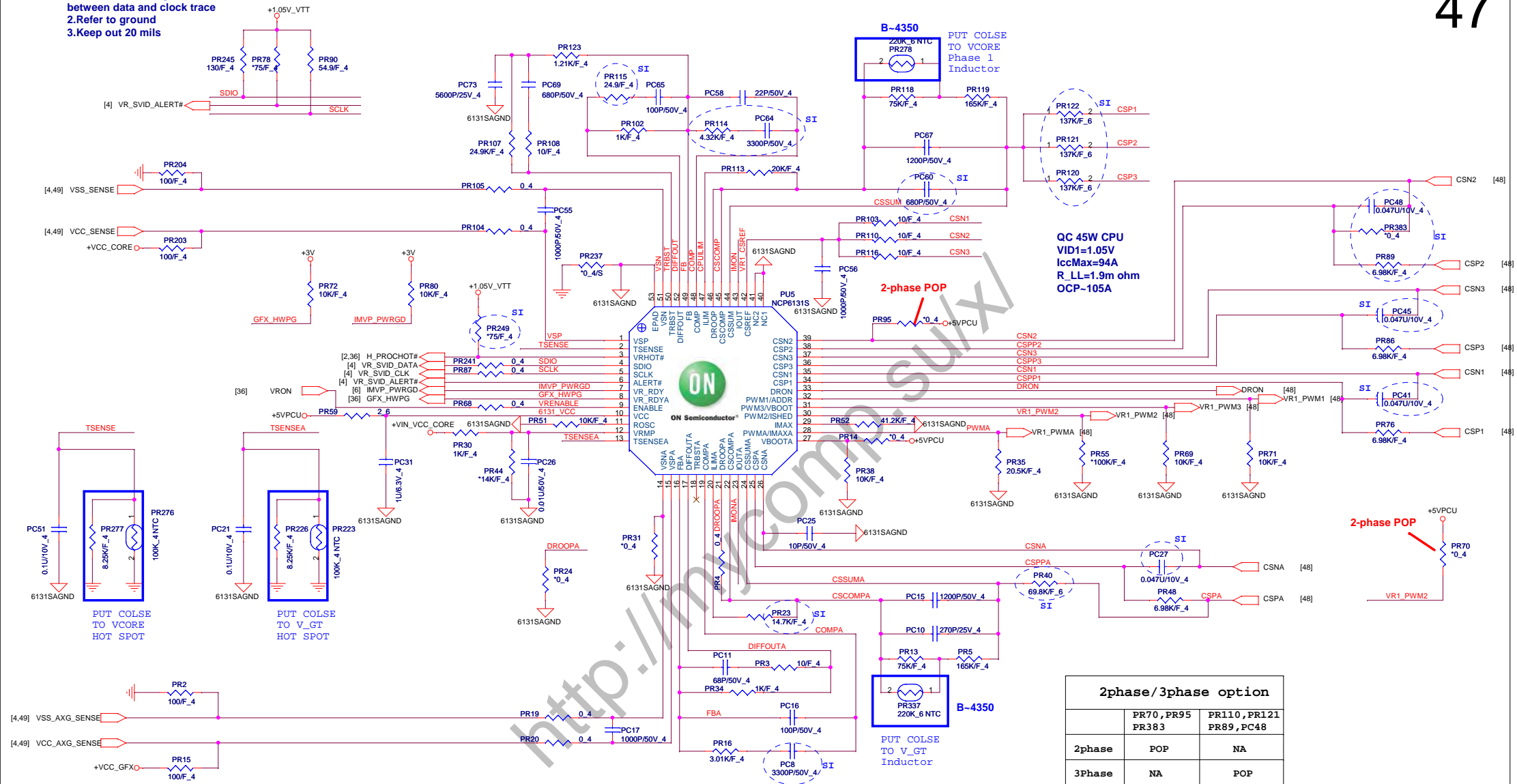
For EMI test only no stuff
Do Not add test pad on BATDIS_G signal



- +VA [45]
- +VAD_1 [45]
- +VH28 [45]
- +BATCHG [45]
- +5VPCU [12,33,34,36,38,39,40,41,42,43,44,45,47,48]

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Size	Document Number	Rev			
Custom	Charger (BQ24704)	1A			
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- 1.Alert trace routing between data and clock trace
- 2.Refer to ground
- 3.Keep out 20 mils



2phase/3phase option

	PR70, PR95 PR383	PR110, PR121 PR89, PC48
2phase	POP	NA
3Phase	NA	POP

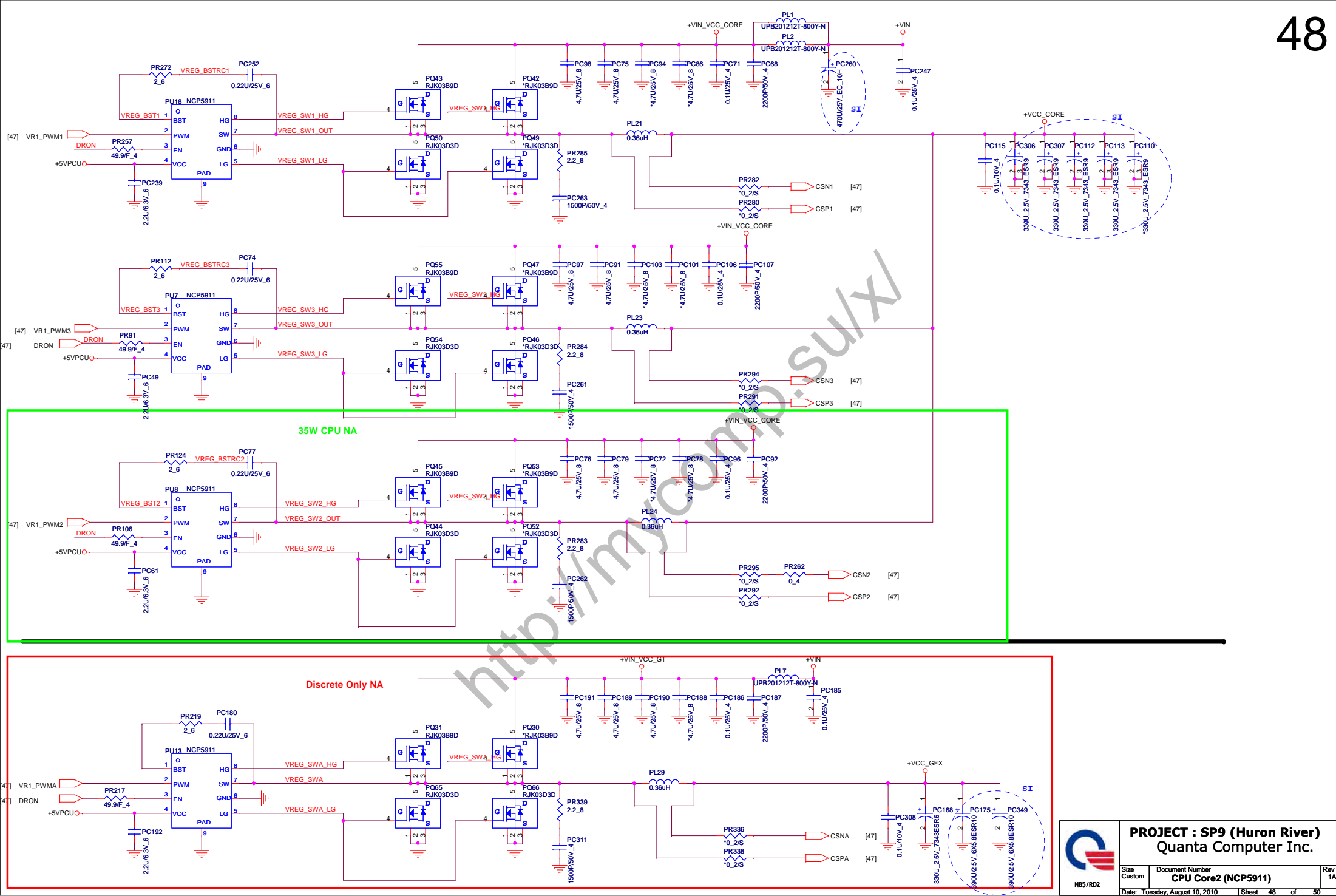
UMA(Switchable)/Discrete Only option


UMA	POP	POP	NA
PC336, PC340 PC343, PC337 PC342	PR427, PR433, PR430, PR431, PR423, PR435 PC338, PR424, PR428, PR432, PC339, PC341 PR425, PR426, PR429, PR420, PR422, PR380 PR399, PR421, PC352, PR417, PR418, PC354 PC419	PR434, PR436 PR378	NA
Discrete	Change to 0 ohm	NA	POP

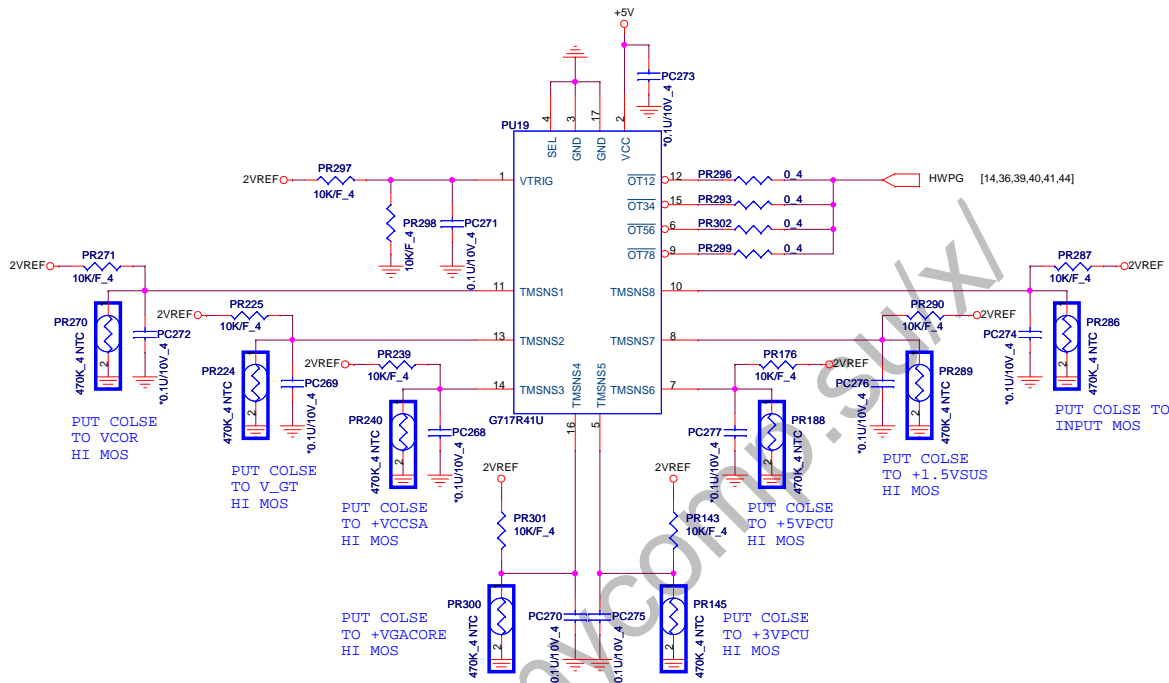
PROJECT : SP9 (Huron River)
Quanta Computer Inc.

Size: Custom Document Number: CPU Core1 (NCP6131S) Rev: 1A


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			PROJECT : SP9 (Huron River)	
			Quanta Computer Inc.	
Size Custom	Document Number CPU Core2 (NCP5911)	Rev 1A		
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Vender	Size	P/N
EON	128KB	AKE37ZN0Q01 (EN25F40-100HIP)
Winbond	128KB	AKE35FN0N00 (W25X10BVSNIG)
	512KB	AKE37FN0N01 (W25X40BVSSIG)
Socket		DG008000031

 NB5/RD2	PROJECT : SP9 (Huron River)		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number IMON	
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