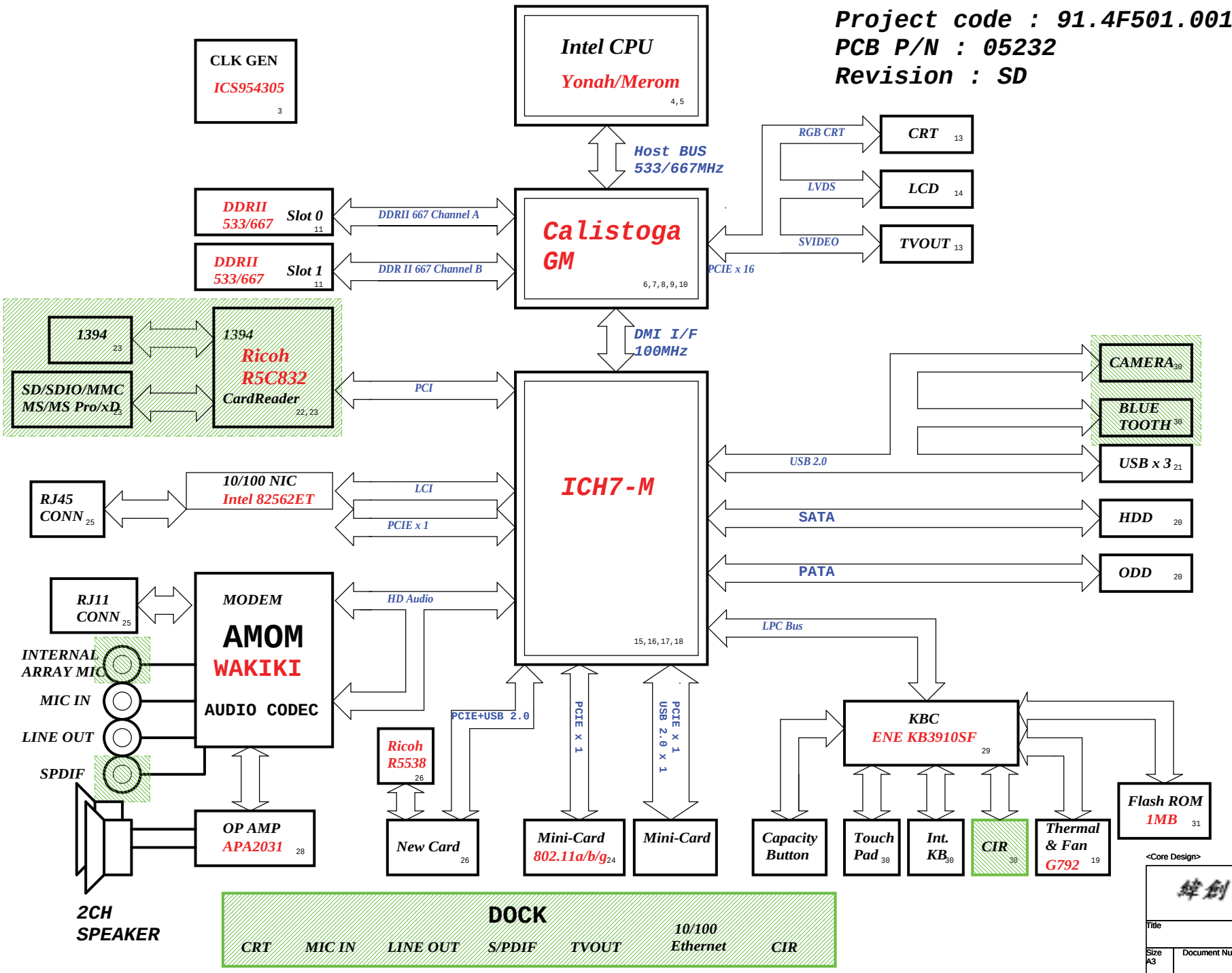
Akita Block Diagram

Project code : 91.4F501.001
PCB P/N : 05232
Revision : SD



SYSTEM DC/DC TPS51120	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3V_S5

SYSTEM DC/DC MAX8743	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3

MAXIM CHARGER MAX8725	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA

CPU DC/DC MAX8736ETL	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 44A

PCB LAYER

L1: Signal 1
L2: GND
L3: Signal 2
L4: Signal 3
L5: VCC
L6: Signal 4

<Core Design>

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Title: Block Diagram
Size: A3 | Document Number: Akita | Rev: SD
Date: Monday, February 06, 2006 | Sheet 1 of 39

Calistoga Strapping Signals and Configuration

page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4 (Default)**
CFG6		0=Moby Dick 1=Calistoga
CFG7	CPU Strap	0 = Reserved **1 =Mobile CPU(Default)**
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG[11:10]	Reserved	
CFG[13:12]	Reserved	
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG17	Global R-comp Disable (All R-comps)	0 = All R-comp Disable **1 = Normal Operation (Default)**
CFG18	VCC Select	**0 = 1.05V** (Default) 1 = 1.5V
CFG19	DMI Lane Reversal	**0 = Normal operation (Default):lane Numbered in order** 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	**0 = Only SDVO or PCIE x1 is operational (Default)** 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL_DATA	SDVO Present	**0 = No SDVO device present** (Default) 1= SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK In signal.

125CV Spread Spectrum Select

page 3

SS3	SS2	SS1	SS0	Spread Amount%
0	0	0	0	-0.8
0	0	0	1	-1.0
0	0	1	0	-1.25
0	0	1	1	-1.5
0	1	0	0	-1.75
0	1	0	1	-2.0
0	1	1	0	-2.5
0	1	1	1	-3.0
1	0	0	0	+-0.3
1	0	0	1	+-0.4
1	0	1	0	+-0.5
1	0	1	1	+-0.6
1	1	0	0	+-0.8
1	1	0	1	+-1.0
1	1	1	0	+-1.25
1	1	1	1	+-1.5

PCI Routing

	IDSEL	IRQ	REQ/GNT
R5C832	25		0

ICH7M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR, EE_CS,	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

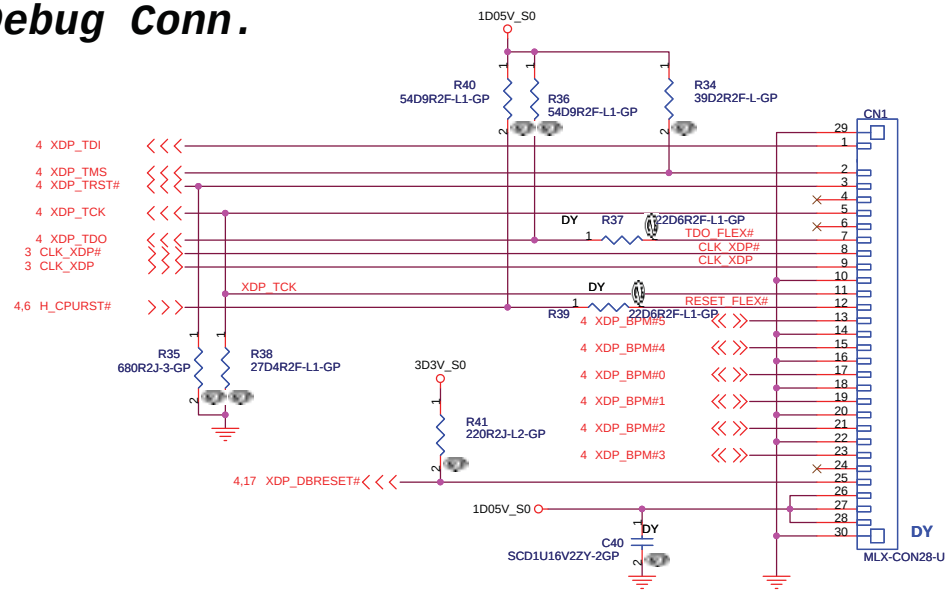
ICH7M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

History

11.18.2004: mini card not ready

ITP Debug Conn.



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Title	ITP	
Size A3	Document Number: Akita	Rev SD
Date: Friday, March 31, 2006	Sheet 2 of 39	

H/L : CPU_ITP/SRC10

IN (3D3V_S0)	EN (6218_PGOOD)	OUT (VTT_PWRGD#)
H	L	H
X	H	Hi - Z

H/L: 100/96MHz

UMA ONLY

FS_C	FS_B	FS_A	CPU
0	0	0	266M
0	0	1	133M
0	1	0	200M
0	1	1	166M
1	0	0	333M
1	0	1	100M
1	1	0	400M
1	1	1	Reserved

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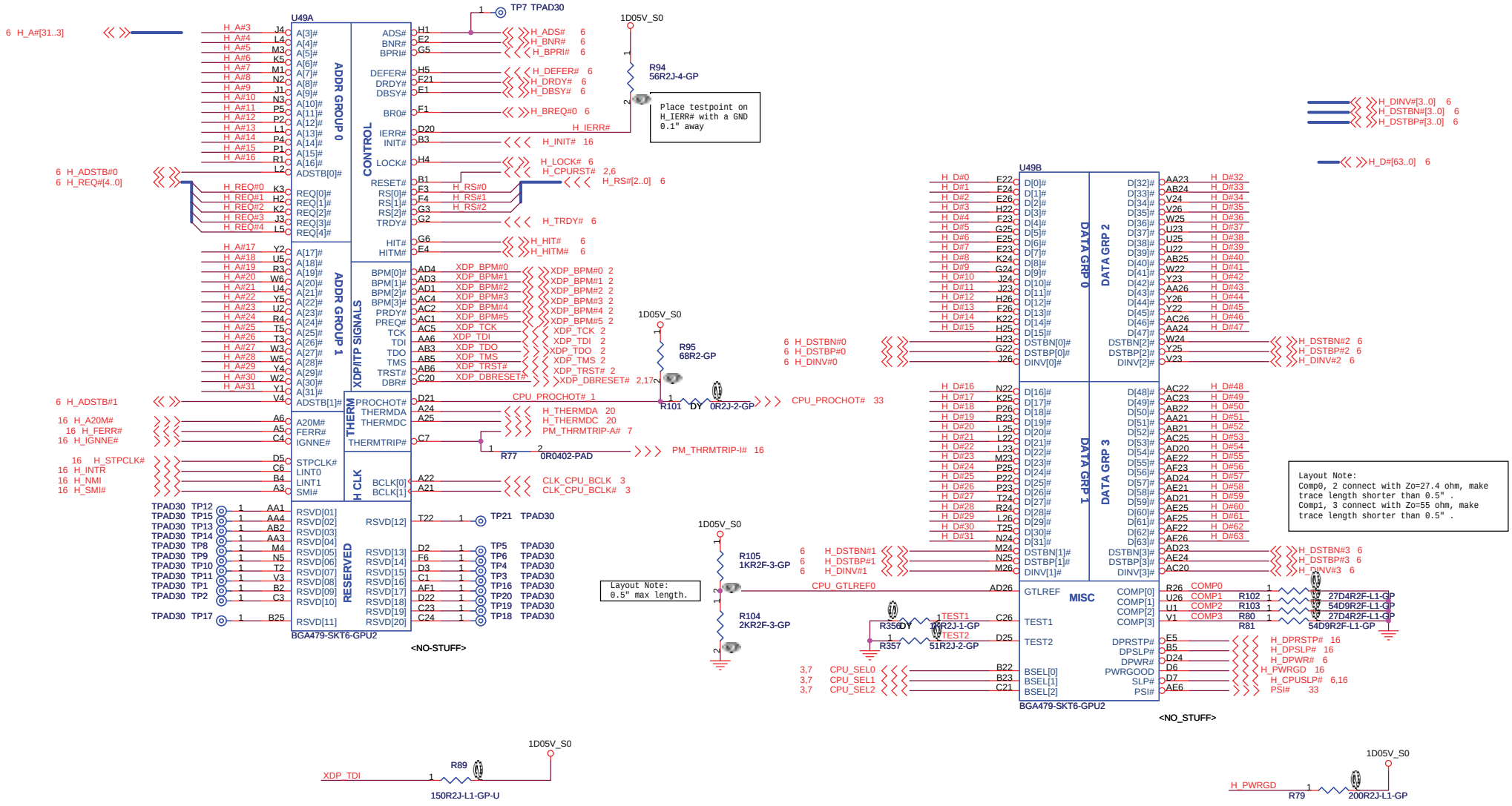
Title: Clock Generator (IDTCV125PA)

Size: A3 | Document Number: Akita | Rev: SD

Date: Friday, March 31, 2006 | Sheet 3 of 39



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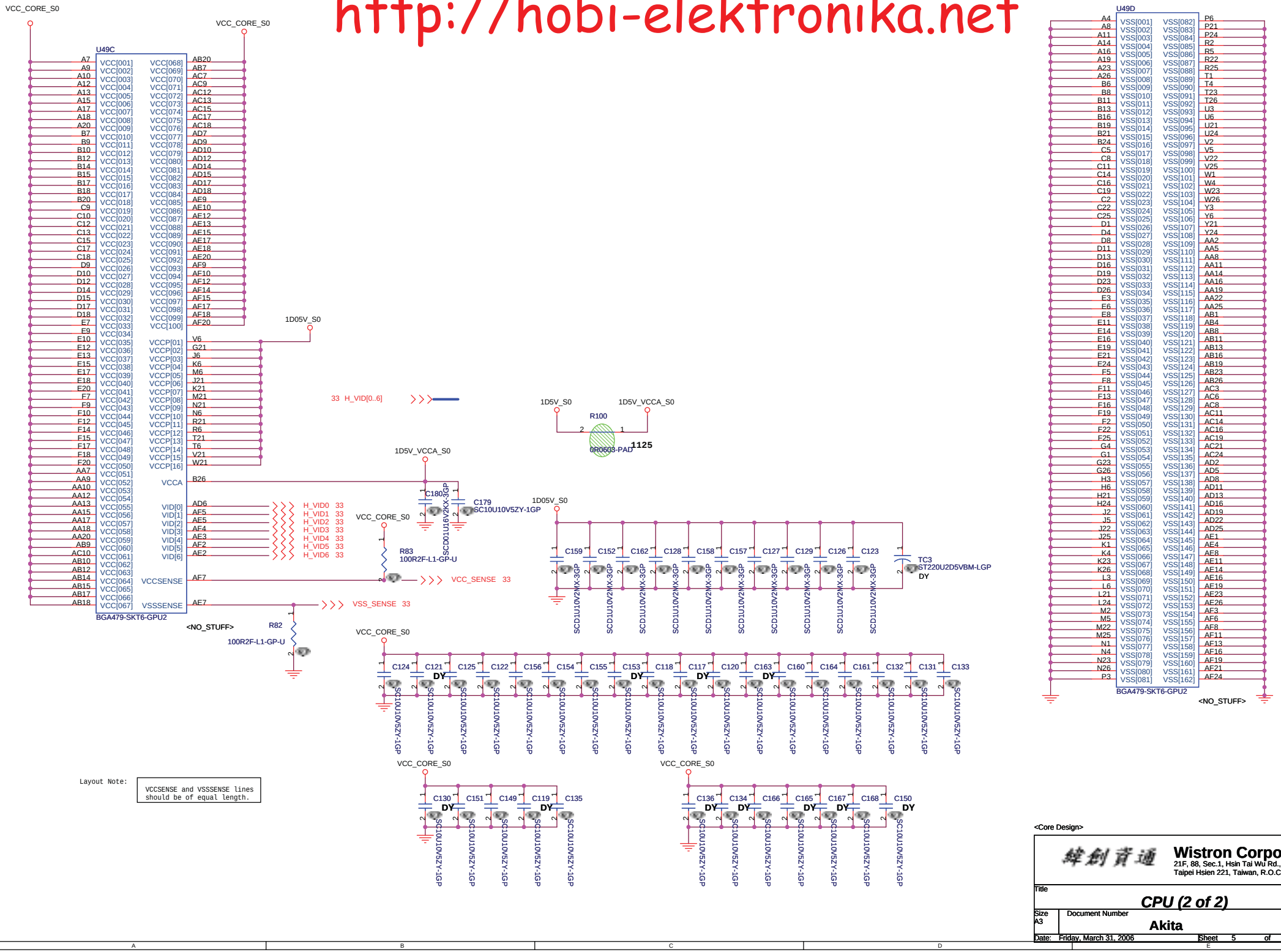
Title: **CPU (1 of 2)**

Size	Document Number	Rev
A3	Akita	SD

Date: Friday, March 31, 2006 Sheet 4 of 39



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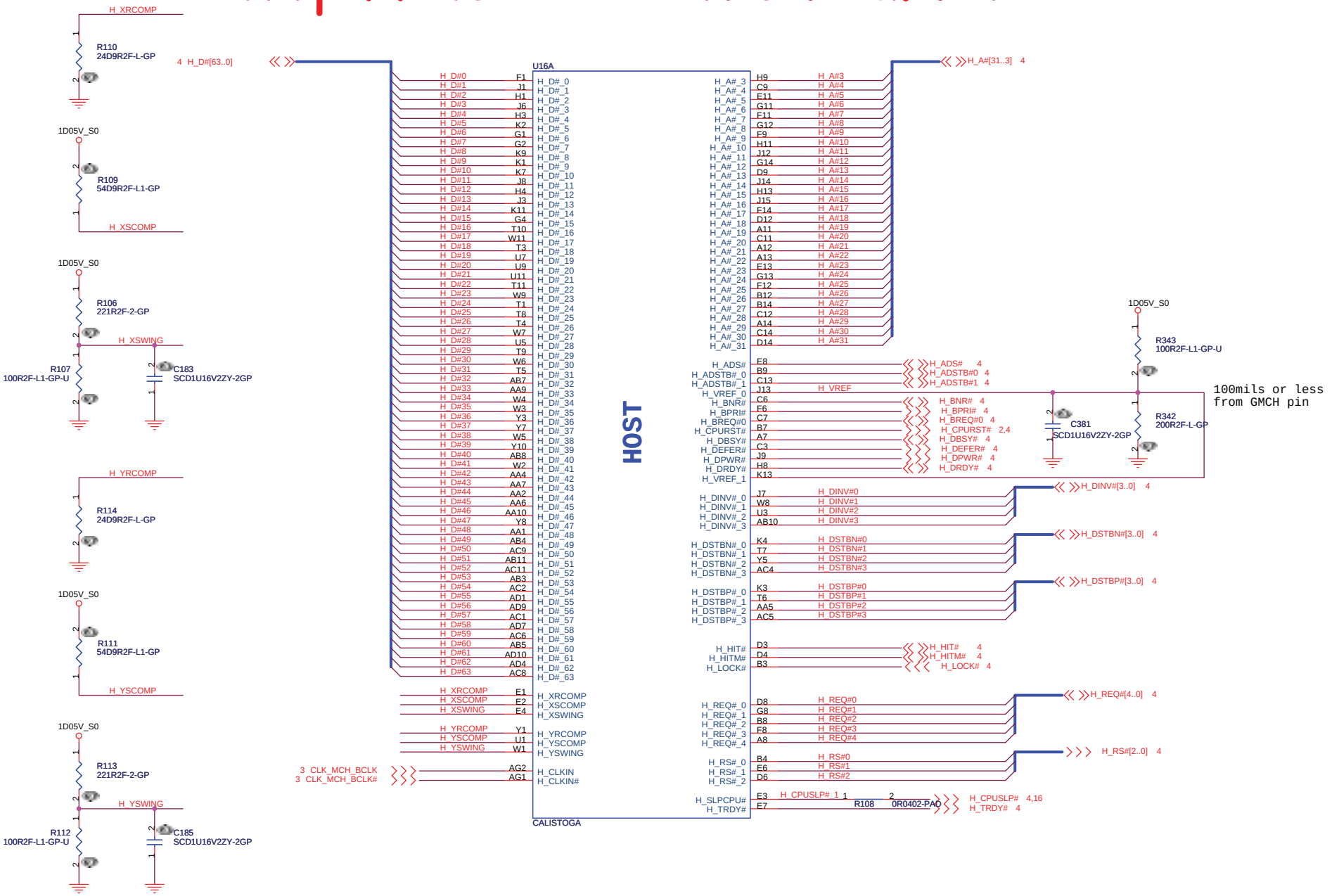
Title: **CPU (2 of 2)**

Size	Document Number	Rev
A3	Akita	SD

Date: Friday, March 31, 2006 Sheet 5 of 39



Place them near to the chip

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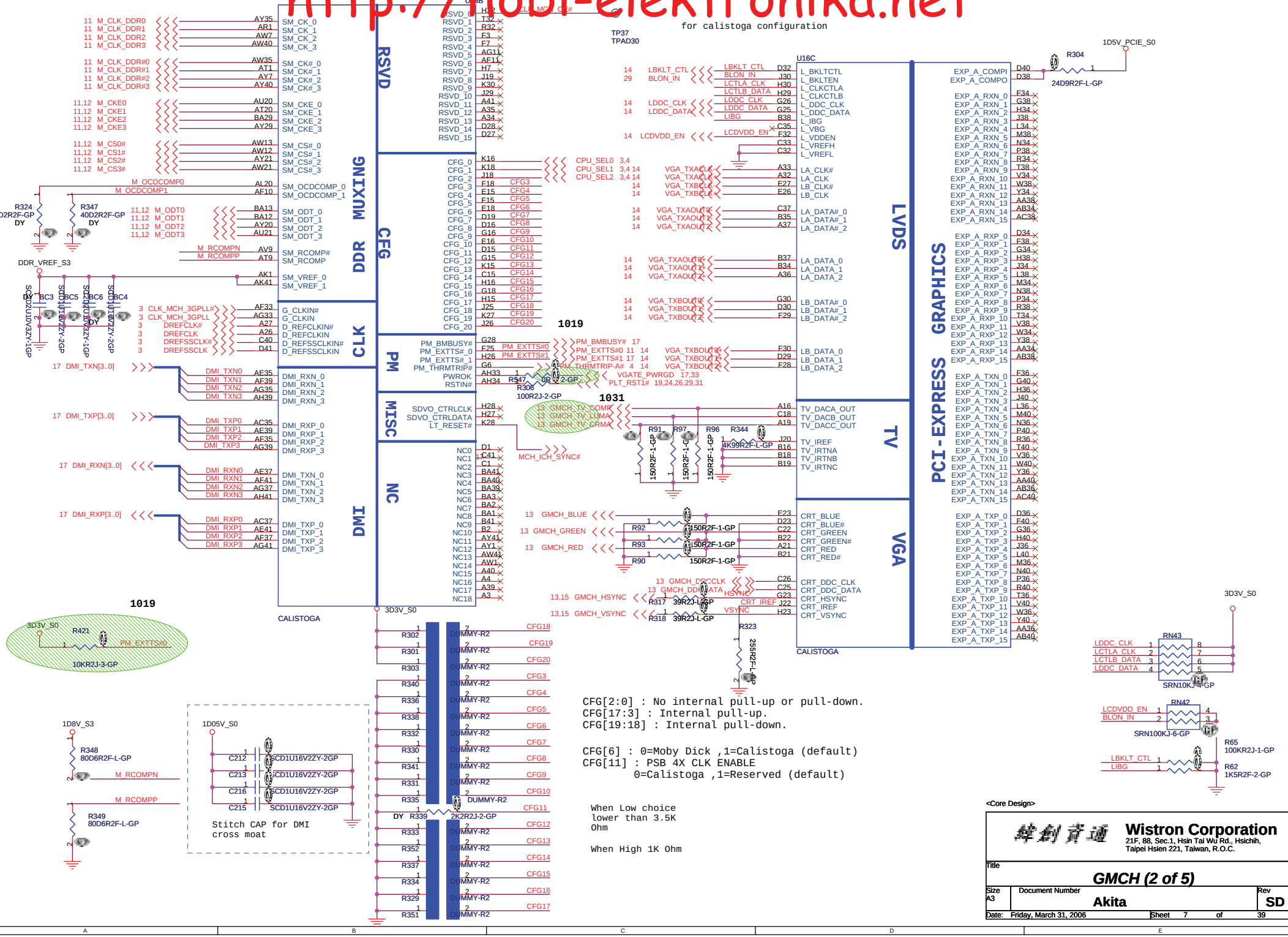
Title: **GMCH (1 of 5)**

Size	Document Number	Rev
A3	Akita	SD

Date: Monday, February 06, 2006 Sheet 6 of 39

for calistoga configuration




```
CFG[2:0] : No internal pull-up or pull-down.
CFG[17:3] : Internal pull-up.
CFG[19:18] : Internal pull-down.

CFG[6] : 0=Moby Dick ,1=Calistoga (default)
CFG[11] : PSB 4X CLK ENABLE
      0=Calistoga ,1=Reserved (default)


 When Low choice
 lower than 3.5K
 Ohm

 When High 1K Ohm
```

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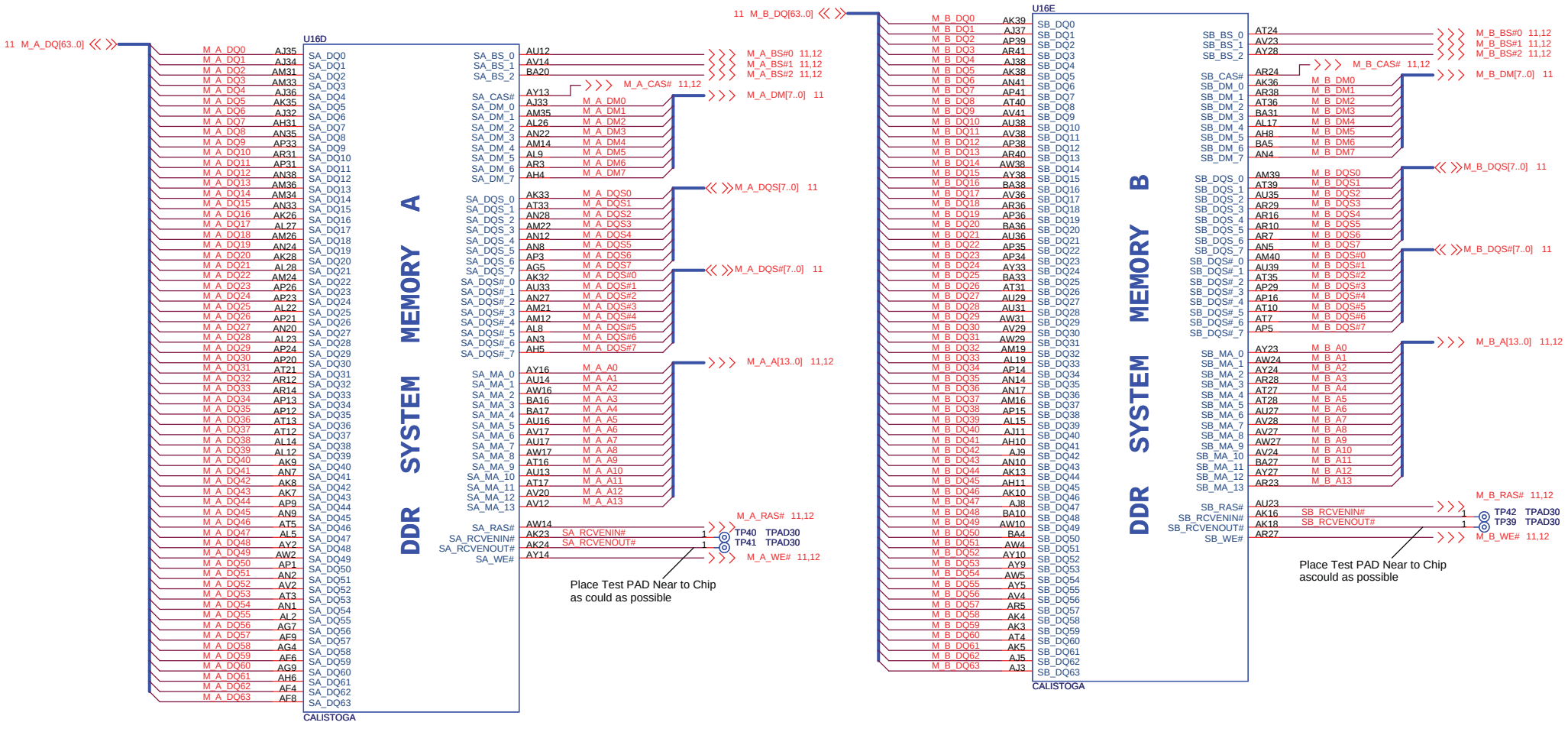
Title: **GMCH (2 of 5)**

Size	Document Number	Rev
A3	Akita	SD

Date: Friday, March 31, 2006 Sheet 7 of 39



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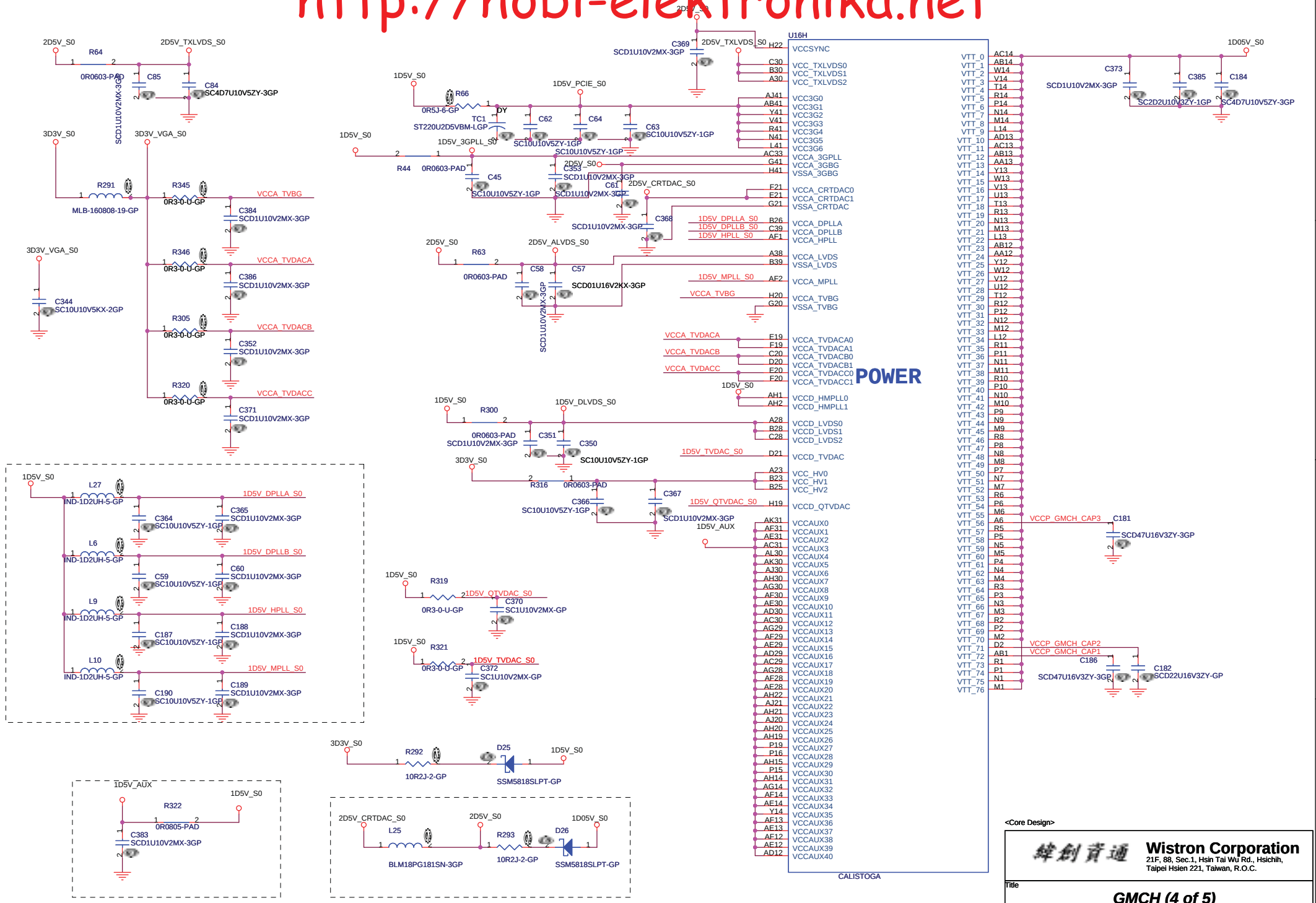
Title: GMCH (3 of 5)

Size: A3 | Document Number: Akita | Rev: SD

Date: Monday, February 06, 2006 | Sheet 8 of 39



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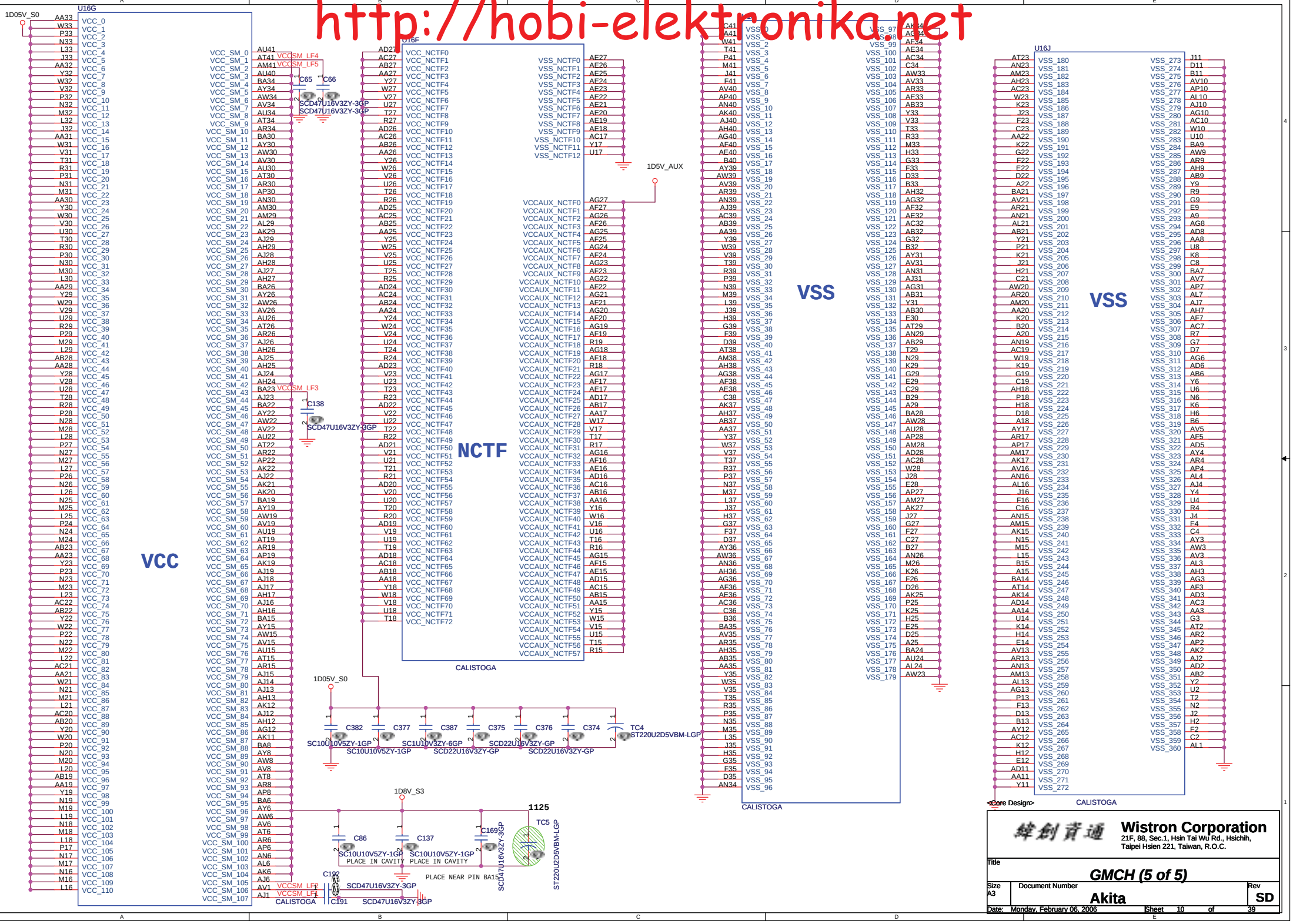
Title: **GMCH (4 of 5)**

Size	Document Number	Rev
A3	Akita	SD

Date: Friday, March 31, 2006 Sheet 9 of 39



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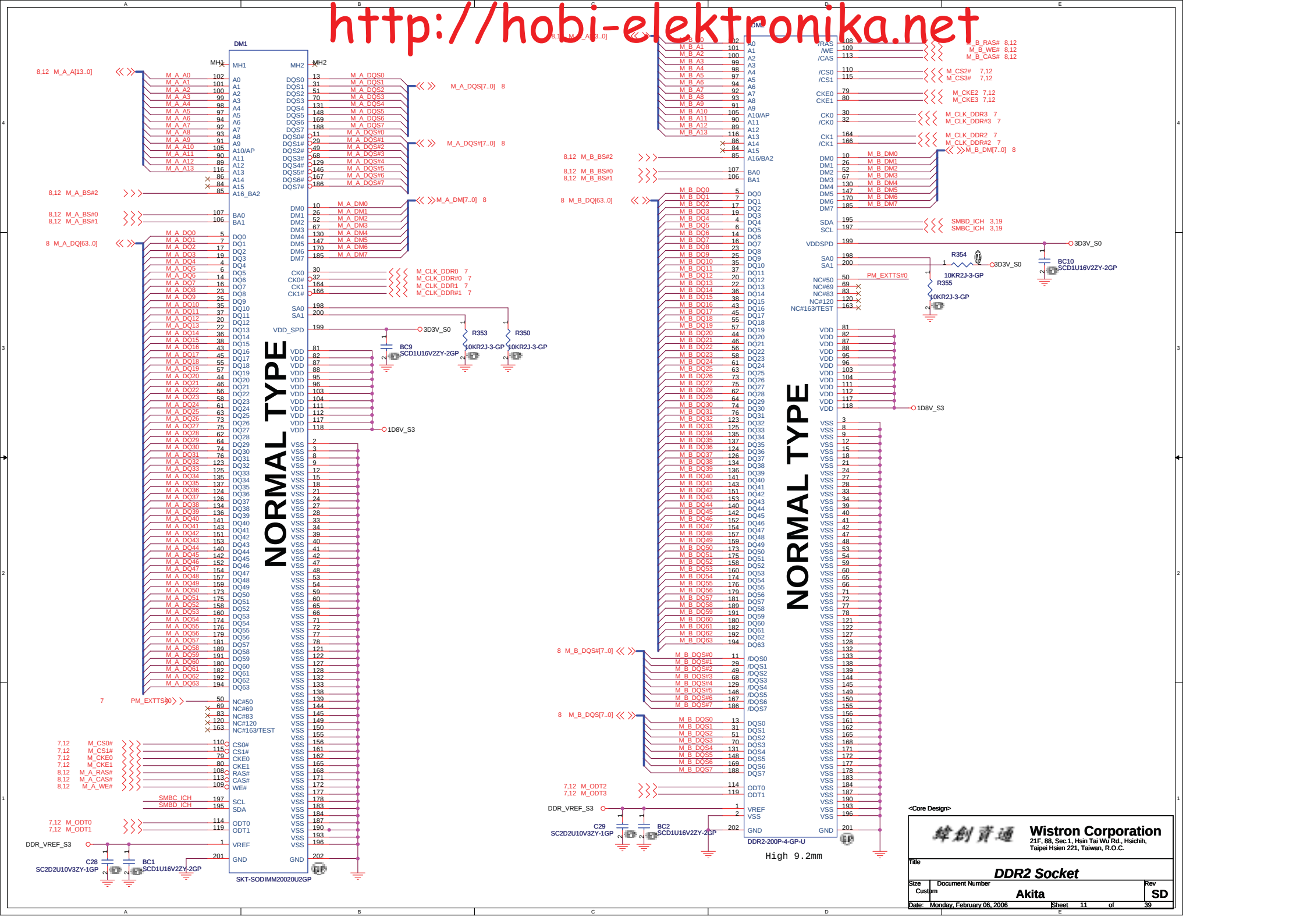
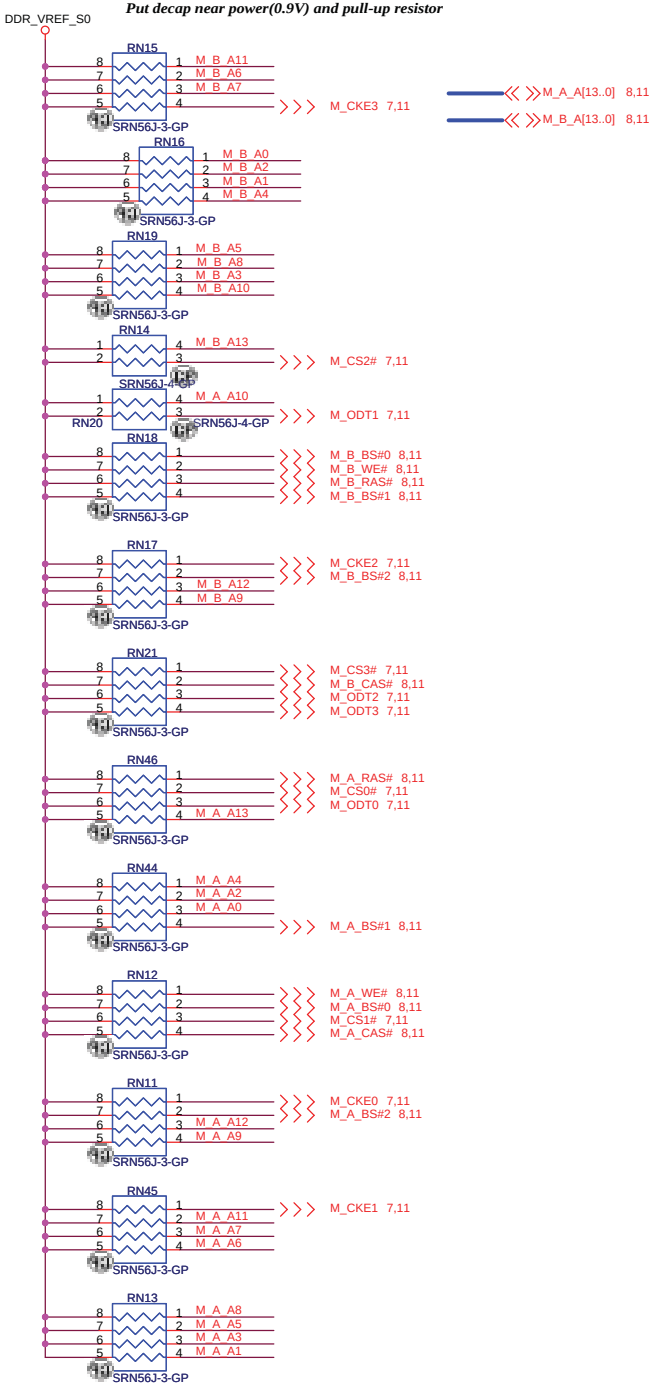
Title	GMCH (5 of 5)
Size A3	Document Number: Akita
Rev	SD
Date: Monday, February 06, 2006	Sheet 10 of 39



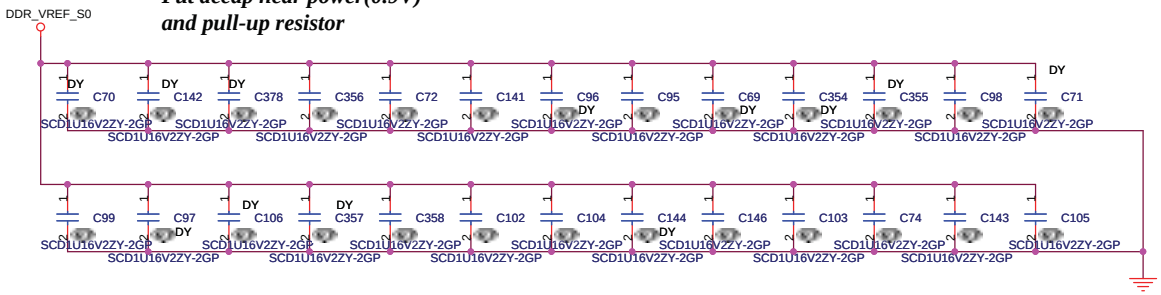
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

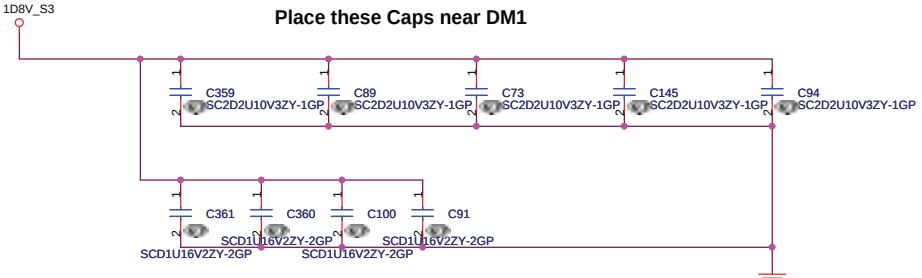


Decoupling Capacitor

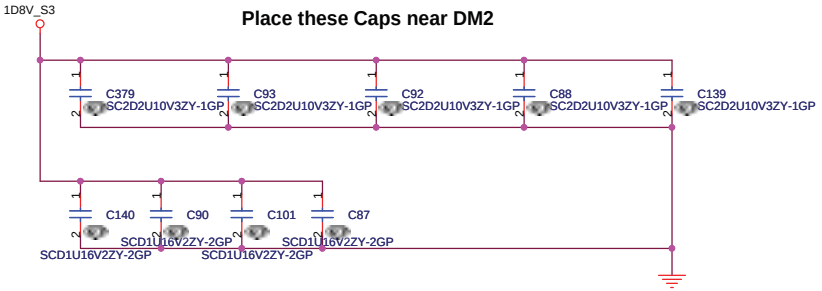
Put decap near power(0.9V) and pull-up resistor



Place these Caps near DM1



Place these Caps near DM2



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Title: DDR2 Termination Resistor

Size: A3 | Document Number: Akita | Rev: SD

Date: Friday, March 31, 2006 | Sheet 12 of 39

CRT I/F & CONNECTOR

Layout Note:
Place these resistors close to the CRT-out connector

1122

7 GMCH_RED — L2 BLM18BB470SN1-GP — CRT_R — CRT_R 15
7 GMCH_GREEN — L3 BLM18BB470SN1-GP — CRT_G — CRT_G 15
7 GMCH_BLUE — L1 BLM18BB470SN1-GP — CRT_B — CRT_B 15

R5 150R2F-1-GP, R4 150R2F-1-GP, R3 150R2F-1-GP
C14 SC22P50V2JN-4GP, C15 SC22P50V2JN-4GP, C11 SC22P50V2JN-4GP
C12 SC2P50V2CN-GP, C13 SC2P50V2CN-GP, C9 SC2P50V2CN-GP

Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift

5V_S0 — C10 SCD01U16V2KX-3GP — F1 FUSE-1D1A6V-8GP — D3 CH751H-40PT-1GP — 5V_CRT1_S0

1124

RN1 SRN2K2J-1-GP

CRT1 VIDEO-15-57-GP-U
CRT_R, CRT_G, CRT_B
DDC_DATA_CON, JVGA_HS, JVGA_VS, DDC_CLK_CON
C7 SC33P50V2JN-3GP DY, C6 SC33P50V2JN-3GP DY, C8 SC22P50V2JN-4GP, C1 SC22P50V2JN-4GP

D10 BAV99-7-F-GP DY, D9 BAV99-7-F-GP DY
DDC_DATA_CON, DDC_CLK_CON

5V_CRT1_S0 — 1124

U2 PACDN009MR-GP-U DY
GMCH_HSYNC, GMCH_VSYNC, CRT_R → CRT_G, CRT_B

5V_S0 — C21 SCD1U16V2ZY-2GP

7,15 GMCH_HSYNC — U5A TSAHCT125PW-GP — HSYNC_5 — PR_INSERT 15
7,15 GMCH_VSYNC — U5B TSAHCT125PW-GP — VSYNC_5

RN4 SRN33J-5-GP-U — JVGA_HS, JVGA_VS

3D3V_S0 — RN2 SRN2K2J-1-GP

U1 2N7002DW-7F-GP
7 GMCH_DDCDATA — DDC_DATA_CON — DDC_DATA_CON 15
15 DDC_CLK_CON — DDC_CLK_CON — GMCH_DDCCLK 7

RN6 DY SRN0J-6-GP

5V @ ext. CRT side

TV OUT CONN

connector

7 GMCH_TV_CRMA — L18 BLM18BB151SN-1GP — TV_CRMA 15
R272 150R2F-1-GP, C328 SC10P50V2JN-4GP, C324 SC10P50V2JN-4GP

7 GMCH_TV_COMP — L20 BLM18BB151SN-1GP — TV_COMP 15
R271 150R2F-1-GP, C326 SC10P50V2JN-4GP, C327 SC10P50V2JN-4GP

7 GMCH_TV_LUMA — L19 BLM18BB151SN-1GP — TV_LUMA 15
R270 150R2F-1-GP, C329 SC10P50V2JN-4GP, C325 SC10P50V2JN-4GP

Place this 2 resistors close to the TV-out connector

TV1 MINDIN7-16-GP
TV_LUMA, TV_CRMA, TV_COMP
LUMA, CRMA, COMP, NC#2, NC#5, GND, GND, GND, GND

D2 BAV99-7-F-GP DY — TV_COMP — 3D3V_S0 — C3 SCD1U16V2ZY-2GP DY
D1 BAV99-7-F-GP DY — TV_LUMA — 3D3V_S0 — C2 SCD1U16V2ZY-2GP DY
D4 BAV99-7-F-GP DY — TV_CRMA — 3D3V_S0 — C4 SCD1U16V2ZY-2GP DY

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Title: CRT/TV Connector
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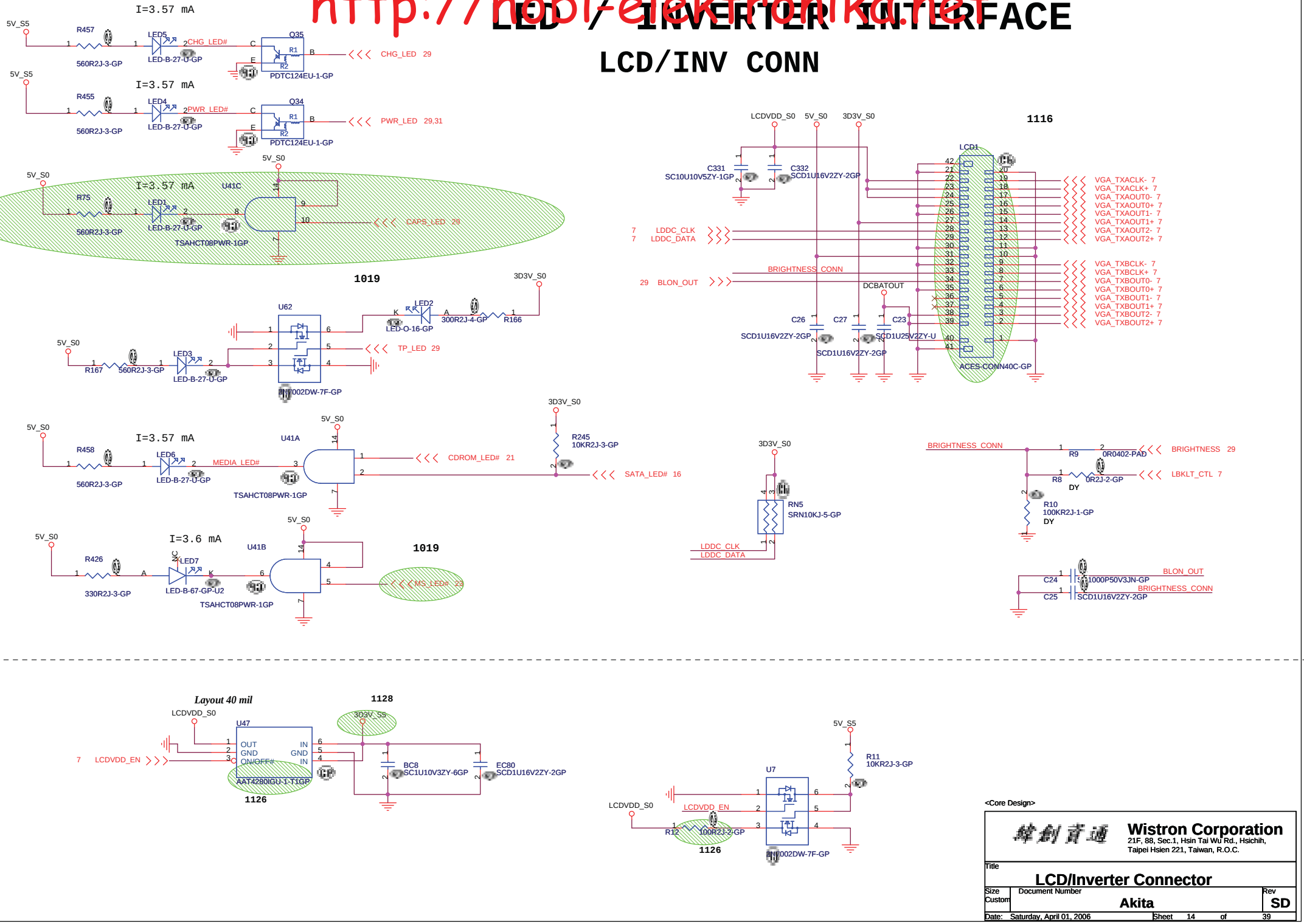
Date: Saturday, April 01, 2006 | Sheet 13 of 39

LED / INVERTER INTERFACE

LCD/INV CONN



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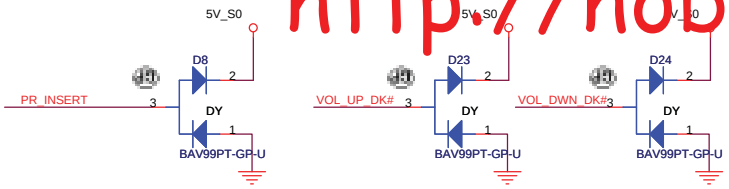
Title: LCD/Inverter Connector

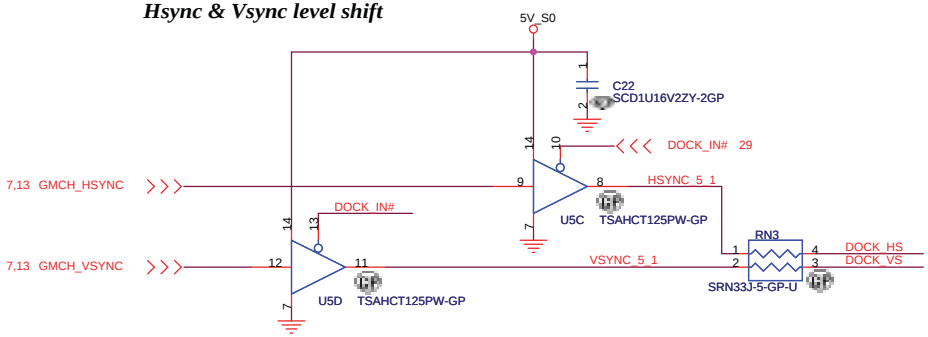
Size	Document Number	Rev
Custom	Akita	SD

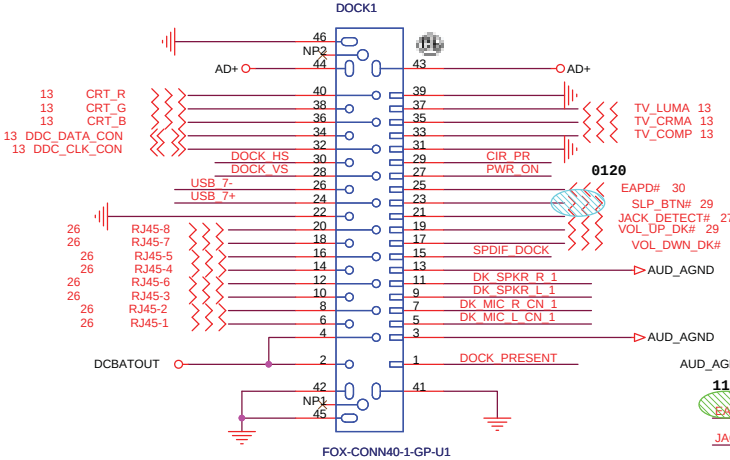
Date: Saturday, April 01, 2006 Sheet 14 of 39

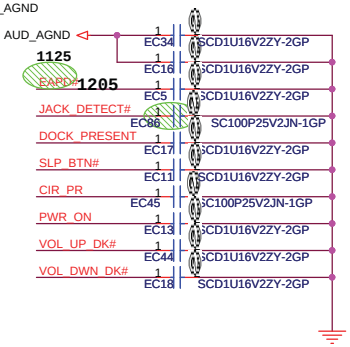
Docking Connector

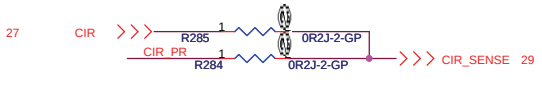


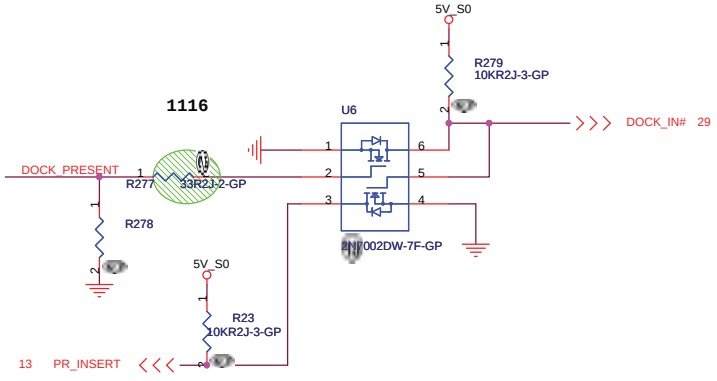
Hsync & Vsync level shift

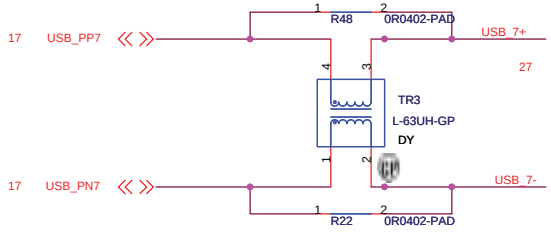


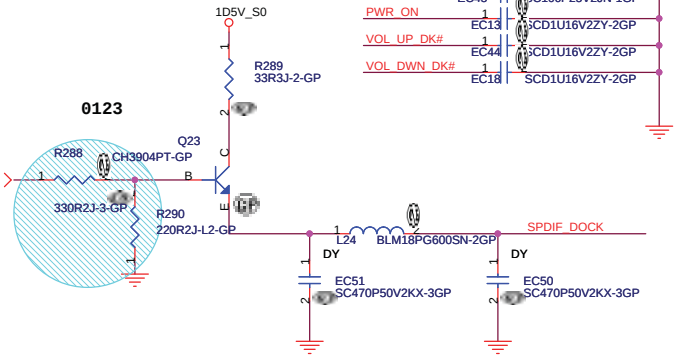


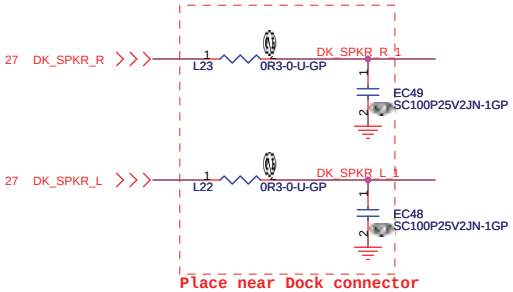


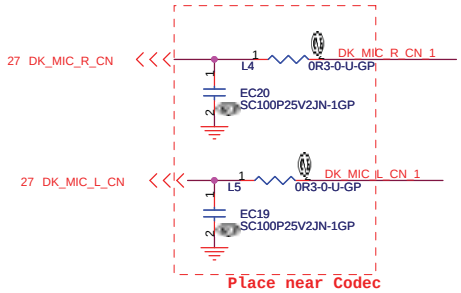


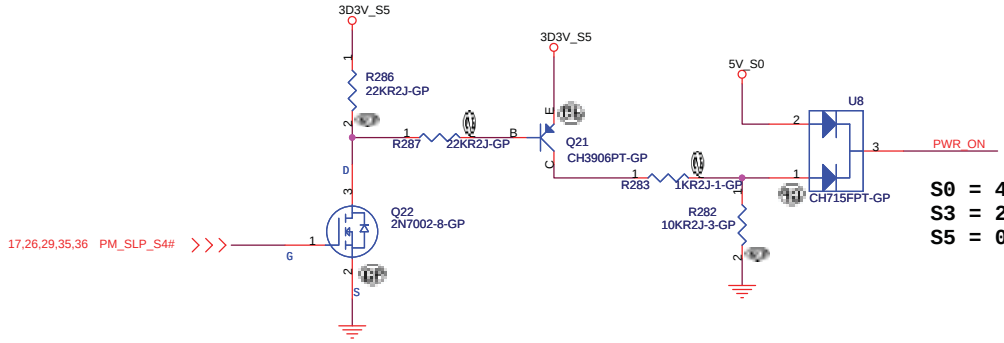












S0 = 4V
S3 = 2.5V
S5 = 0V

<Core Design>

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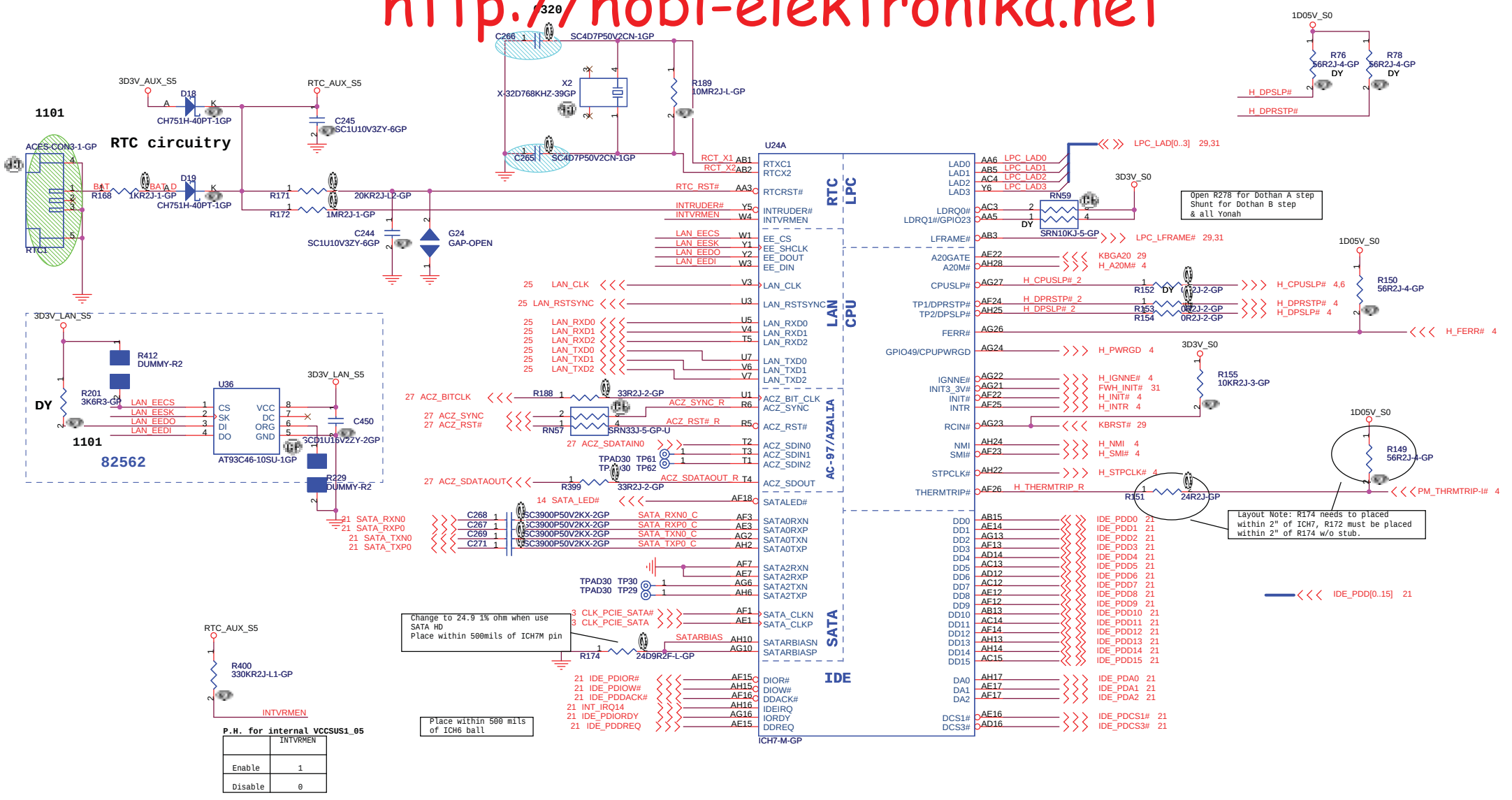
Title	Board to board conn/ Docking	
Size A3	Document Number Akita	Rev SD
Date: Friday, March 31, 2006	Sheet 15 of 39	



Placement Note:
Diatance between the ICH-6 M and cap on the "P" signal should be identical distance between the ICH-6 M and cap on the "N" signal for same pair.

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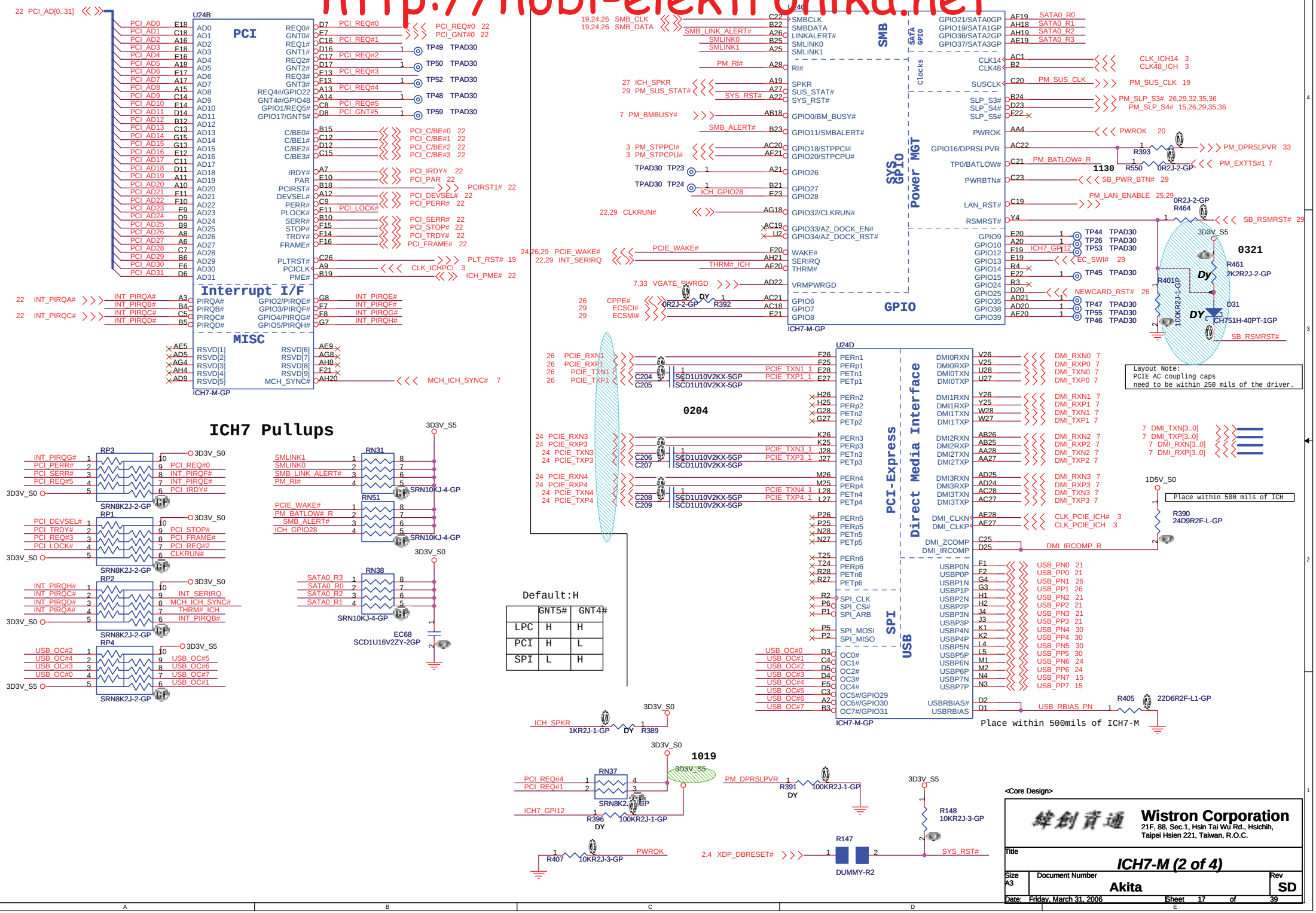
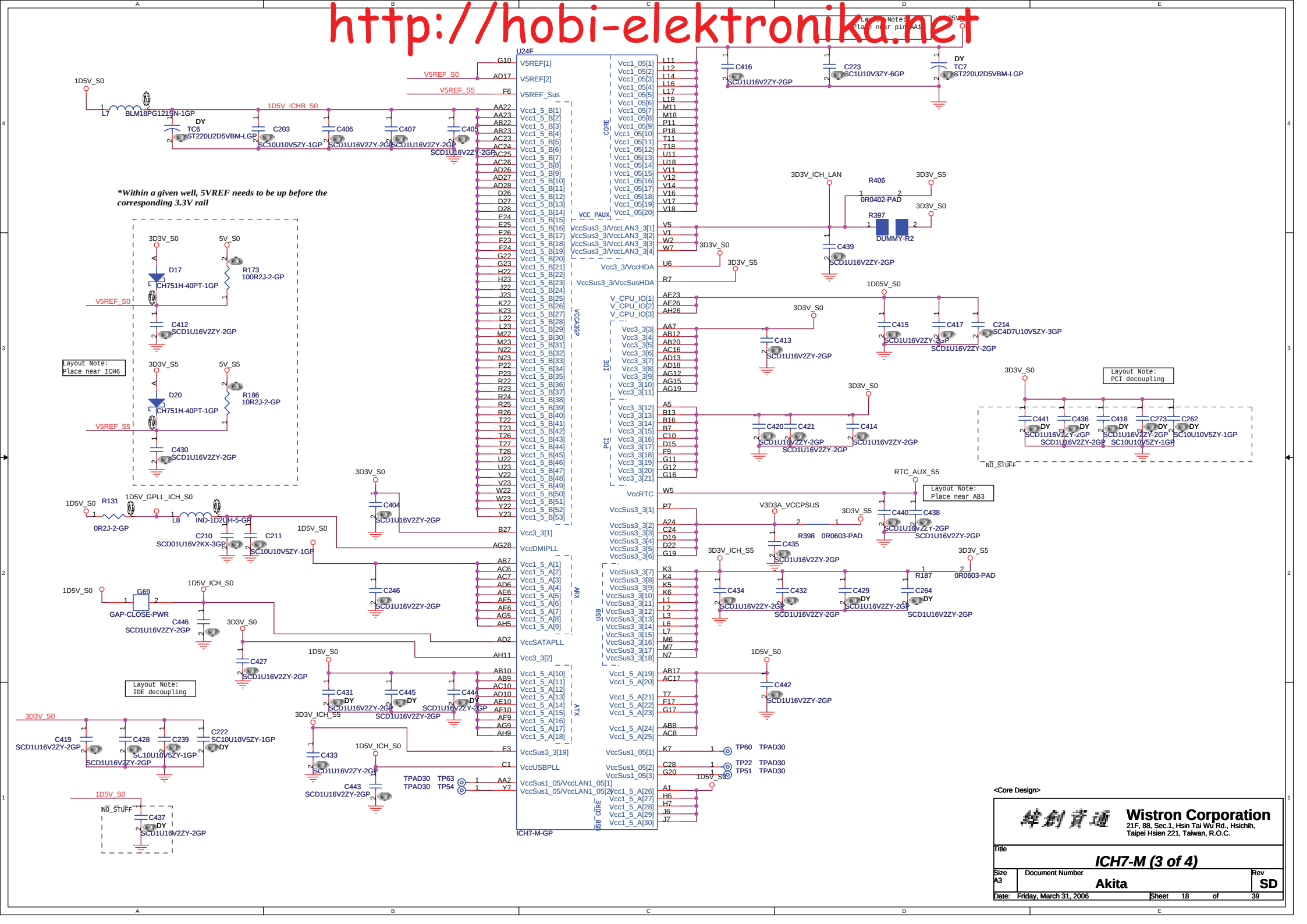
Title: **ICH7-M (1 of 4)**

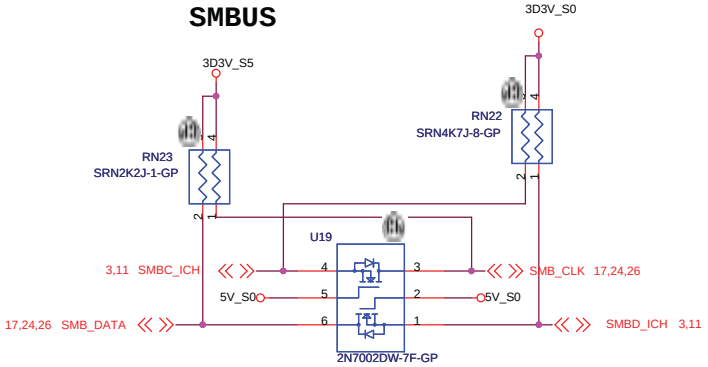
Size	Document Number	Rev
A3	Akita	SD

Date: Friday, March 31, 2006 Sheet 16 of 39



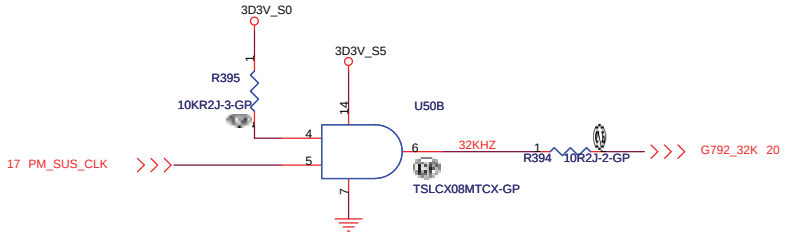


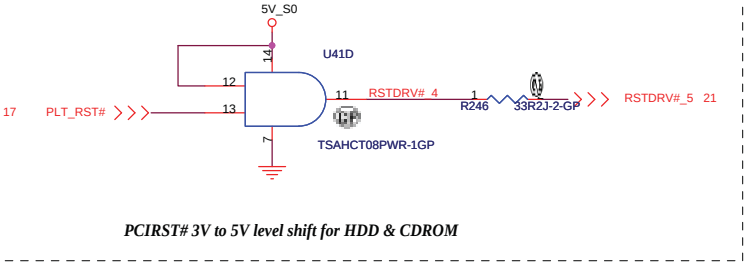
SMBUS



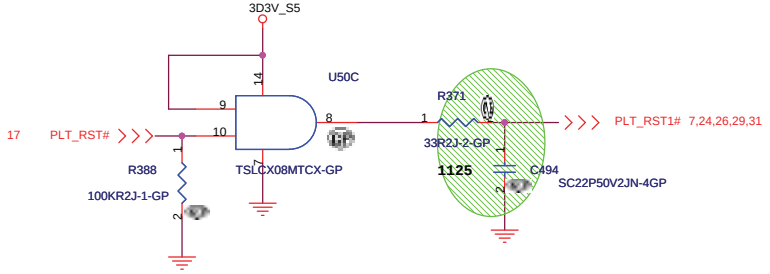
Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

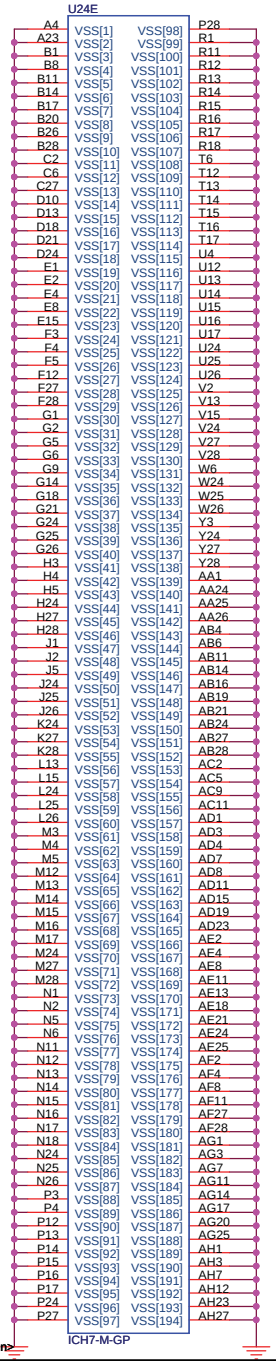
32K suspend clock output





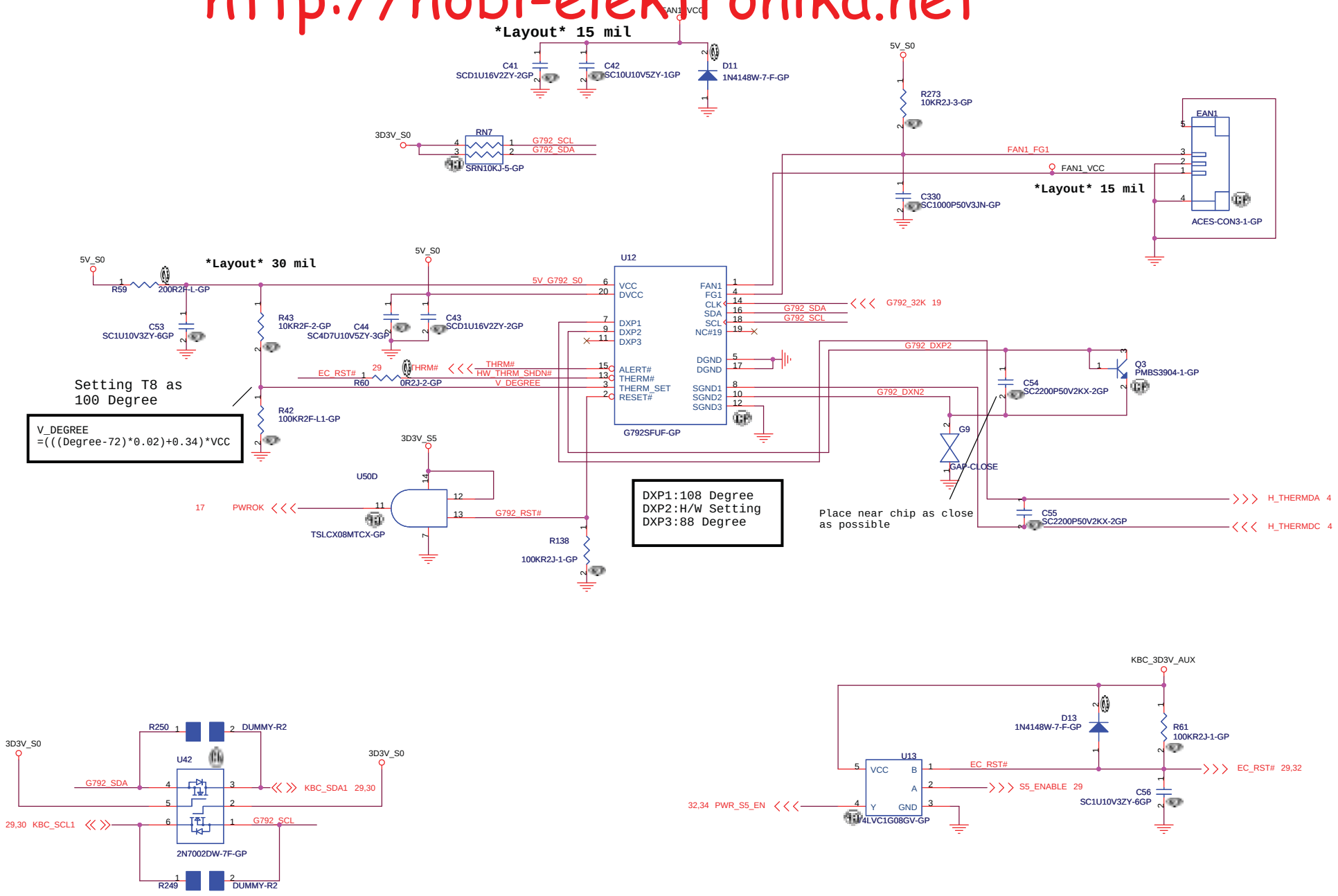
PCIRST# 3V to 5V level shift for HDD & CDROM





<Core Design>

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	ICH7-M (4 of 4)
Size A3	Document Number: Akita
Rev	SD
Date: Monday, February 06, 2006	Sheet 19 of 39



<Core Design>

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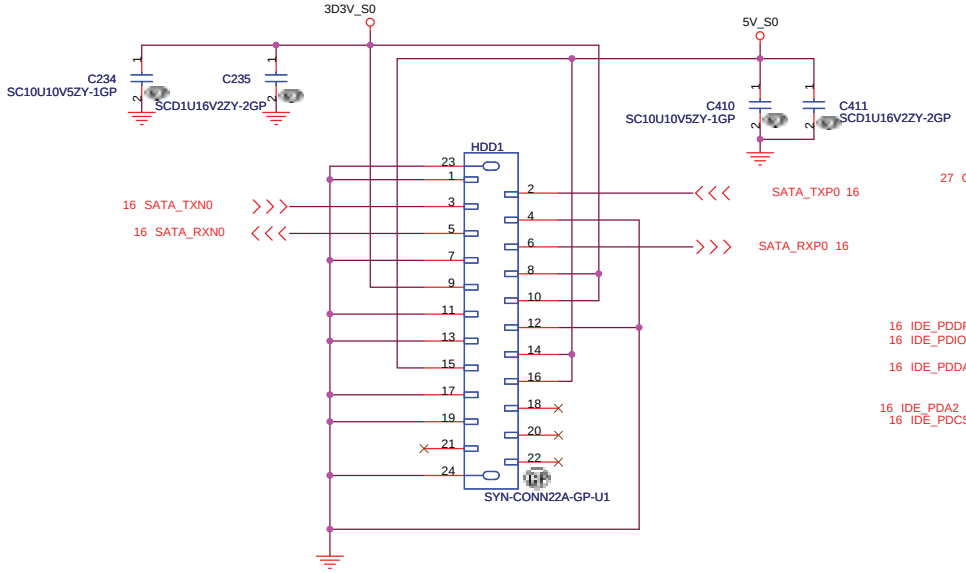
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor

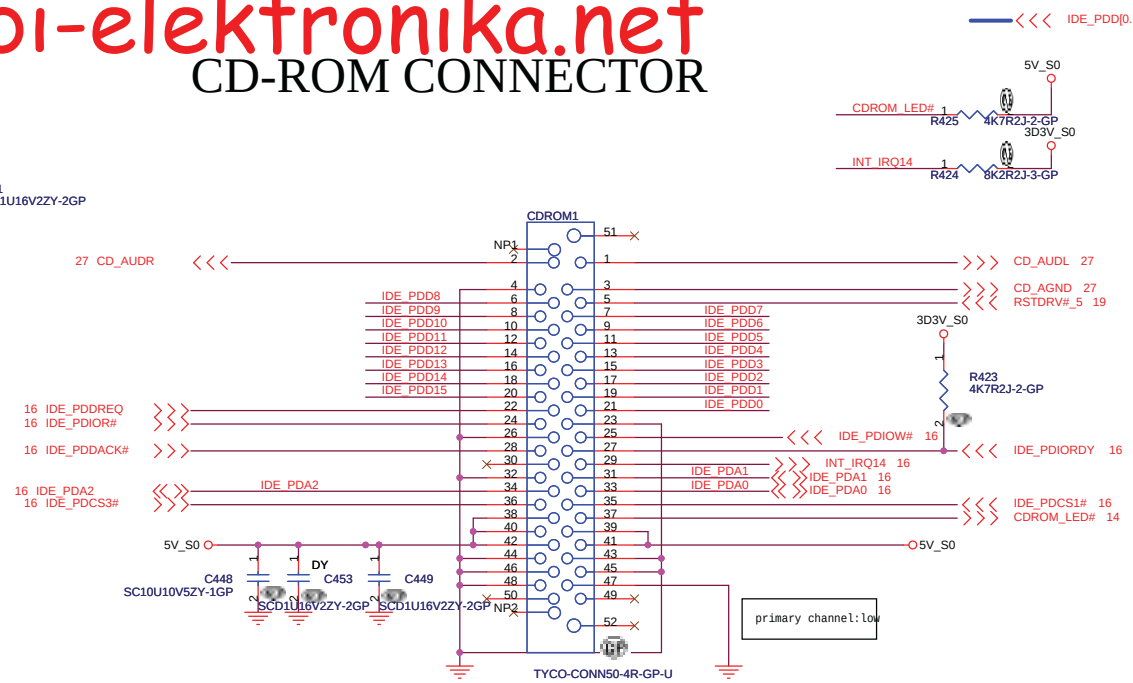
Size	Document Number	Rev
Custom	Akita	SD

Date: Monday, February 06, 2006 Sheet 20 of 39

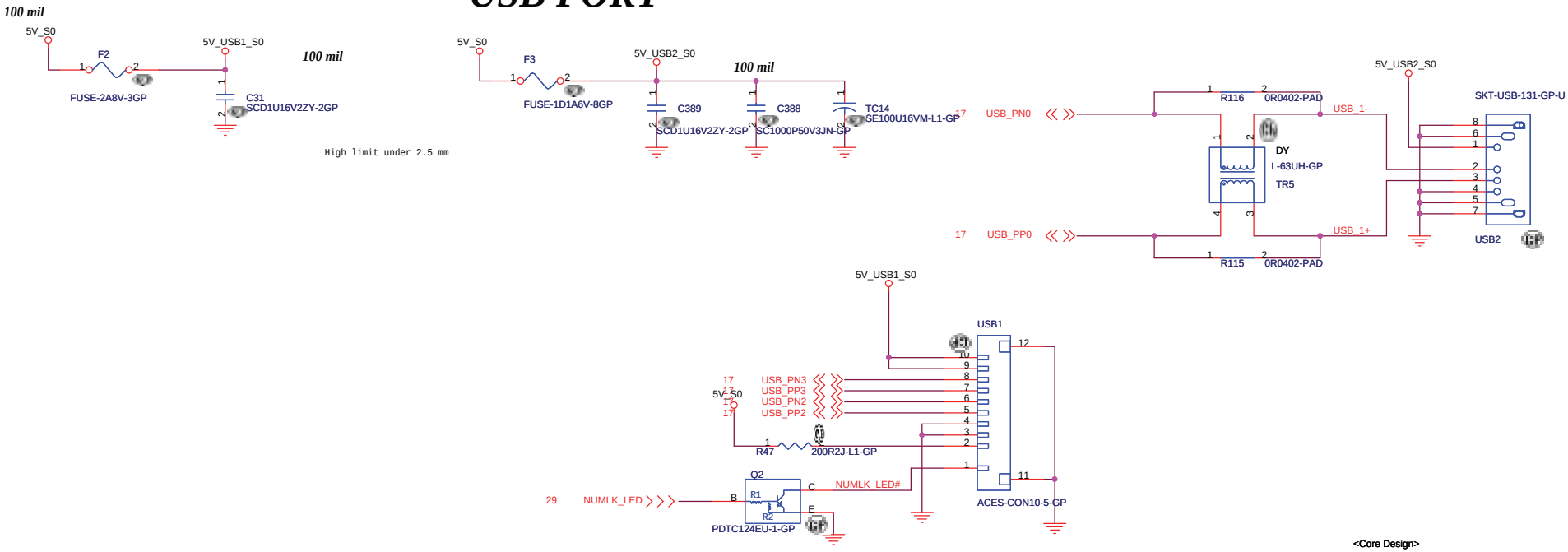
SATA HD Connector



CD-ROM CONNECTOR



USB PORT



<Core Design>

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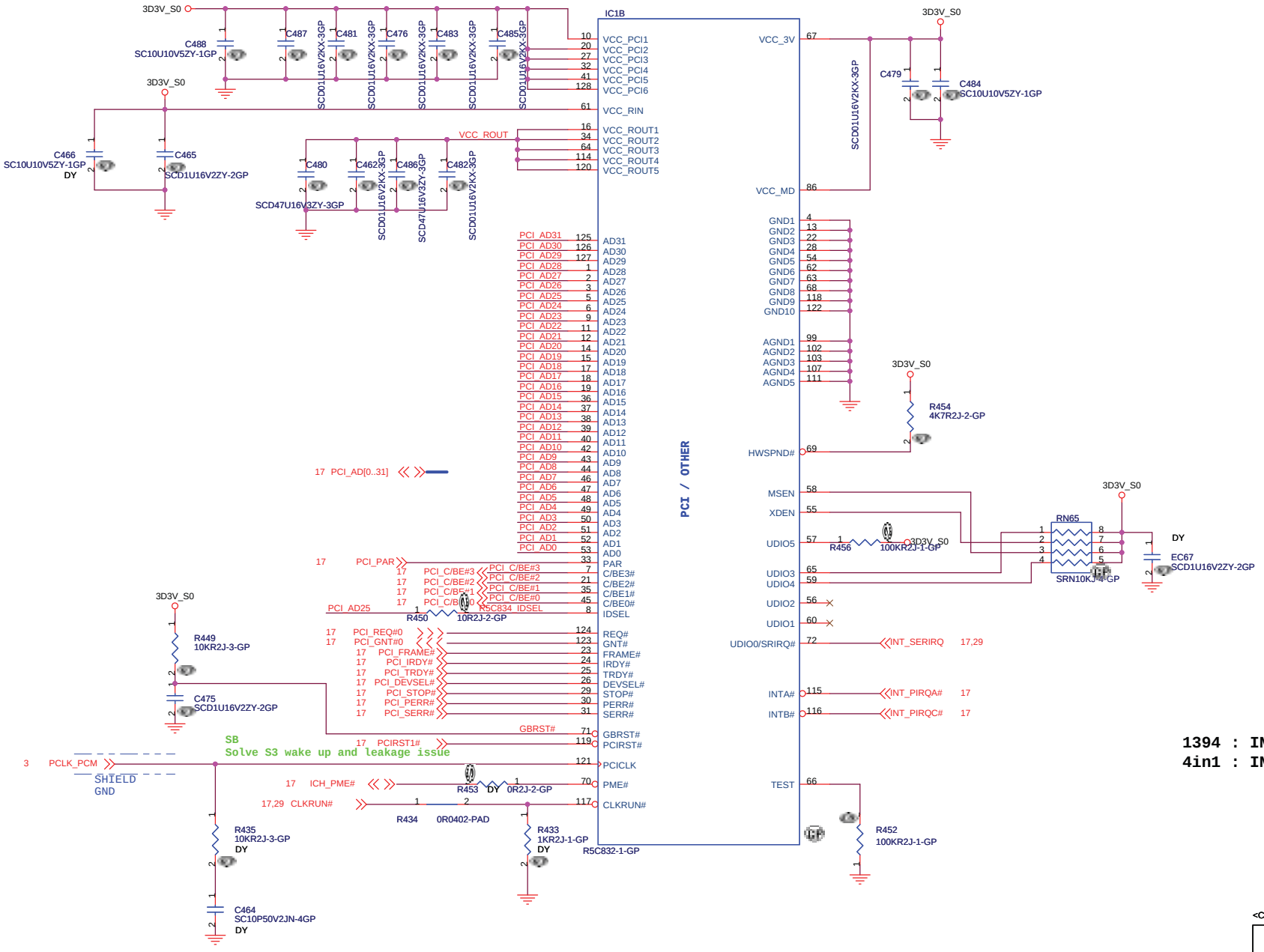
Taipei Hsien 221, Taiwan, R.O.C.

Title	HD/CDROM	
Size A3	Document Number: Akita	Rev SD
Date: Friday, March 31, 2006	Sheet 21 of 39	



1394 : INTA#
4in1 : INTB#

<Core Design>

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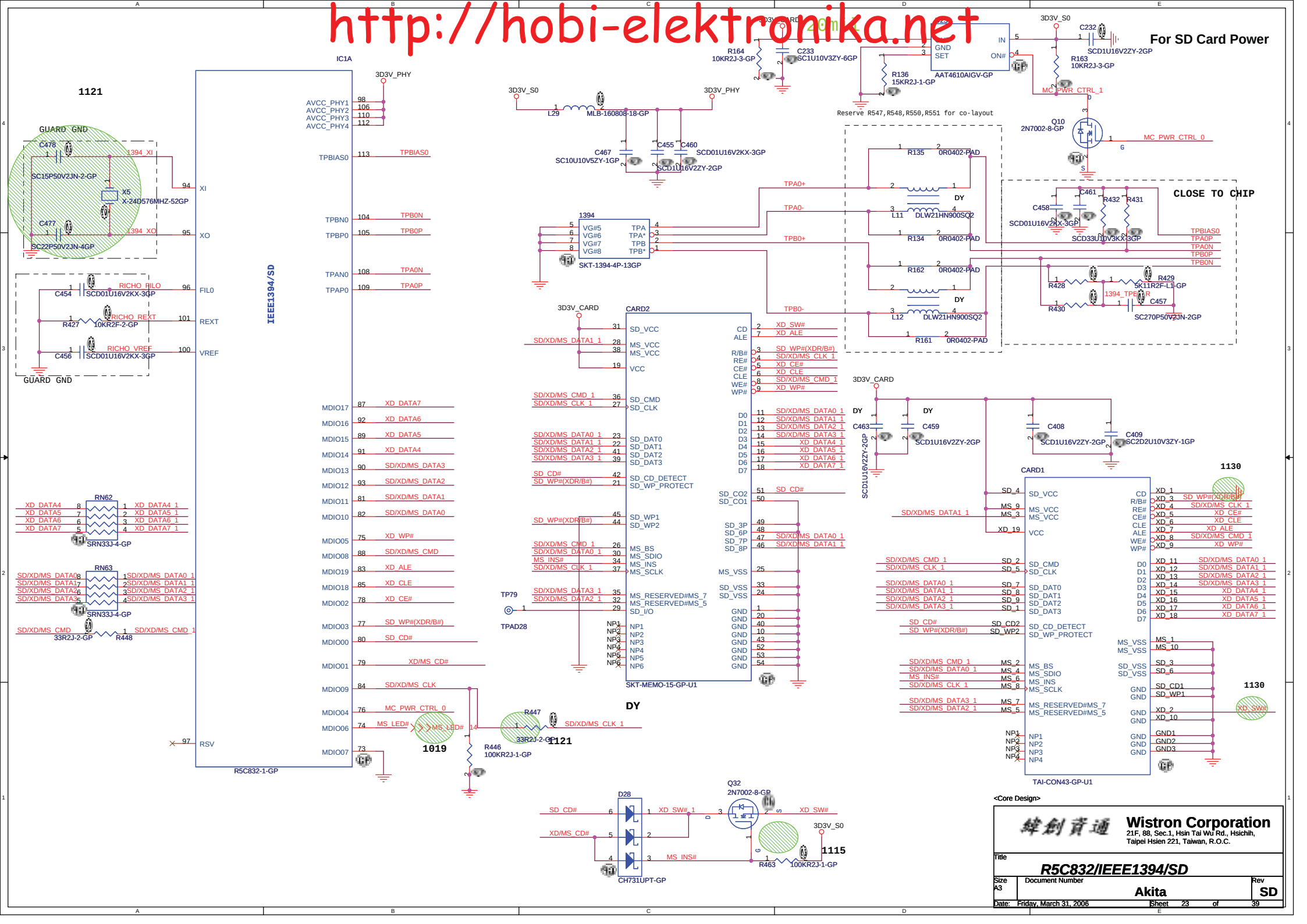
Taipei Hsien 221, Taiwan, R.O.C.

Title: *R5C832/PCI*

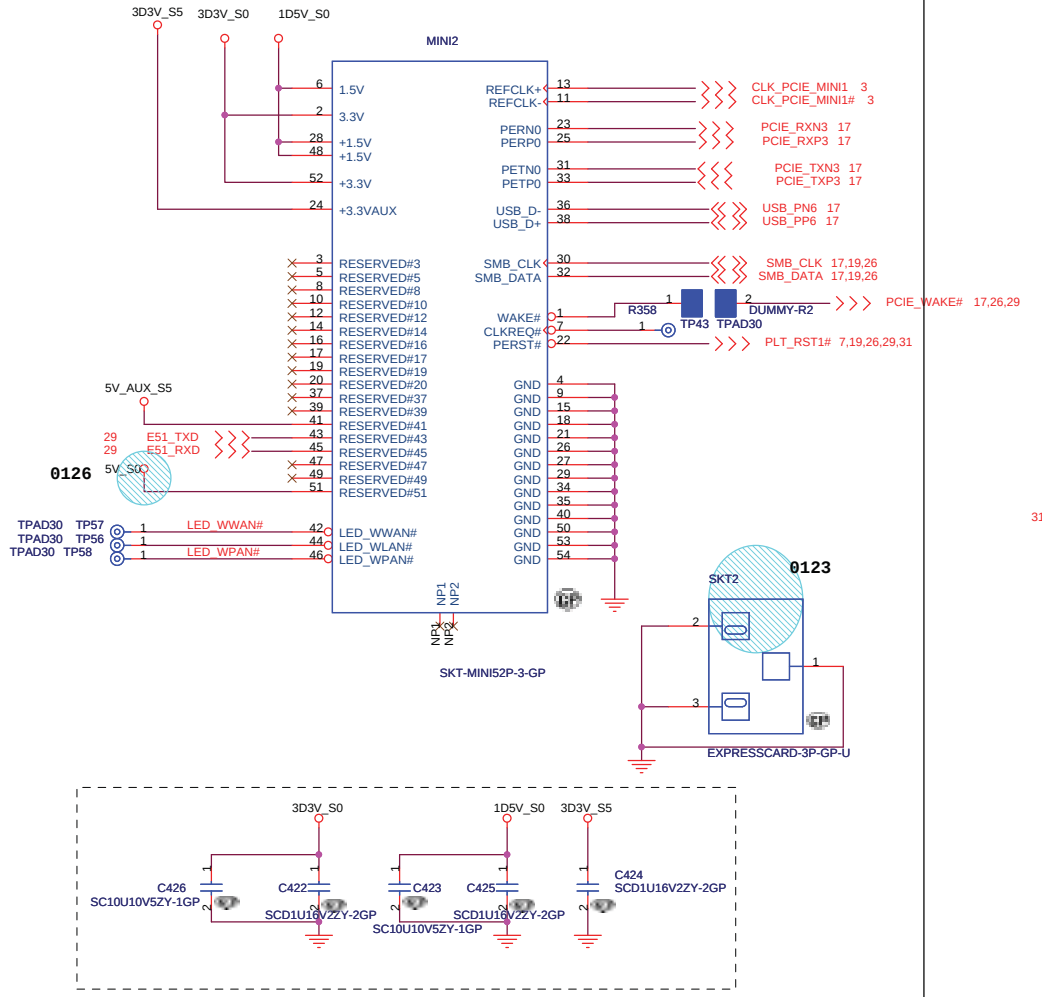
Size: A3 | Document Number: Akita | Rev: SD

Date: Friday, March 31, 2006 | Sheet 22 of 39

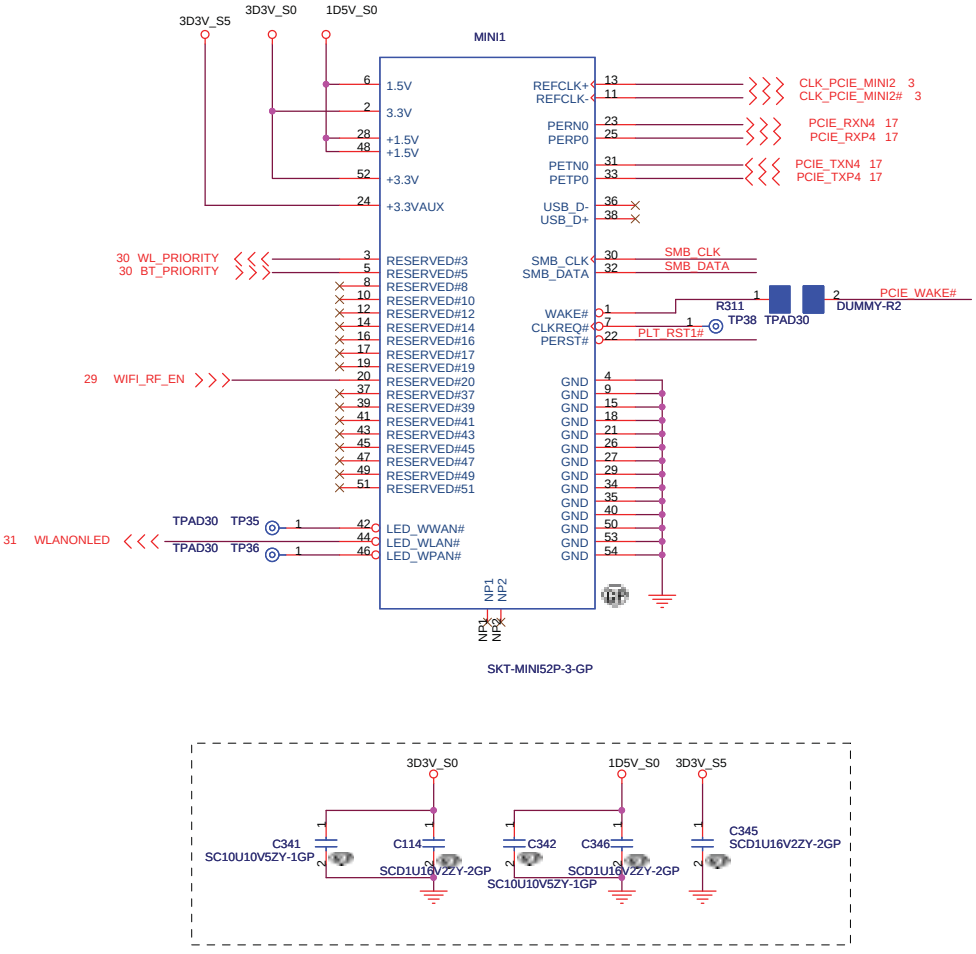


Mini Card Connector

Mini Card Connector 1



Mini Card Connector 2



<Core Design>

Wistron Corporation
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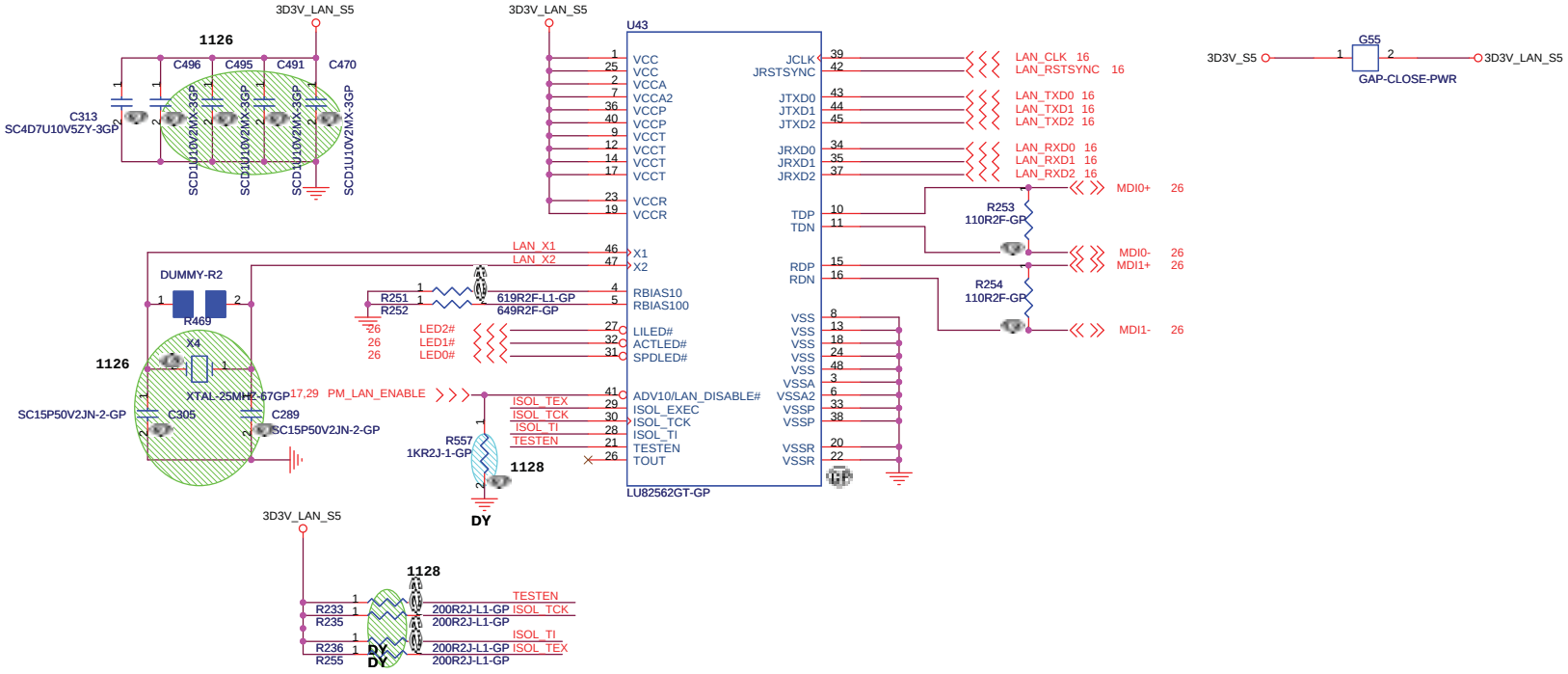
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINI CARD CONN .

Size: A3 | Document Number: Akita | Rev: SD

Date: Thursday, March 23, 2006 | Sheet 24 of 39



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN TEKOA**

Size	Document Number	Rev
A3	Akita	SD

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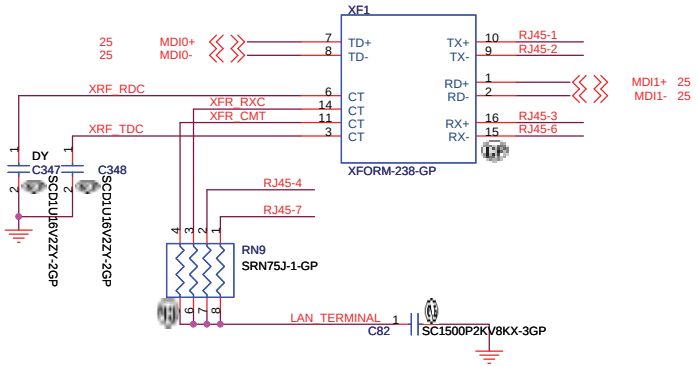
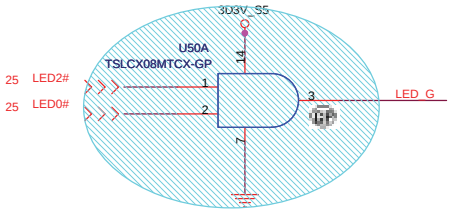
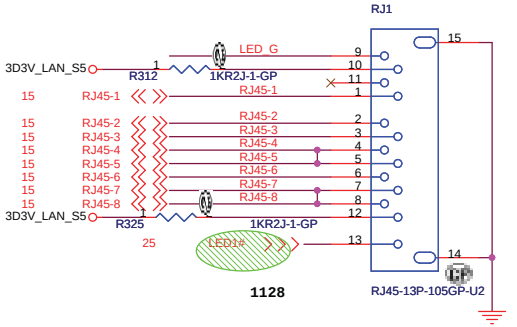
Off : Link 10 Mbps
Green : Link 100 Mbps
Orange : Link 1000 Mbps

10/100M Lan Transformer



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.



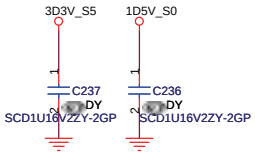


Green : Link up
Blinking : TX/RX activity

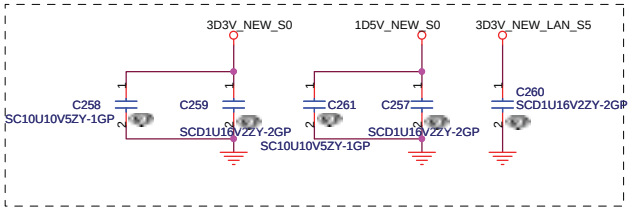
PIN09 : GREEN
PIN11 : ORANGE
PIN13 : YELLOW

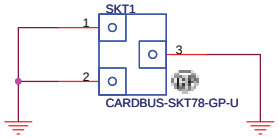
NEWCARD Connector

Place them Near to Chip

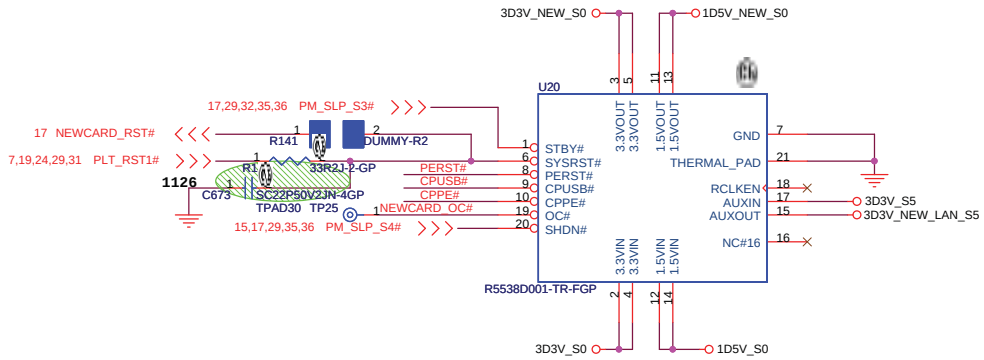


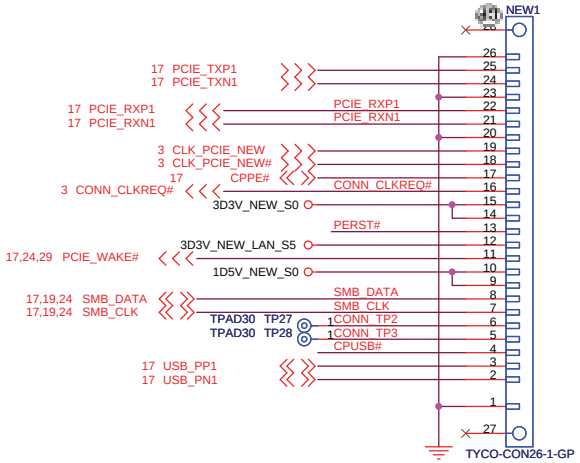
Place them Near to Connector





For Newcard socket





<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: New Card
Size: A3
Document Number: Akita
Rev: SD
Date: Friday, March 31, 2006
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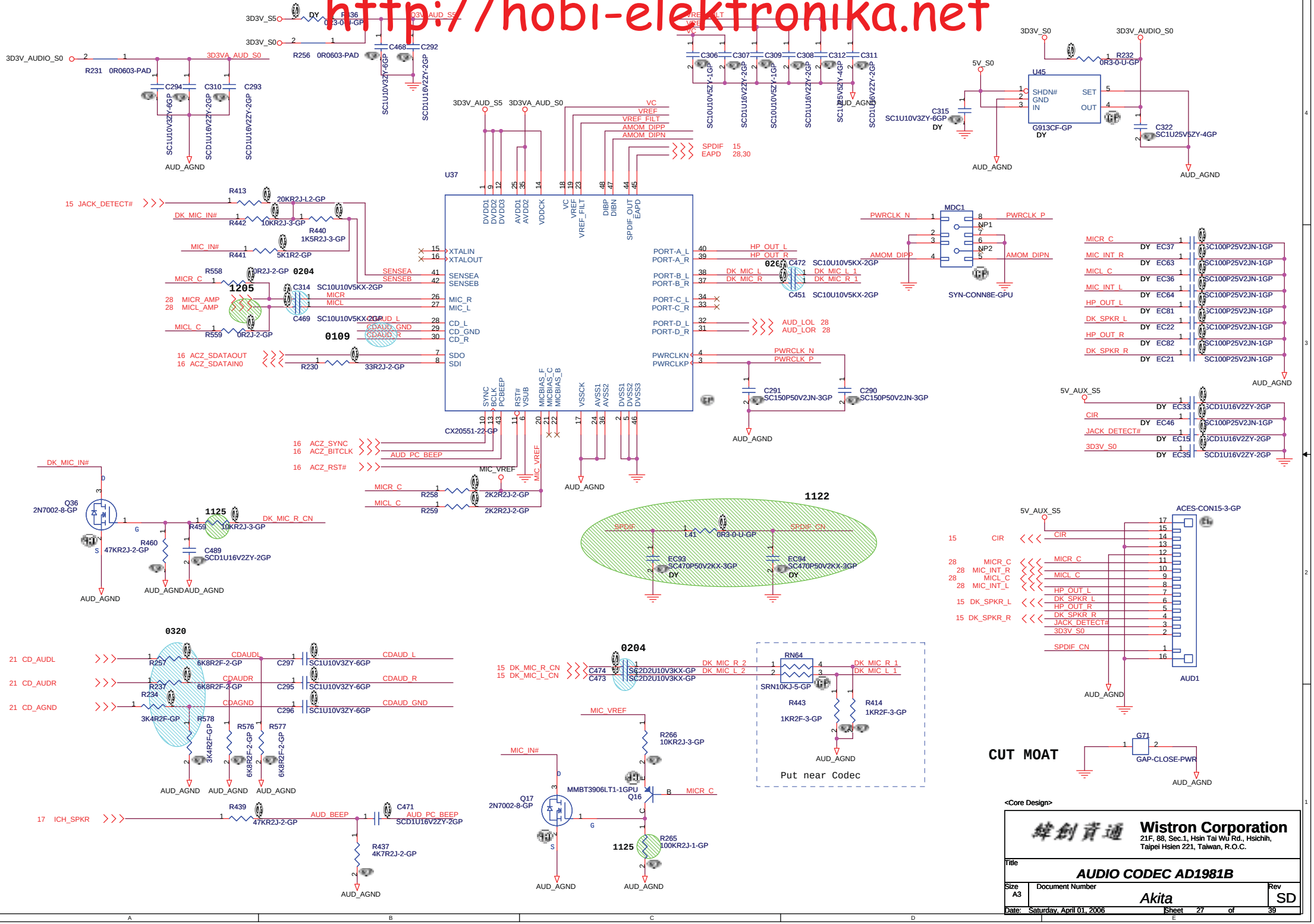


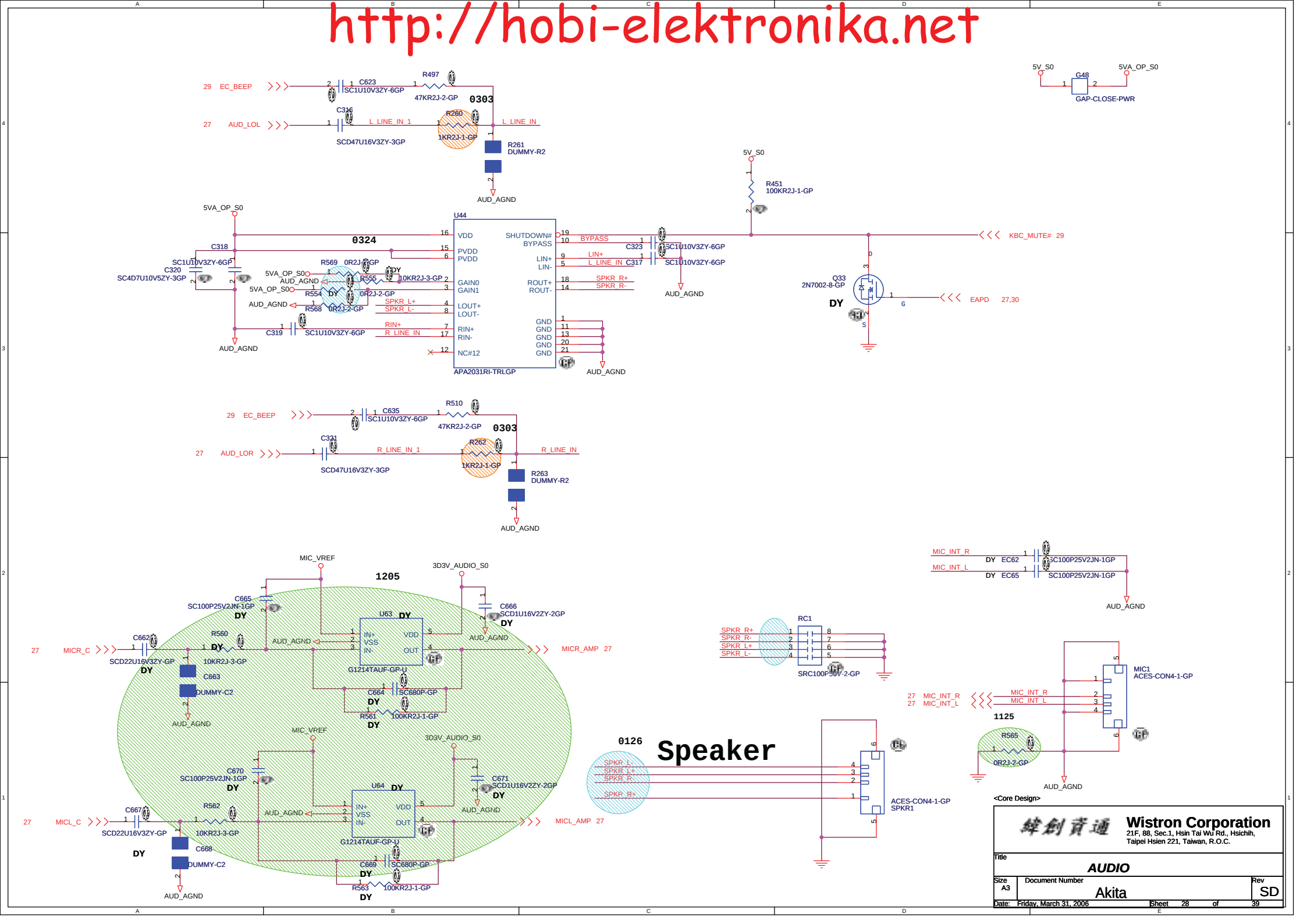
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

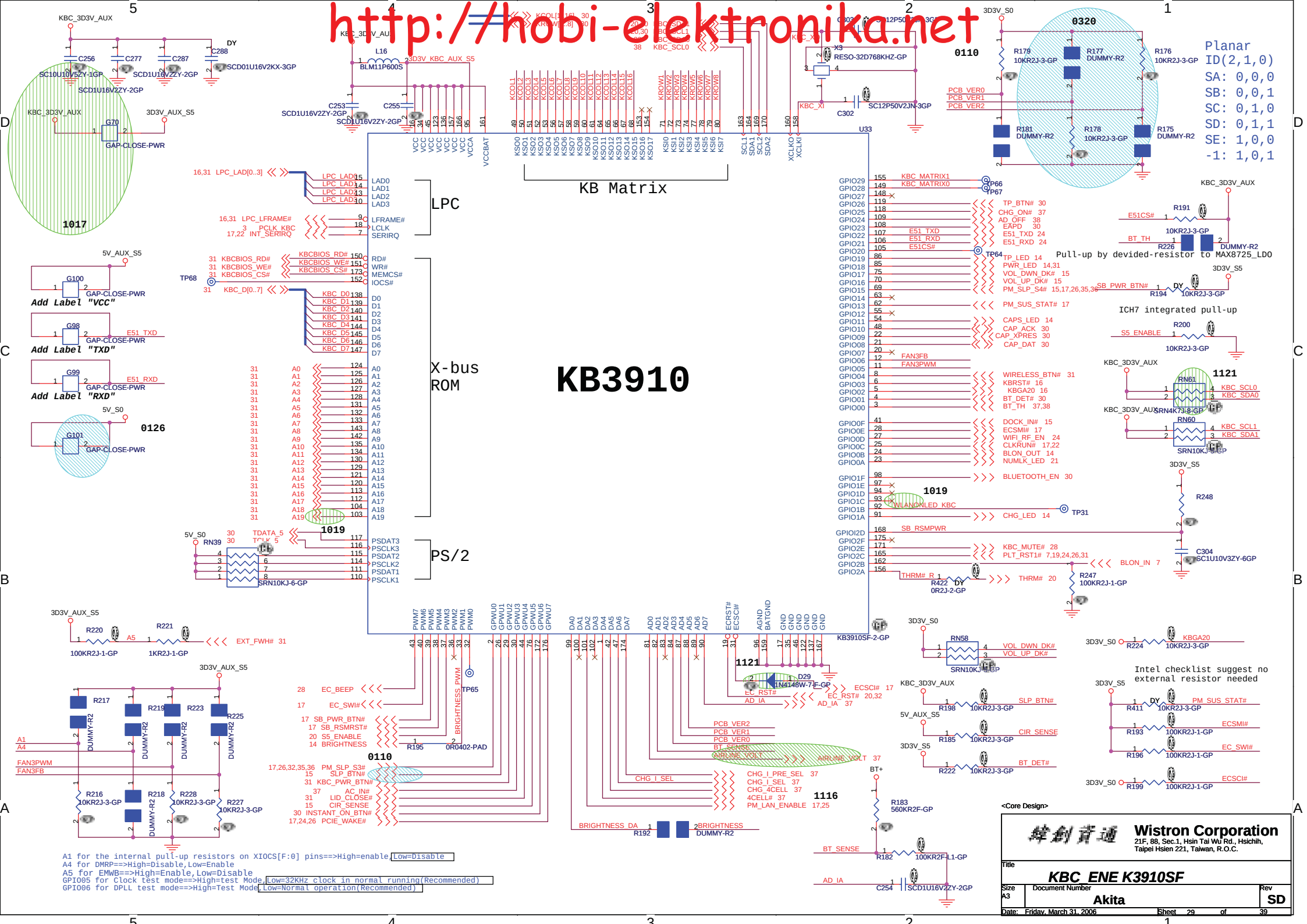
Title: **AUDIO CODEC AD1981B**

Size	Document Number	Rev
A3	Akita	SD

Date: Saturday, April 01, 2006 Sheet 27 of 39



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***AUDIO***	
Size A3	Document Number: Akita	Rev: SD
Date: Friday, March 31, 2006	Sheet 28 of 39	



CAMERA

Blue thumb

Internal KeyBoard Connector

29 KROW[1..8]
29 KCOL[1..16]

KB1
ACES-CON24-2-GP

Keyboard matrix (from vendor)

	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1

TouchPad Connector

5V_S5
TPAD1
ACES-CON8-6-GP
29 TDATA_5
29 TCLK_5

CAMERA

5V_S0
ACES-CON5-1GP
CAM1
USB_4-
USB_4+

17 USB_PN4
17 USB_PP4
TR4 L-63UH-GP DY

17 USB_PN5
17 USB_PP5
TR6 L-63UH-GP DY

Blue thumb

BT1
ACES-CON8-4-GP
3D3V_BT_S0
USB_5+
USB_5-
31 BT_LED
24 WL_PRIORITY
24 BT_PRIORITY
29 BT_DET#

Close to CN8

29 BLUETOOTH_EN
U53 G913CF-GP
MAX 150mA

TOUCH-PAD SWITCH

SW1 SW-TACT-68-GP-T
TP_BTN# 29

CAPACITY BUTTON

CAP1
ACES-CON12-4-GP
29 CAP_XPRES
20,29 KBC_SCL1
20,29 KBC_SDA1
29 CAP_ACK
29 CAP_DAT
29 INSTANT_ON_BTN#
EAPD#

0322
0119
0204

EMI

RC6 SRC100P50V-2-GP
RC5 SRC100P50V-2-GP
RC4 SRC100P50V-2-GP
RC7 SRC100P50V-2-GP
RC2 SRC100P50V-2-GP
RC3 SRC100P50V-2-GP
for EMI

<Core Design>
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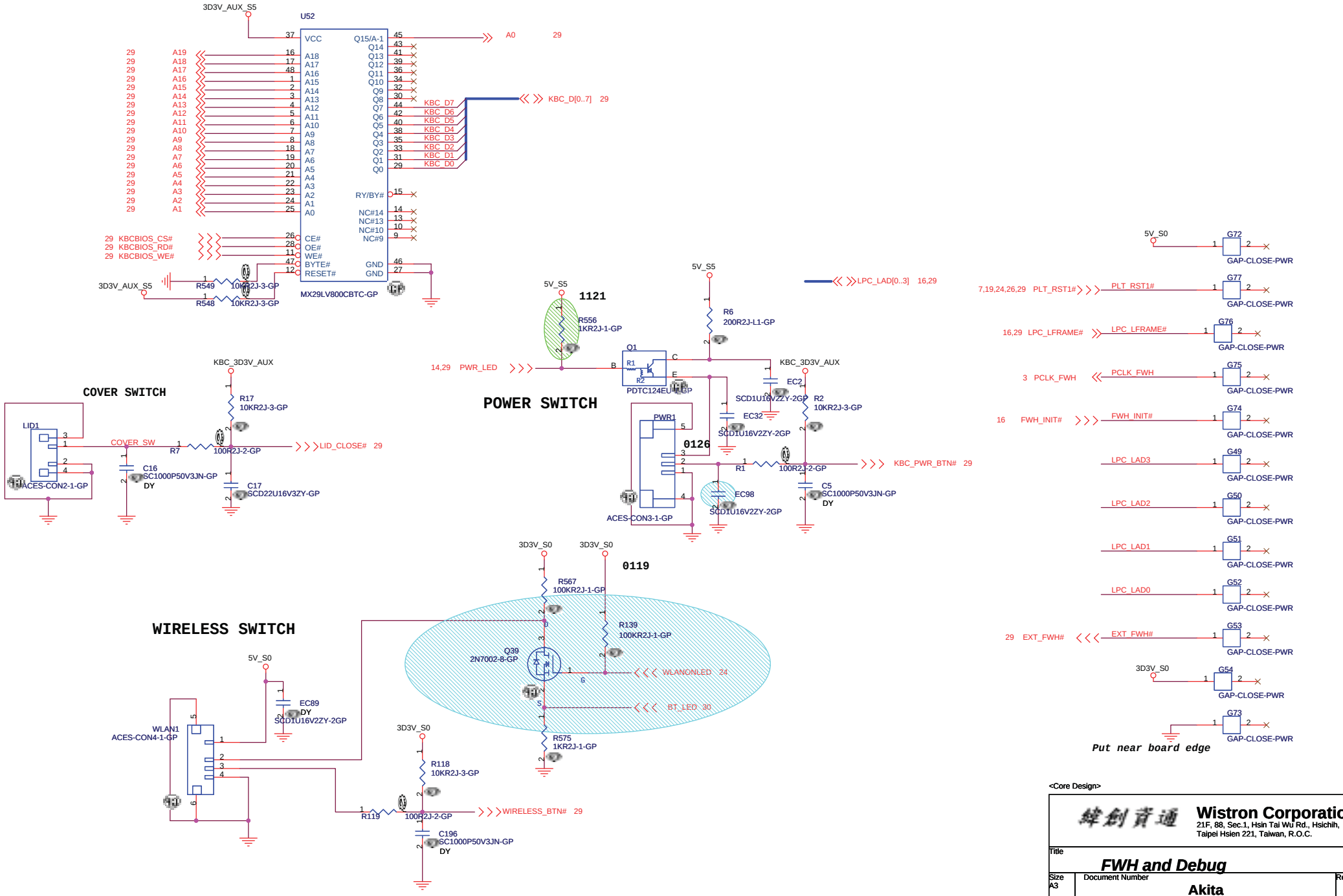
Title: KeyBoard-CONN
Size: A3
Document Number: Akita
Rev: SD
Date: Friday, March 31, 2006
Sheet 30 of 39



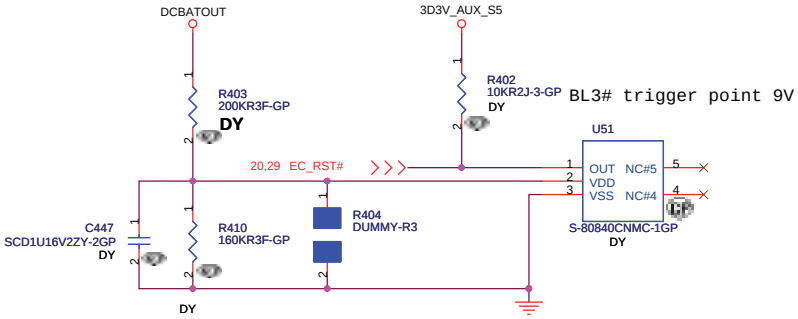
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

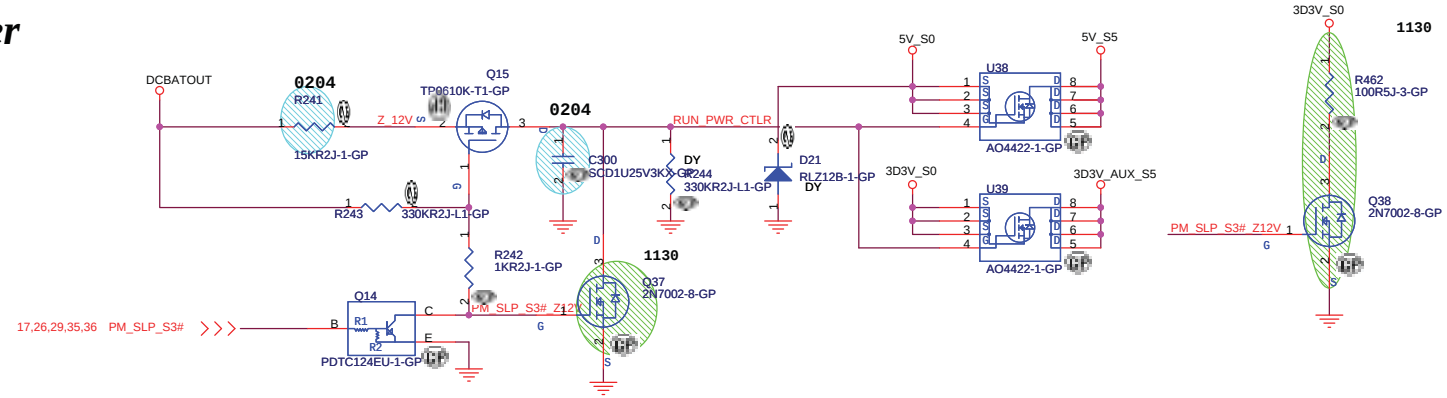
Title: FWH and Debug

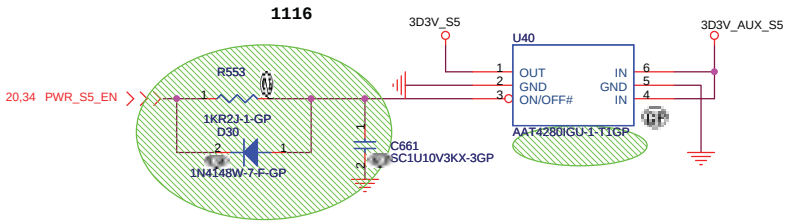
Size: A3 | Document Number: Akita | Rev: SD

Date: Friday, March 31, 2006 | Sheet 31 of 39



Run Power





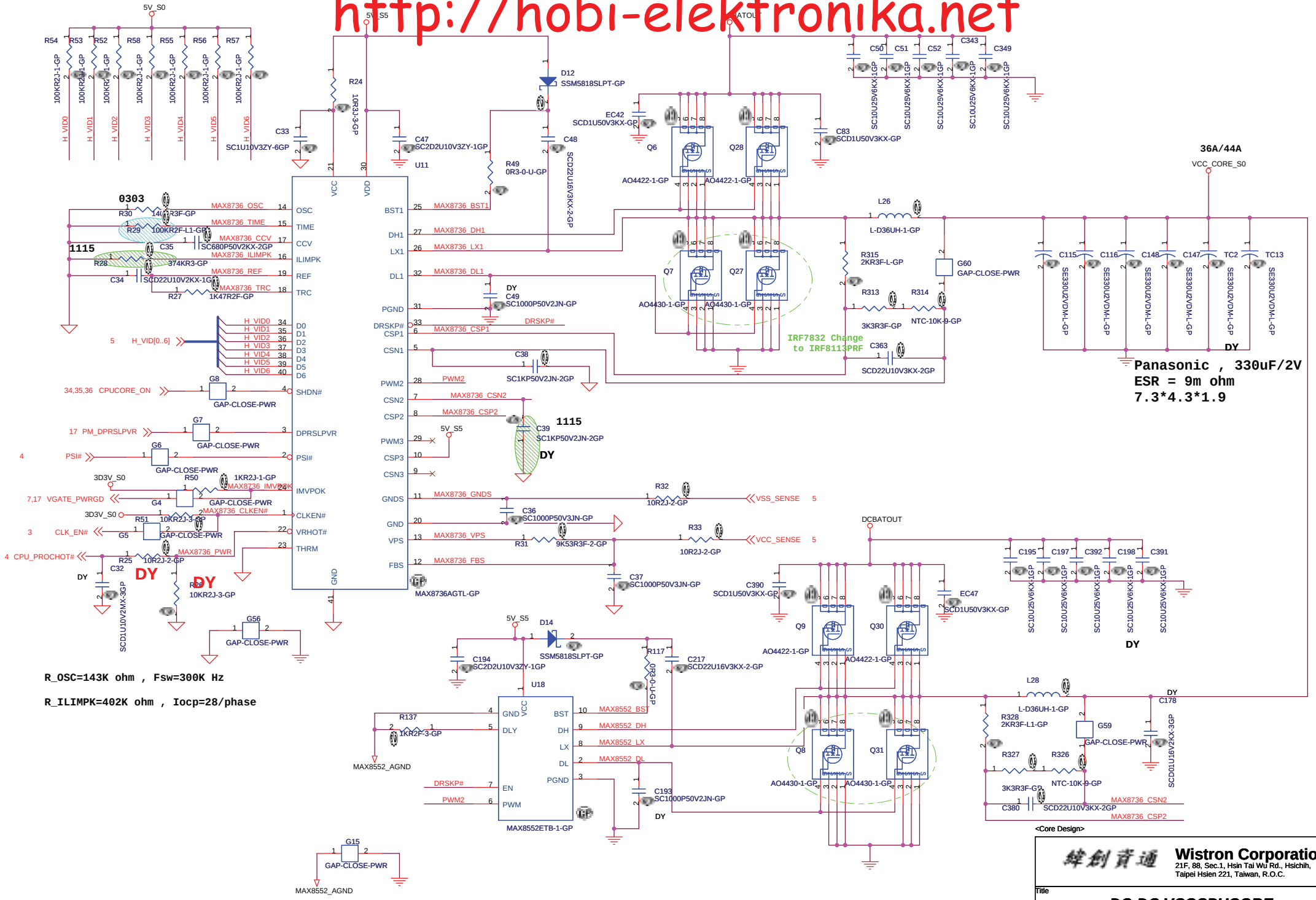
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PWRPLANE&RESETLOGIC

Size: A3 | Document Number: Akita | Rev: SD

Date: Friday, March 31, 2006 | Sheet 32 of 39

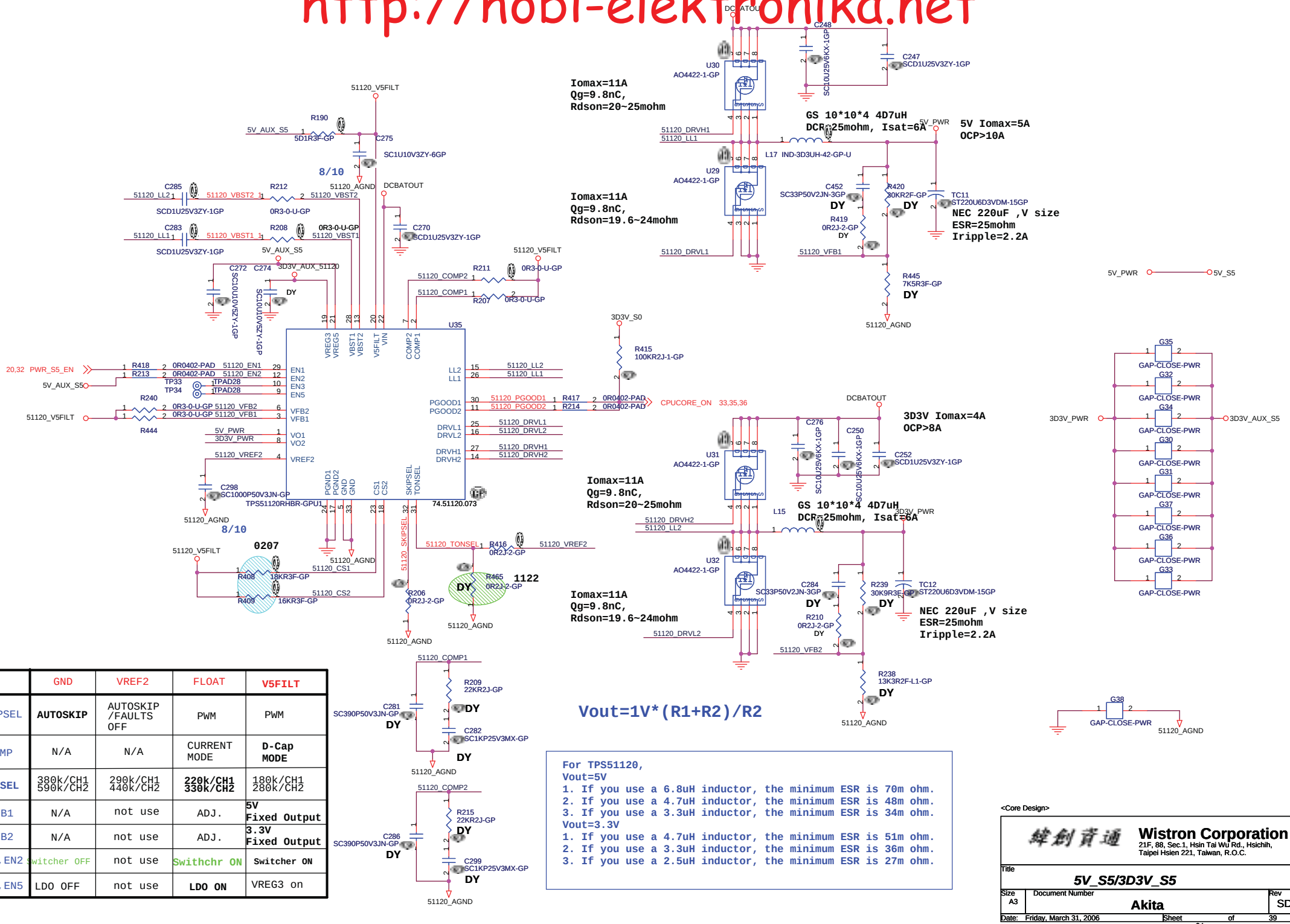


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC-DC VCCCPUCORE

Size: A3 | Document Number: Akita | Rev: SD

Date: Friday, March 31, 2006 | Sheet 33 of 39



	GND	VREF2	FLOAT	V5FILT
SKIPSEL	**AUTOSKIP**	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	**D-Cap MODE**
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	**220k/CH1 330k/CH2**	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	**5V Fixed Output**
VFB2	N/A	not use	ADJ.	**3.3V Fixed Output**
EN1,EN2	Switcher OFF	not use	Swithchr ON	**Switcher ON**
EN3,EN5	LDO OFF	not use	**LDO ON**	VREG3 on

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 5V_S5/3D3V_S5

Size: A3 | Document Number: Akita | Rev: SD

Date: Friday, March 31, 2006 | Sheet 34 of 39

Iocp=7.0 2 = 14A*
Rds,on=17m ohm
*Vcs1=Iocp*Rds,on=238mV*
VILIM=Vcs1/0.1=2.38V

*Iocp=7.0*2 = 14A*
Rds,on=17m ohm
*Vcs2=Iocp*Rds,on=28mV*
VILIM2=Vcs2/0.1=2.38V

1D8V / 7.0A
OCP>=14A

1D05V_S0/7A
OCP>=14A

NEC
Irms=7.5A(Isat=10.4A)
DCR=13mohm
12*12*5.5

Iomax=11A
Qg=9.8nC,
Rdson=20~25mohm

Iomax=11A
Qg=9.8nC,
Rdson=19.6~24mohm

Panasonic 220uF/2D5V
ESR=15m ohm
Iripple=2.7 A

Panasonic 220uF/2V
ESR=15m ohm
Iripple=2.7 A

Voutsetting=1.820V

Voutsetting=1.0511V

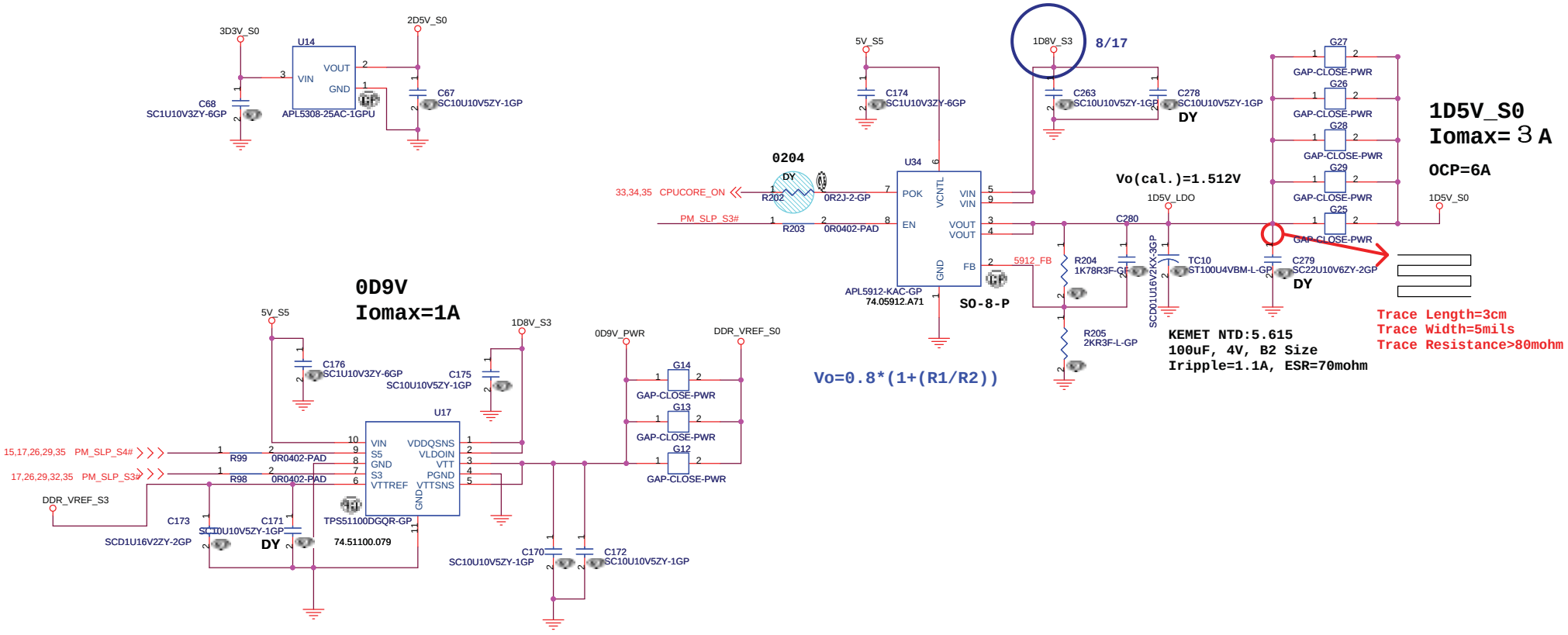
Vout=Vfb*(1+(R1/R2))
Where Vfb=1.0V,R2=10Kohm

Ton	Frequency (Out1)KHz	Frequency (Out2)KHz
AGND	620	460
REF	485	355
OPEN	345	255
VCC	235	170

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 1D8V_S3/1D05V_S0
Size: A3
Document Number: Akita
Rev: SD
Date: Friday, March 31, 2006
Sheet 35 of 39



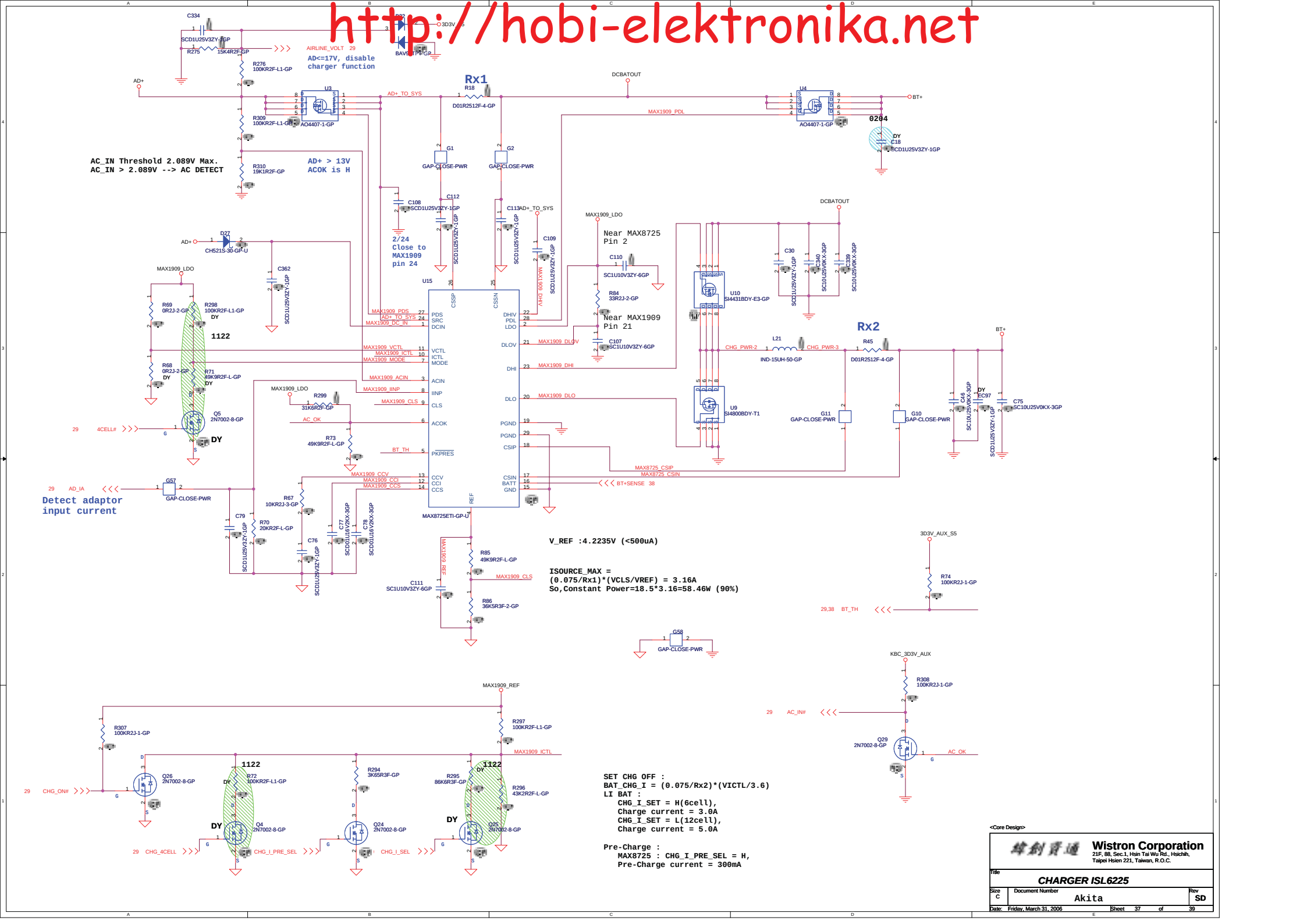
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 0D9V_LDO/1D2V_LDO/1D5V_LDO/2D5V_LDO

Size	Document Number	Rev
A3	Akita	SD

Date: Friday, March 31, 2006 Sheet 36 of 39



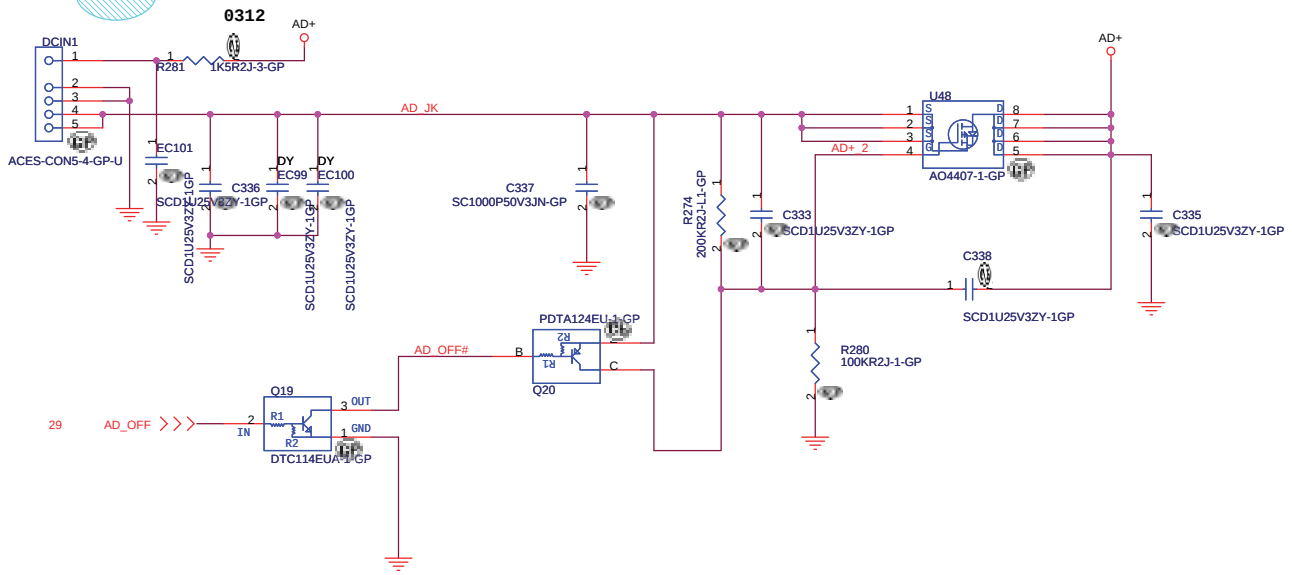
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER ISL6225

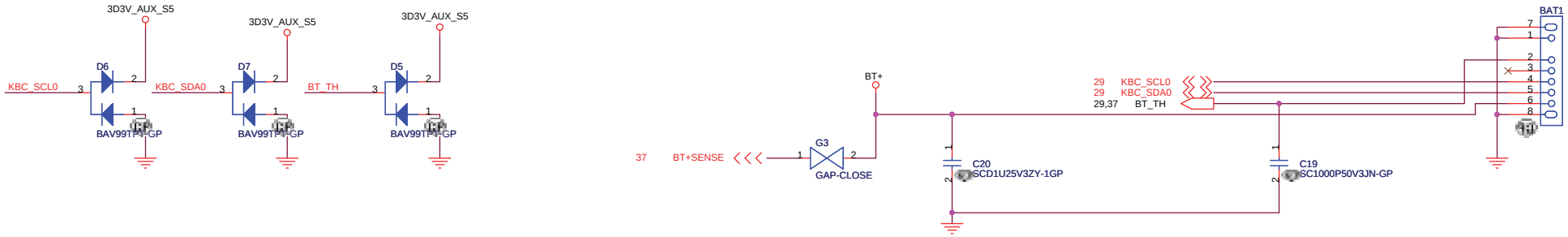
Size	Document Number	Rev
C	Akita	SD

Date: Friday, March 31, 2006 Sheet 37 of 39

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AD/BATT CONN		
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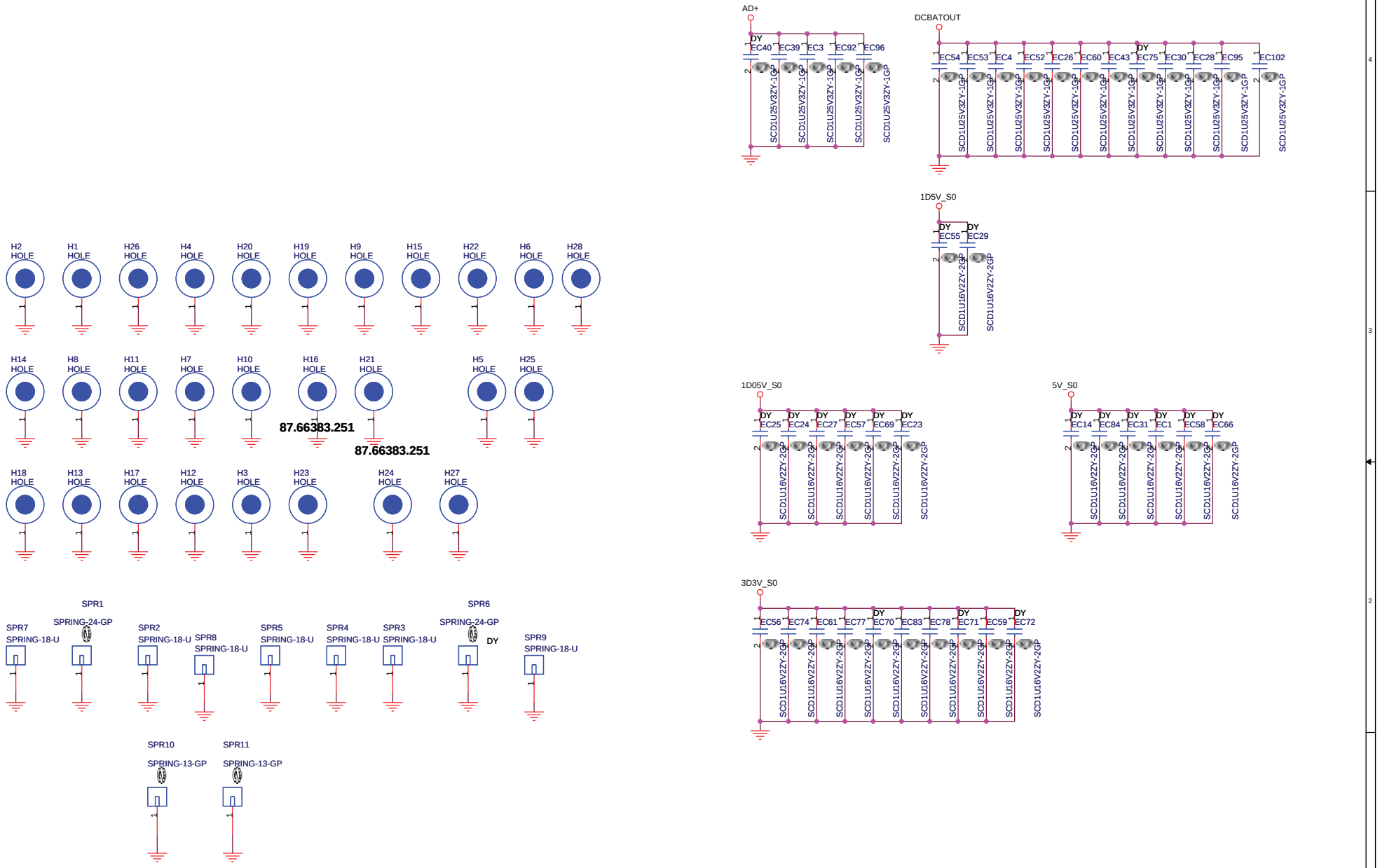

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Title	***MISC***	
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