Application Report
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Semiconductor and IC Package Thermal Metrics

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ABSTRACT

Many thermal metrics exist for semiconductor and integrated circuit (IC) packages ranging from $R_{\theta JA}$ to Ψ_{JT}. Often, these thermal metrics are misapplied by those who try to use them to estimate junction temperatures in their systems. This document describes traditional and new thermal metrics and puts their application in perspective with respect to system-level junction temperature estimation.

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Trademarks

1 $R_{\theta JA}$ Junction-to-Ambient and $R_{\theta JMA}$ Junction-to-Moving Air

The junction-to-ambient thermal resistance, $R_{\theta JA}$, is the most commonly reported thermal metric and is the most often misused. $R_{\theta JA}$ is a measure of the thermal performance of an IC package mounted on a specific test coupon. The intent of $R_{\theta JA}$ is to give a metric by which the relative thermal performance of a package can be compared. Thus, the thermal performance of a TI device can be compared to a device from another company. This is true when both companies use a standardized test to measure $R_{\theta JA}$, such as that specified by JEDEC in the EIA/JESD51-x series of documents. Sometimes, however, JEDEC conditions are not followed and the excursions from the standards are not documented. These test variations can have a dramatic effect on the measured values of $R_{\theta JA}$. Therefore, unless test conditions are reported with the $R_{\theta JA}$ value, they should be considered suspect.

The measurement of $R_{\theta JA}$ is performed using the following steps (summarized from EIA/JESD51-1, -2, -5, -6, -7, and -9):

Step 1. A device, usually an integrated circuit (IC) package containing a thermal test chip that can both dissipate power and measure the maximum chip temperature, is mounted on a test board.

Step 2. The temperature sensing component of the test chip is calibrated.

Step 3. The package- and test-board system is placed in either a still air ($R_{\theta JA}$) or moving air ($R_{\theta JMA}$) environment.

Step 4. A known power is dissipated in the test chip.

Step 5. After steady state is reached, the junction temperature is measured.

Step 6. The difference in measured ambient temperature compared to the measured junction temperature is calculated and is divided by the dissipated power, giving a value for $R_{\theta JA}$ in °C/W.

1.1 Usage

Unfortunately, $R_{\theta JA}$ has often been used by system designers to estimate junction temperatures of their devices when used in their systems. The equation usually assumed to be valid for calculating junction temperature from $R_{\theta JA}$ is:

$$T_J = T_A + \left(R_{\theta JA} \times \text{Power}\right) \quad (1)$$

This is a misapplication of the $R_{\theta JA}$ thermal parameter because $R_{\theta JA}$ is a variable function of not just the package, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the part is mounted. In effect, the test board is a heat sink that is soldered to the leads of the device. Changing the design or configuration of the test board changes the efficiency of the heat sink and therefore the measured $R_{\theta JA}$. In fact, in still-air JEDEC-defined $R_{\theta JA}$ measurements, almost 70%–95% of the power generated by the chip is dissipated from the test board, not from the surfaces of the package. Because a system board rarely approximates the test coupon used to determine $R_{\theta JA}$, application of $R_{\theta JA}$ using Equation 1 results in extremely erroneous values.

Table 1 lists factors that can influence $R_{\theta JA}$ for a given package outline when all materials are held constant. The first column lists the factor while the second column gives a *rule of thumb* estimate as to the impact of the factor.

Table 1. Factors Affecting $R_{\theta JA}$ for a Given Package Outline

Factors Affecting $R_{\theta JA}$	Strength of Influence (rule of thumb)
PCB design	Strong (100%)
Chip or pad size	Strong (50%)
Internal package geometrical configuration	Strong (35%)
Altitude	Strong (18%)
External ambient temperature	Weak (7%)
Power dissipation	Weak (3%)

In light of the fact that $R_{\theta JA}$ is not a characteristic of the package by itself but of the package, PCB, and other environmental factors, it is best used as a comparison of package thermal performance between different companies. For example, if TI reports an $R_{\theta JA}$ of 40°C/W for a package compared to a competitor's value of 45°C/W, the TI part will likely run 10% cooler in an application than the competitor's part.

1.2 Test Card Impact

JEDEC has established a set of standards for measuring and reporting the thermal performance of IC packages. These standards fall under the EIA/JESD51 umbrella. EIAJ/Semi also has a set of thermal standards that are substantially different from the JEDEC version. $R_{\theta JA}$ is not a constant; therefore, it is critical to determine the standards that were used to calculate or measure $R_{\theta JA}$ before attempting a comparison.

Within the JEDEC specification, two test board types are allowed. A 1s (single signal layer) configuration gives a *typical* usage value for a moderately populated, multi-plane system-level PCB application. A 2s2p (double signal layer, double buried power plane) configuration gives a best case performance estimate assuming a sparsely populated, high-trace-density board design with buried power and ground planes. Figure 1 shows modeled $R_{\theta JA}$ differences for these two boards for 17 different package types. Note that all the materials and package geometries were held constant for these models.

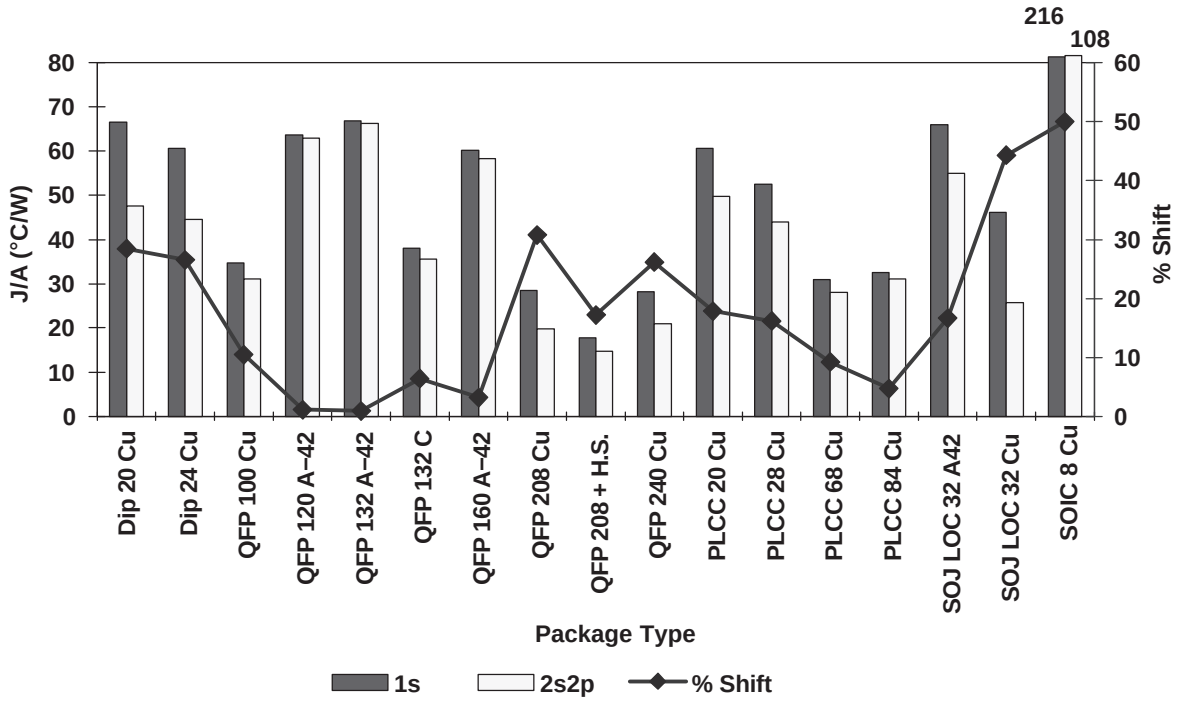

Figure 1. 1s vs 2s2p PCB for Various Packages

As shown, as much as a 50% $R_{\theta JA}$ variation can be expected as a function of 1s vs 2s2p test card construction alone.

1.3 Die Size Impact

The chip or die pad inside a package can perform the same function as a heat spreader if the chip or pad is large enough. The function of the heat spreader is twofold. First, it spreads energy from the hot spot of the chip over a wider area on the package surface, thereby increasing convective energy loss. Second, it increases heat transfer from the pad to the lead fingers or to the package balls, which then conduct the heat to the PCB. Figure 2 shows the impact of die size on $R_{\theta JA}$ for a tape-based area array chip scale package (CSP). As shown, the $R_{\theta JA}$ for this package changes almost 8× with die size. *It is important to re-measure or recalculate $R_{\theta JA}$ for a package if a die shrink is planned.*

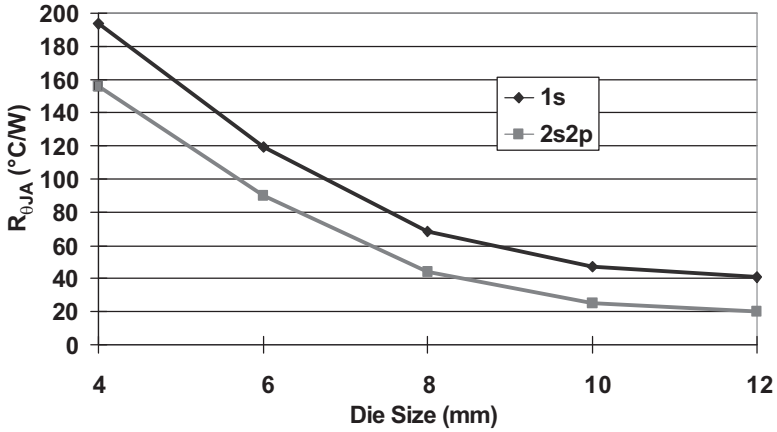

Figure 2. Die Size Impact on a CSP

1.4 Internal Package Geometrical Configuration

This topic refers to the layout within a package, be it a traditional lead frame package, small pad (S-pad) package, lead-on-chip (LOC), or ball grid array (BGA) package. More mundane geometrical configurations can also have a major impact on the package thermal performance. These can include the distance between the tips of the lead in the package and the die pad as shown in Figure 3, or even the downset between the pad and lead fingers. The latter is an especially important thermal criterion in thin packages. In BGAs, design of the interposer trace configuration is important in spreading heat from the die to the package balls where it is conducted into the PCB.

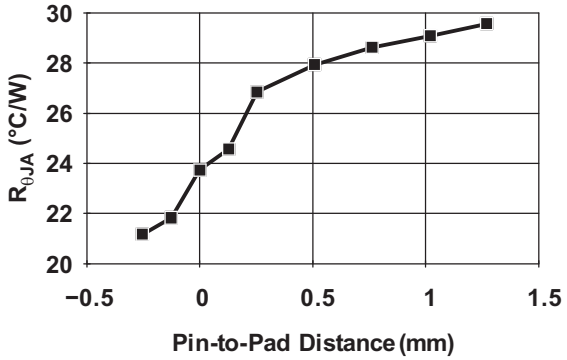

Figure 3. $R_{\theta JA}$ vs Pin-to-Pad Distance

1.5 Altitude

As the air pressure of the ambient environment changes with altitude, the cooling efficiency of the air also changes. IBM [1] showed that a device is expected to run 20% hotter at 8000 ft compared to the same device operating at sea level. Other investigators have shown large shifts in fan performance and internal chassis air flow when used at different altitudes. These effects should be considered, especially when the system design is marginal from a thermal standpoint. Many major system companies have pressure chambers that are used to test their systems at various effective altitudes. Usually, these companies instrument their designs to measure internal component temperatures when operating at different atmospheric pressures. Table 2 lists multiplication factors taken from the IBM work to derate $R_{\theta JA}$ values determined at sea level.

Table 2. Multiplication Factors

Altitude (ft)	Factor
0	1
3000	1.1
5000	1.14
7000	1.17
8350	1.2

1.6 Ambient Temperature

Ambient temperature has a great effect on convective and radiative heat transfer. Because thermal radiation varies with 4th power of temperature (T4), radiative heat transfer is significantly enhanced as temperature increases. On the contrary, convective heat transfer suffers with increasing temperature as the air is less dense at higher temperature. Generally, the effect of radiation is much higher than that of free convection. Experiments in the TI thermal lab show about a 10%–20% improvement in $R_{\theta JA}$ when measured between an ambient of 0°C–100°C; that is, $R_{\theta JA}$ at 100°C ambient is about 20% lower than the $R_{\theta JA}$ at 0°C ambient.

1.7 Power Dissipation

The surface temperature of the device drives both convection and radiation energy loss from the package. The hotter the package surface becomes, the more efficient convection and radiation heat loss to the ambient environment. Therefore, $R_{\theta JA}$ decreases with increasing power dissipation from a package. For very low power dissipation which results in minimal increase in surface temperature, $R_{\theta JA}$ is sometimes found to be 2×–3x higher than at rated package power levels.

1.8 $R_{\theta JA}$ Effective

Theta-ja ($R_{\theta JA}$) is a system-level parameter that depends strongly on system parameters as described in the previous sections; therefore, it is sometimes useful to define an $R_{\theta JA(effective)}$, which is simply the $R_{\theta JA}$ of the device operating in the system of interest. If $R_{\theta JA(effective)}$ can be estimated from thermal modeling or measurements in the system, it is possible to use Equation 1 to calculate the junction temperature assuming the power of the surrounding components on the system does not change. Equation 1 then becomes:

$$T_J = T_A + \left(R_{\theta JA(effective)} \times \text{Power} \right) \tag{2}$$

The system conditions leading to an $R_{\theta JA(effective)}$ value should always be defined when reporting $R_{\theta JA(effective)}$.

2 $R_{\theta JC}$ Junction-to-Case

The junction-to-case thermal resistance metric was originally devised to allow estimation of the thermal performance of a package when a heat sink was attached. EIA/JESD51-1 states that $R_{\theta JC}$ is, "the thermal resistance from the operating portion of a semiconductor device to outside surface of the package (case) closest to the chip mounting area when that same surface is properly heat sunk so as to minimize temperature variation across that surface." Though no current JEDEC specification is available defining $R_{\theta JC}$, a fairly universal industry practice exists for measuring $R_{\theta JC}$. This method is described in the following section. The SEMI Standard G43-87 describes a fluid immersion method for measuring $R_{\theta JC}$. Though TI has used this method in the past, it only has historical value and is not detailed here.

2.1 *Copper (Cu) Cold Plate $R_{\theta JC}$ Measurement*

This method forces almost all the power of the test device through a defined surface of the package. Depending on how a heat sink will be applied to the device, this may be the top or bottom of the package. Most generally, it is the top surface of the package. $R_{\theta JC}$ is good to determine the thermal resistance between the die and the surface onto which a heat sink is to be mounted.

Summarized, the procedure is:

Step 1. An IC package normally containing a thermal test chip is mounted on a test PCB. This is normally a JEDEC-defined low-k 1s0p PCB which has low copper content to minimize heat loss though the PCB.

Step 2. The package is pressure fit to a Cu cold plate (a copper block with circulating constant-temperature fluid) with the leads facing up and the case against the cold plate when the top of the case is to be measured. Otherwise, a Cu cold plate contact to the bottom of the package is provided through the PCB when the primary cooling path of the package is through a soldered plate into the PCB.

Step 3. Silicone thermal grease or other thermal interface material provides thermal coupling between the cold plate and package.

Step 4. Insulation is provided around the test coupon to minimize parasitic heat loss.

Step 5. Power is applied to the device.

Step 6. The junction temperature of the test chip is measured.

Step 7. The temperature of the package surface in contact with the cold plate is measured by a thermocouple or other temperature sensor pressed against this surface.

Step 8. $R_{\theta JC}$ is calculated by dividing the measured temperature delta by the dissipated power.

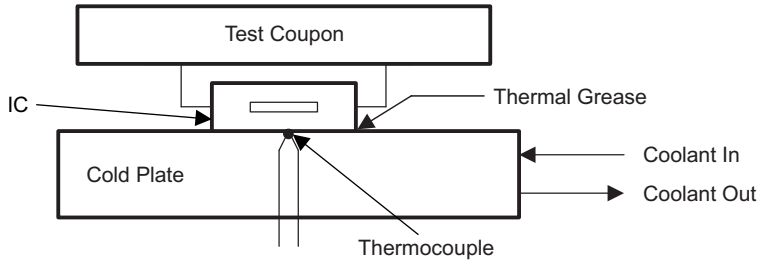

Figure 4. Cu Cold Plate Measurement Process

2.2 *$R_{\theta JC}$ Application*

The old and obsolete understanding of $R_{\theta JC}$ is shown in Equation 3.

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad (3)$$

Here, the package thermal performance $R_{\theta JA}$ is reported to be the sum of two resistances: $R_{\theta JC}$ and $R_{\theta CA}$. $R_{\theta CA}$ stands for the case-to-ambient thermal resistance, which was defined by this equation. This might have been a valid equation for packages with metal cans, which were relatively at a constant temperature and were not thermally coupled to the PCB. But, these conditions do not apply with today's plastic or ceramic packages that are tightly coupled to the PCB. Large thermal gradients are common across modern packages, so the meaning of Equation 3 is questionable.

A traditional, but invalid, usage of $R_{\theta JC}$ is to calculate the junction temperatures of chips operating in a system. Case temperatures of devices operating in the system are measured using thermocouples, IR cameras, or Fluoroptic® probes. Equation 4 is then mistakenly used to calculate the junction temperature: Equation 4:

$$T_J = T_C + \left(R_{\theta JC} \times \text{Power}\right) \tag{4}$$

The fallacy here is that only a very small percentage of heat energy in a typical plastic package is convected and radiated off the top surface of the package. Many models have shown 60%-95% of thermal energy from a chip is actually convected and radiated off the PCB to which the package is attached. If one assumes the entire power is dissipated by the top surface, the junction temperature calculated by Equation 4 is higher than reality. In designs with thermal margin, this is a nuisance, but in designs without thermal margin, erroneous limitations might be imposed. This limitation of $R_{\theta JC}$ is overcome by the new thermal metric, Ψ_{JT}, which is described below.

Equation 5 shows the proper application of $R_{\theta JC}$ for those instances when a high-efficiency heat sink is applied to the top surface of a device for which $R_{\theta JC}$ is small compared to $R_{\theta JA}$:

$$T_J \cong T_A + \left(\left(R_{\theta JC} + R_{\theta(CS)} + R_{\theta(SA)}\right) \times \text{Power}\right) \tag{5}$$

Here, $R_{\theta(SA)}$ is the heat sink-to-ambient performance of the heat sink and $R_{\theta(CS)}$ is the case-to-heat sink thermal resistance of the thermal interface material (see Equation 7). The ambient temperature is at the location used for characterizing $R_{\theta(SA)}$, usually some distance away from the heat sink. This equation is the most accurate for packages where $R_{\theta JC}$ is small compared to $R_{\theta JA}$, meaning that most of the heat can be dissipated through the top surface of the package when a sufficiently efficient heat sink is applied.

Equation 6 shows an approximation that is more accurate than Equation 5 for any combination of $R_{\theta JA}$, $R_{\theta JC}$, or $R_{\theta(SA)}$ if $R_{\theta JA}$ is known for the system configuration:

$$T_J \cong T_A + \left(\frac{R_{\theta JA} \times \left(R_{\theta JC} + R_{\theta(CS)} + R_{\theta(SA)}\right)}{R_{\theta JA} + R_{\theta JC} + R_{\theta(CS)} + R_{\theta(SA)}}\right) \times \text{Power} \tag{6}$$

2.3 $R_{\theta(CS)}$

The best method for calculating $R_{\theta(CS)}$ is to actually measure the $R_{\theta(CS)}$ value, but if this is not possible, Equation 7 can be used to estimate $R_{\theta(CS)}$. Note that this is merely an estimate, because the thermal interfacial resistance that can be developed between any two surfaces is neglected.

$$R_{\theta(CS)} = \frac{T}{k \times A} \tag{7}$$

where:

- T = The thickness of interface layer between package and heat sink
- k = The bulk thermal conductivity of the thermal interface material
- A = The area over which the thermal interface material is applied

2.4 $R_{\theta JC(top)}$ and $R_{\theta JC(bot)}$

Some packages have mechanisms such as heat slugs or exposed pads to remove heat from the top, bottom, or both surfaces of the package. When only a single surface is used for heat removal, this is the surface that would be used for $R_{\theta JC}$ based on the EIA/JESD51-1 specification. Sometimes, designers wish also to include heat sinks on the top of the package, even if the exposed pads are soldered to the PCB. In such instances, it is appropriate to define $R_{\theta JC(top)}$ and $R_{\theta JC(bot)}$ to avoid confusion over which surface is

being referenced. The top surface is the surface of the package facing away from the PCB, whereas the bottom surface is the surface of the package facing toward the PCB. When $R_{\theta JC(bot)}$ is to be measured, a special PCB is constructed with a cutout to allow contact between the bottom package surface and Cu cold plate. When in contact with the Cu cold plate, the temperature taken at the bottom surface of the package becomes the case temperature that is used in calculating the temperature delta between the case and junction temperature.

It should be noted that Texas Instruments has at times used the nomenclature of $R_{\theta(JP)}$, or junction-to-pad, to refer to the thermal resistance between the junction and exposed pad of the package. This nomenclature has been used regardless of whether the pad was exposed on the top or bottom of the package.

3 Ψ_{JT}, Junction to Top of Package

In an attempt to provide the user community with a thermal metric to estimate in-use junction temperatures from measured case temperatures, a new thermal metric, Ψ_{JT}, has been adopted by the industry (JESD51-2). The metric is defined by the Greek character psi (Ψ) rather than theta (θ) because Ψ_{JT} is not a true thermal resistance.

The measurement procedure for Ψ_{JT} is summarized from JESD 51-2 as follows:

Step 1. Mount a test package, usually containing a thermal test die, on a test board.

Step 2. Glue a fine gauge thermocouple wire (36 gauge or smaller) to top center of package.

Step 3. Dress the thermocouple wire along package to minimize heat sinking nature of thermocouple.

Step 4. Dissipate power in test die.

Step 5. Measure the test die junction temperature and thermocouple temperature.

Step 6. Divide the thermal gradient between the junction temperature and surface temperature by the dissipated power.

Why is Ψ_{JT} not a true thermal resistance? In the above procedure, the heat energy generated by the test die is allowed to flow normally along preferential thermal conduction paths. The quantity of heat flowing from the die to the top of the package is actually unknown in the measurement, but is assumed to be the total power of the device for the purposes of Ψ_{JT} calculation. Clearly, this assumption is invalid, but when calculated this way, Ψ_{JT} becomes a very useful number because the experimental configuration is much like the application environment of the IC package. As such, the amount of energy flowing from the die to the top of the package during test is similar to the partitioning of the energy flow in an application environment. In comparison to Equation 4, the actual junction temperature can be very closely estimated using Equation 8:

$$T_J = T_C + \left(\Psi_{JT} \times \text{Power}\right) \tag{8}$$

For plastic packages, Ψ_{JT} is typically 0.5°C/W–2°C/W compared to $R_{\theta JC}$ values of 4°C/W–15°C/W. Thinner packages have smaller Ψ_{JT} values than thicker packages. Packages with embedded heat slugs have Ψ_{JT} values close to zero. You should be aware that Ψ_{JT} varies with both board construction and air flow conditions as shown in Table 3. The values in Table 3 were obtained through modeling.

Table 3. Ψ_{JT} for Typical 128-Pin TQFP Package(1)(2)(3)(4)(5)(6)(7)(8)

DIE PAD	PCB TYPE(9)	AIR FLOW (LFM)	Ψ_{JT}
Exposed	1s0p	0	0.22
Exposed(10)	2s2p	0	0.09
Non-exposed	1s0p(11)	0	0.13
Non-exposed	2s2p(11)	0	0.09
Exposed	1s0p	250	0.47
Exposed	2s2p	250	0.18
Non-exposed	1s0p	250	0.31
Non-exposed	2s2p	250	0.23

(1) Size, type, pin: 14 mm × 14 mm × 1.1 mm, TQFP, 128
(2) Die size: 8.4 mm × 8.3 mm
(3) Die thickness: 0.31 mm for exposed pad; 0.28 mm for non-exposed
(4) Die pad size: 10.5 mm × 9.2 mm × 0.15 mm
(5) Die attach impedance: 5.77°C-mm^2/W
(6) Mold compound thermal conductivity: 0.9 W/m-K
(7) Ambient temperature: 25°C
(8) Power dissipation: 1 W
(9) Size: 114.3 mm × 76.2 mm × 1.6 mm
(10) Thermal vias: 9 × 9 connecting die pad to ground plane (only for 2s2p PCB with exposed pad)
(11) Type: JEDEC high-k (2s2p) and low-k (1s0p) as defined in JESD 51-7 and JESD 51-3, respectively

3.1 Case Temperature Measurement

The case temperature is defined as the hottest temperature on the top of the device. In most instances, this is at the center of the top surface or lid of the device. The case temperature measurement can be performed with (in order of accuracy) an IR camera, a fluor-optic probe, a thermocouple, or IR gun with a maximum field view of 4-mm diameter just to name a few techniques. When a thermocouple is chosen as the technique to perform the measurement, a fine gauge wire (36 to 40 gauge, J or K wire) should be used to minimize the local cooling from the thermocouple. You should be aware that if the case temperature is measured by a gauge thermocouple larger than 36, the thermocouple sinks heat away from the surface, cooling the spot that is being measured, invalidating the calculation of Equation 8. The impact of using a heavy-gauge thermocouple to measure the package top surface can be very substantial, reducing the delta between the ambient and actual surface temperature by 50% or more. There can be error even when a 36 gauge or smaller thermocouple is employed.

If using a thermocouple, it should be attached to the center of the package surface (± 1 mm) with a bead of thermally conductive epoxy no larger than 2 × 2 mm on a side. Taping the thermocouple to the package surface is not recommended. To minimize the heat sinking nature of the thermocouple, the wire should be dressed along the diagonal of the package, down to the PCB surface, and over a minimum distance of 25 mm before lifting from the PCB. The thermocouple wire can be tacked to the PCB for this routing purpose by using a tape. Use of improper thermocouple wire gauge can create errors in the measurements of 5%–50%.

When using either an IR camera or IR gun, be sure to correct the reading for the emissivity of the surface being investigated. For details, see the documentation for the instrument being used.

Measuring case temperatures with heat sinks applied represents special challenges because the heat sink covers the surface to be measured. If you wish to measure the case temperature with a heat sink applied, the following procedure is recommended (see Figure 5).

Step 1. Drill a hole less than 1 mm in diameter in the heat sink so the hole is at the center of the package when the heat sink is attached. Chamfer the end of the hole on the face of the heat sink that mates with the package. The chamfer should be sized to accommodate the epoxy that will attach the thermocouple to the package.

Step 2. Thread a fine-gauge (less than 36-gauge) thermocouple through the drilled hole from the top of the heat sink.

Step 3. Use epoxy to attach the thermocouple bead to the package top surface with thermocouple wire oriented perpendicular to the package top surface. Wait for the epoxy to cure.

Step 4. Apply heat sink compound to the base of the heat sink.

Step 5. With the thermocouple wire still threaded through the drill hole, carefully slide the heat sink onto the top of the package.

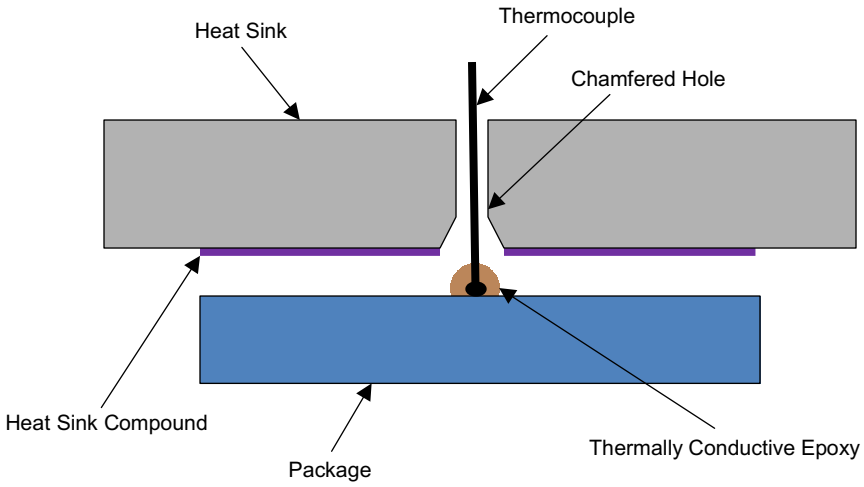

Figure 5. Installing a Heat Sink With Thermocouple

3.2 Ψ_{JT} vs $R_{\theta JC}$ When Using Heat Sinks

Ψ_{JT} should not be used when application of a heat sink is intended. Instead, Equation 5 and Equation 6 should be used.

4 $R_{\theta(JB)}$ Junction-To-Board

The junction-to-board thermal resistance, or junction-to-pin thermal resistance, attempts to represent the thermal resistance between the package and the board with one number. In reality, the resistance between the junction and board is distributed, with different resistance paths such as the junction-to-pin-to-board and the junction-through-plastic-through-air-to-board. Furthermore, the concept of $R_{\theta JB}$ implies that the board temperature under the device is uniform temperature (single node), which is erroneous. Nevertheless, a single thermal metric like $R_{\theta(JB)}$ is useful for a first-pass estimation of junction temperature based on the following simple three-resistor thermal approximation as shown in Figure 6. In this model, the resistance from the junction-to-board is simply the $R_{\theta(JB)}$ value. The resistance between the junction and case surface is simply the $R_{\theta JC}$ value. The ambient resistance, $R_{\theta(a)}$, is calculated from the convective heat loss and radiation loss from the top of the package.

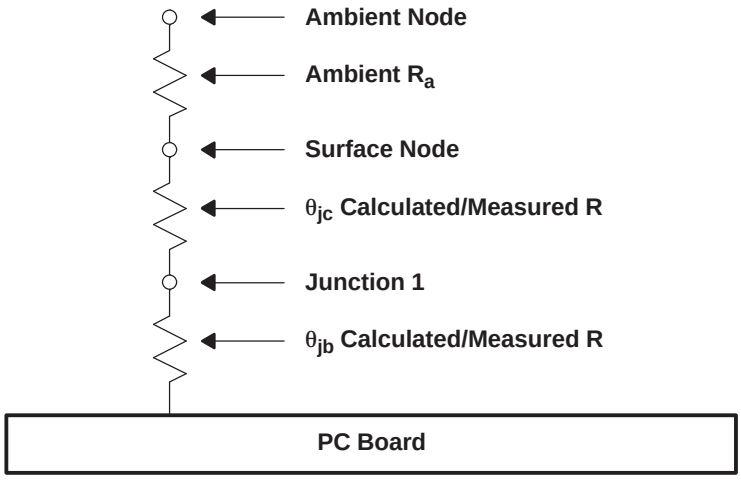

Figure 6. Three-Resistor Thermal Approximation Model

4.1 $R_{\theta(JB)}$ Measurement Method

The primary method to measure $R_{\theta(JB)}$ is as follows:

Step 1. A test package containing a thermal test die is mounted on a test board.

Step 2. A fine wire thermocouple (36–40 gauge) is glued or soldered to the device pin closest to the die. In the case of BGA packages, the thermocouple is soldered or glued to the trace exiting from under the package edge that is closest to the die.

Step 3. The board is clamped in a special double cold plate fixture with insulation between the package and the cold plate surfaces, but with thermal contact between the cold plate and the board. The cold plate heat sinks the PCB.

Step 4. Power is dissipated in the die.

Step 5. The temperatures of the die and pin are monitored.

Step 6. When steady state is achieved, the delta between the junction and pin temperatures is divided by the total power dissipated.

This procedure is defined more precisely in JESD 51-8.

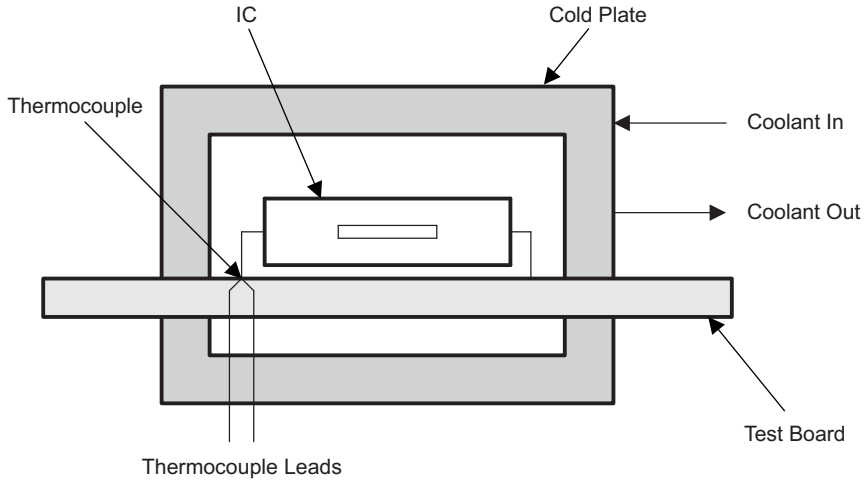

Figure 7. $R_{\theta(JB)}$ Measurement Method

5 Ψ_{JB} Junction-to-Board Characterization Parameter

Ψ_{JB} is very similar to Ψ_{JT} in concept. It refers to the measurement of the difference between the junction temperature and the center package pin temperature, divided by the power dissipation of the device. As such, it is not a true thermal resistance because the actual partitioning of power through this thermal resistance is unknown.

5.1 Ψ_{JB} Application

Ψ_{JB} can allow the system designer to measure the board temperature with a fine gauge thermocouple and back-calculate the junction temperature using Equation 9. Note that Ψ_{JB} is close to $R_{\theta(JB)}$, as the PCB dissipates 75%–95% of the heat of a device.

$$T_J = T_{(PCB)} + (\Psi_{JB} \times \text{Power}) \tag{9}$$

Measurement of Ψ_{JB} is defined by JESD51-6. Care should be taken with the selection of the thermocouple type, gauge and dressing of the thermocouple across the PCB in a similar fashion to the thermocouple intended to measure case temperature for Ψ_{JT} measurements. As with Ψ_{JT} measurements, an IR camera or fiber optic probe can be used to measure the PCB temperature. However, an IR thermal gun is not appropriate due to the small spot size to be imaged.

6 Industrial and Commercial Temperature Ranges

Texas Instrument devices marked *Industrial Temperature Range* function at ambient temperatures between –40°C and 85°C when proper care is taken to ensure that the absolute maximum operating temperatures are not exceeded. Note that system-level thermal design is required to ensure that the maximum operating device temperatures are not exceeded even when the input ambient air temperature is between –40°C and 85°C. The minimum operating temperature is –40°C when the industrial temperature range is specified. There is no industry standard defining the meaning of industrial temperature capable, so variations will likely exist from company to company.

Texas Instrument devices marked *Commercial Temperature Range* function at ambient temperatures between 0°C and 70°C when proper care is taken to ensure the absolute maximum operating temperatures are not exceeded. The minimum operating temperature is 0°C when the commercial temperature range is specified.

7 Miscellaneous Definitions

Absolute Maximum Junction Temperature— The temperature beyond which damage occurs to the device. The device may not function or meet expected performance at this temperature.

Absolute Maximum Operating Temperature— The maximum junction temperature at which the device functions electrically. The lifetime of the device is reduced if the device operates continually at this temperature. Another wording sometimes used is Maximum Operating Temperature.

Ambient Air Temperature— Multiple sources list different locations for determining the ambient air temperature. NEBS specifies the air temperature coming into the system box as ambient. AEC specifies the air temperature under the device as the ambient. JEDEC specifies the air stream temperature in advance of the PCB. Sometimes the ambient air temperature is taken above the device as an understanding of ambient. Each of these measurement locations yields a different temperature for the ambient air temperature. It is important to understand, in any case, that the critical factor affecting device reliability and functionality is the junction temperature, not the ambient temperature. Because the junction temperature and ambient temperature are interrelated, clarification of the ambient temperature assumption is crucial before any system level analysis is undertaken.

Junction Temperature— The hottest temperature of the silicon chip inside the package.

Maximum Case Temperature— Sometimes, rather than specifying Maximum Operating Temperature, a maximum case temperature is given. Running the device at the maximum case temperature (without a heat sink) results in the die running at the Recommended Operating Junction Temperature. Sometimes, this is written as T_C. T_C is normally measured at the center of the package top-side surface.

Recommended Operating Temperature —The junction temperature at which the device operates continuously at the designated performance over the designed lifetime. The reliability of the device may be degraded if the device operates above this temperature. Some devices will not function electrically above this temperature. Another wording sometimes used is Recommended Continuous Operating Junction Temperature.

8 References

1. Mansuria, Proceedings of the 1994 International Electronics Packaging Conference, IEPS, San Diego, CA, September 1994, pp 122-130
2. Rosten, H., 1996, ‘‘DELPHI—A Status Report on the European-funded Project for the Development of Libraries and Physical Models for an Integrated Design Environment,’’ Proc. of 46th Electronic Components & Technology Conference, pp. 172–185.
3. EIA/JESD51-1, *Integrated Circuits Thermal Measurement Method – Electrical Test Method (Single Semiconductor Device)*
4. JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions – Natural Convection (Still Air)*.
5. JESD51-5, *Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment*

Mechanisms

6. JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions – Forced Convection (Moving Air)*
7. JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
8. JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from B Revision (July 2012) to C Revision	Page
• Added pertinent JEDEC specifications	2
• Changed Y-axis label of Figure 2	4
• Changed Y-axis label and caption of Figure 3	4
• Changed partial pressure to atmospheric pressure	5
• Changed test of Section 1.6	5
• Changed text of Section 1.7.	5
• Updates were made to Section 1.8.	5
• Updates were made to Section 2.2.	6
• Corrected specification reference from JEDEC JC51.1 to EIA/JESD51-1	7
• Changed the procedure for measuring case temperature	9

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