

## Failure Modes in Wire bonded and Flip Chip Packages

**Mumtaz Y. Bora**

Peregrine Semiconductor

San Diego, Ca. 92121

[mbora@psemi.com](mailto:mbora@psemi.com)

### Abstract

The growth of portable and wireless products is driving the miniaturization of packages resulting in the development of many types of thin form factor packages and cost effective assembly processes. Wire bonded packages using conventional copper lead frame have been used in industry for quite some time. However, the demand for consumer electronics is driving the need for flip chip interconnects as these packages shorten the signals, reduce inductance and improve functionality as compared to the wire bonded packages. The flip chip packages have solder bumps as interconnects instead of wire bonds and typically use an interposer or organic substrate instead of a metal lead frame.

The integration of these packages in high volume SMT assembly demands good assembly process controls at the package level and clear understanding of the failure modes to minimize defect escape to subsequent assembly operations. This challenge is enhanced with the transition to lead free reflow as the higher peak reflow temperatures results in more thermal and CTE mismatch between package and PWB.[1]

The paper provides a general overview of typical defects and failure modes seen in package assembly and reviews the efforts needed to understand new failure modes during package assembly. The root cause evaluations and lessons learned as the factory transitioned to thin form factor packages are shared.

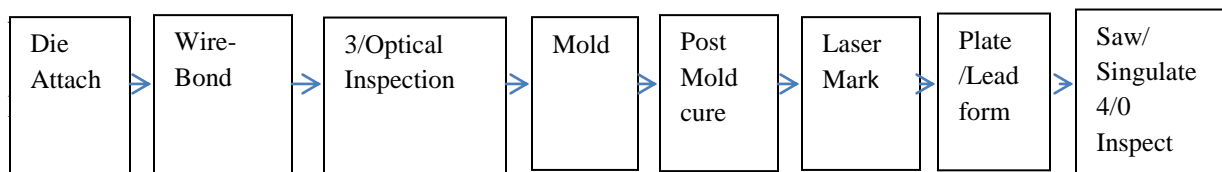
### Introduction

Wire bonded and Flip chip interconnects are in demand for consumer electronics due to reduced circuit geometries and increased wiring density. Reliability of these packages in high volume SMT assembly production requires careful selection of assembly materials and processes such as die attach epoxy, overmold /under fill material s and carefully controlled reflow profiles. Tighter storage and handling controls of components and processes are necessary for good yields and reliability due to the narrow process windows for lead free reflow.

The paper summarizes the typical defects and failure modes seen in manufacturing of thin form factor packages, understanding of the root cause, corrective actions and lessons learned in high volume subcontract assembly operations.

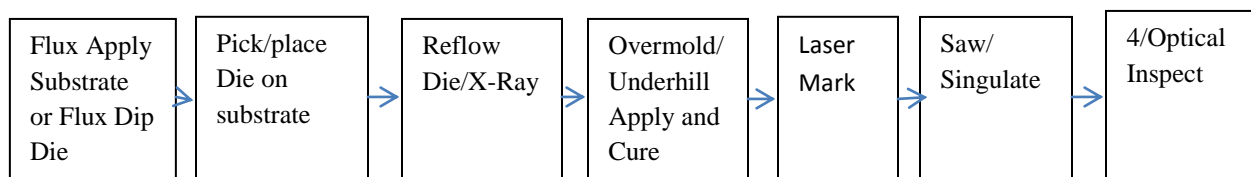
### Overview of Assembly Process Flow

Wire bonded and flip chip assembly has a unique process flow and material set to provide optimum yield. Wire bond assembly operations are separated as front end of line (FOL) and back end of line (BOL). FOL includes die attach, wirebond and 3<sup>rd</sup> Optical inspection. EOL includes mold, cure, mark, plate and singulation processes as shown in Figure 1



**Figure 1 Wire Bond Assembly (Metal leadframe, gold wire)**

Flip chip Assembly operations are separated as FOL- front end of line, EOL back end of line. FOL includes die place reflow and 3<sup>rd</sup> Optical inspection. EOL includes mold, cure, mark, and singulation processes as shown in Figure 2



**Figure 2 Flip Chip Assembly- (Organic substrate, solder/copper bumps)**

After completing assembly, packages go through Test, Tape and Reel and are then packaged for shipment.

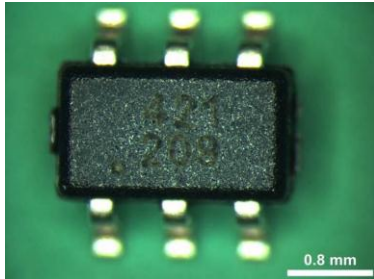
### Defects and failure mode evaluation

The package manufacturing process has a variety of materials and processes used to make the end product. There can be many sources of defects if materials and processes are not controlled adequately. One key defect prevention tool used in the early engineering stages is DFMEA ( Design Failure Modes and Effects analysis) and PFMEA ( Process Failure Modes and Effects Analysis) to predict the risks in design and process and put controls in place to minimize defects[2]

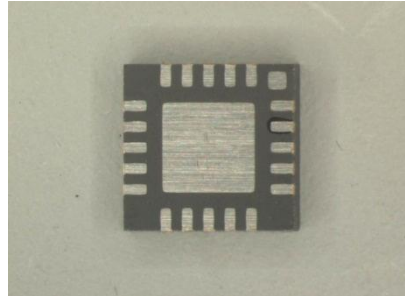
The migration to thin form factor packages requires more focus on handling controls, moisture sensitivity classifications,[3], material shelf life and tighter process windows.

### Wire Bond Packages

Wire bonded packages come in both versions, leaded and leadless(QFN) . As shown in Figure 3 and Figure 4



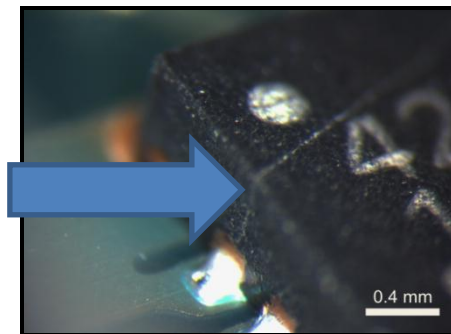
**Figure 3 Leaded Package**



**Figure 4 Leadless package**

Both packages are made using wirebonded copper leadframes. The external termination plating is 100% matte tin or NiPdAu to meet RoHS requirements.. The typical failure modes seen are delamination, plating cracks, burrs, contamination , corrosion of wire bond pads and mold compound cracks.

The migration to thin form factor packages requires more focus on handling controls, material shelf life and tighter process windows. One such issue can be seen with higher incidence of mold compound cracks as we migrate from 1 mm thick package to 0.7 and 0.5 mm thick packages as shown in Figure 5.



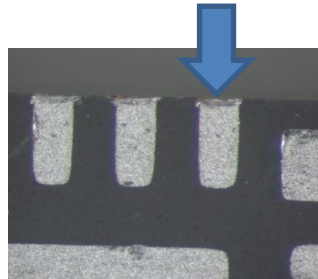
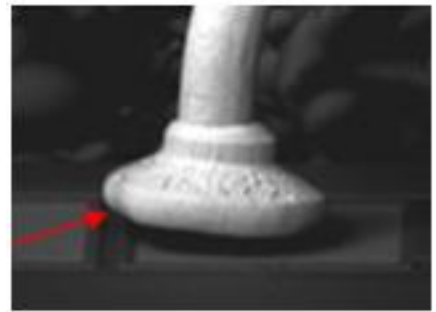
**Figure 5- Mold Compound Crack**

Damage to packages can be eliminated by switching to automated fixtures for depaneling and singulation and reducing manual handling. Designed experiments were conducted to define new process windows for sawing and blade wear followed by training for inspection and handling

Burrs, scratches and tooling marks on packages can impact assembly yields due to solder wetting issues. Burrs should be measured and controlled within 0.05 mm as shown in the Table 1 and Figure 6

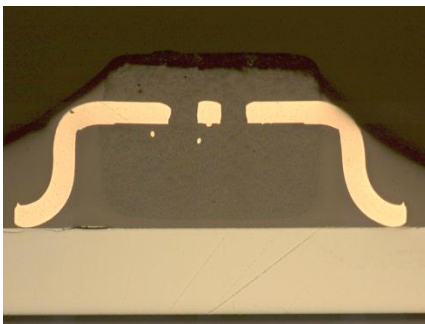
### Table 1 –Package Dimensional Analysis

Package Dimensional Analysis			
Item	LSL	USL	Mean
Package Thickness	0.8 mm	0.9 mm	0.864mm
Package Dimension-X	3.95 mm	4.05 mm	4.003mm
Package Dimension-Y	3.95 mm	4.05 mm	3.990 mm
Lead Length	0.500 mm	0.600 mm	0.549 mm
Saw Burr	0.000 mm	0.050 mm	0.021 mm
Side Smear	0.000 mm	0.135 mm	0.046 mm

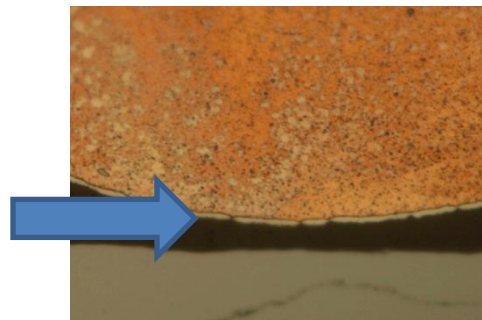


**Figure 6 - Burrs**

For leaded packages, plating cracks can occur during lead form in the “knee” area of the form. With the migration to finer SMT pitch and narrow lead widths, tighter process controls are required for forming process. Cracked, insufficient or missing plating can be a solderability and reliability issue. Figure 7 and 8 show the lead with NiPdAu plating.

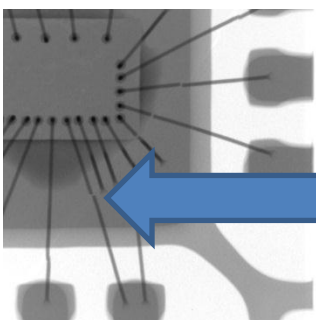


**Figure 7 NiPdAu plated lead**



**Figure 8 Voids in Ni Plating**

Wire bonding process is the key driver of the package assembly yields. Proper optimization and process window development for wire bonding is essential to minimize nonstick on pad, lifted or broken wire bonds. The proper bond pad cleanliness also contributes to reliable wire bonds. Figure 9 shows a broken wire bond and Figure 10 shows a lifted wire bond



**Figure 9 Broken Wire bond**

**Figure 10 Lifted Wire Bond**

## Flip Chip Packages

The flip chip package assembly yields are very dependent on proper bump alignment, reflow and molding process. The laminate substrate material, surface finish, and CTE play a key role in the reliability of the package. Successful assembly of the package requires proper bump alignment and intermetallic formation at package /die interface and bump/substrate interface as shown in Figure 11 and Figure 12. The laminate pad geometry and solder mask windows optimization is critical for proper joint formation. The glass transition temperature of the laminate, and its CTE (Coefficient of thermal expansion) and warpage characteristics can have an impact on bump reliability. Additionally, reflow profiles need to be optimized to provide adequate solder reflow without causing delamination of the substrate.

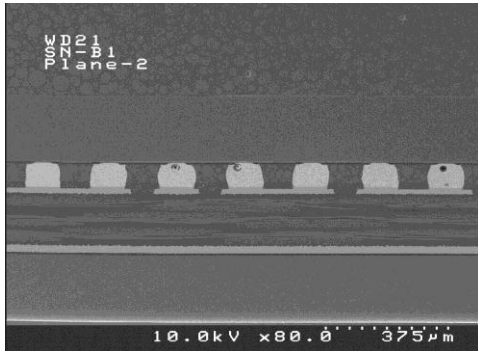


Figure 11- Flip chip solder bumps

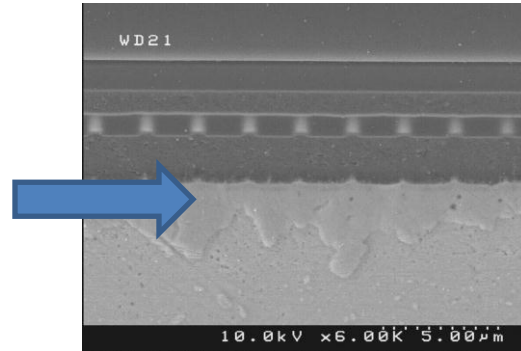


Figure 12 Intermetallic die/package

Copper studs are another form of bump interconnects used for fine pitch flip chip packages.

Proper pad to bump alignment is more critical for a copper stud bump as it does not have the self-centering that a solder bump has. CTE mismatch between substrate and die can have significant impact on copper bump reliability. [4]. Figure 13 shows an acceptable joint using copper interconnect and Figure 14 shows a crack in a copper bump interconnect.



Figure 13 – Reflowed Copper Bump

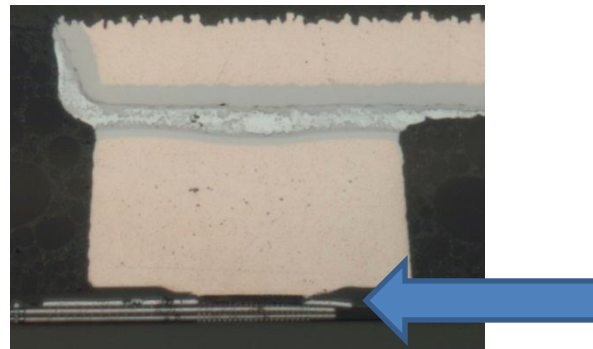


Figure 14- Copper bump Crack

X-sectioning is conducted post reflow to understand the solder joint profile, alignment, presence or absence of voids and to evaluate the grain structure of the solder joint. Voids can get trapped at the bump to substrate interface and cause assembly issues. Generally acceptable criteria for voids are less than 30% of the bump diameter.

Switching to a low voiding solder paste can help minimize the void issue. An alternate to bumping with solder paste is a solder ball drop process which has minimal void issues. [5]

X- Sectional analysis also helps evaluate the package molding process to ensure that there is proper coverage of the mold compound around the bumps and minimal voiding. Low pin count packages are typically over molded and survive the package level reliability tests. Higher pin counts packages require under fill apply and cure post reflow. Careful evaluation of under filled packages is required to ensure that there is no solder extrusion in the under fill during the cure process. Other failure modes that can be seen in X-sectional and SEM/EDX analysis are UBM (under bump metallurgy) separation from solder bump, passivation cracking, bump corrosion, pad separation etc.

## Root Cause Analysis

The variety of defects discussed earlier in flip chip and wire bonded packages require a thorough follow up with production line records, controls, training and documentation. Typical causes of cosmetic and functional defects are optimized processes, handling damage, ESD controls, operator turnover, training, material controls etc. Some of the defects are not exposed during qualification process and surface later on when machines and processes are fully utilized for production ramp. To minimize this defect escape a detailed package construction analysis is conducted prior to qualification approval. This allows time to isolate defects and drive corrective action and conduct process window optimization before launching production.

For wire bonded packages, die attach, ball bonds, wedge bonds and package molding are evaluated using an X-section. Figure 15 shows the package wire bonds and Figure 16 shows the package mold compound.

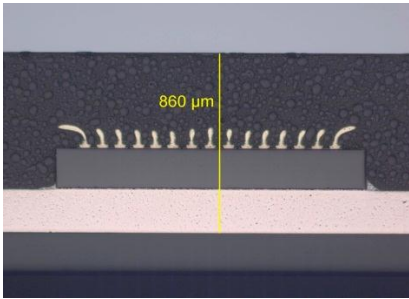


Figure 15 Ball Bonds

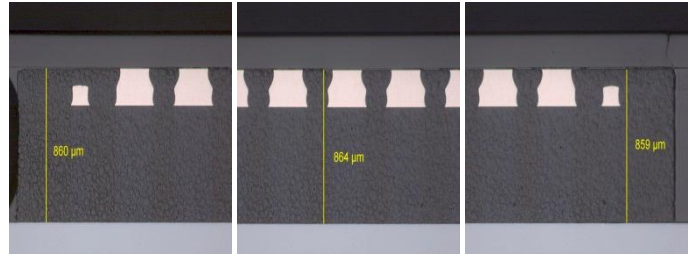


Figure 16 Package leads and Mold compound

Wirebond reliability is critical for the success of the package in assembly processes and subsequent customer applications. Proper intermetallic formation and shear values >25 gms, and minimal voiding are expected post wire bond. Figure 17 shows the intermetallic formation in Agold to Aluminum wire bond. Figure 18 shows a wedge bond made on the lead. Lifted wedge bonds can be prevented by optimizing the bond parameter recipes and maintaining a clean bond surface.

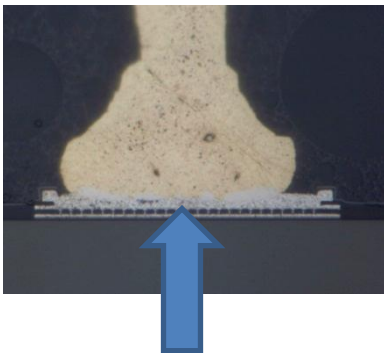


Figure 17 - IMC(intermetallics)

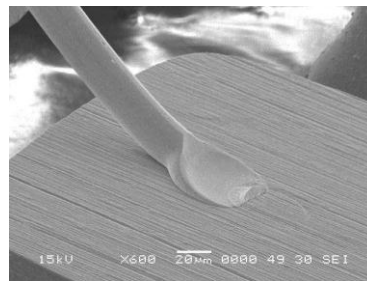


Figure 18 - Wedge Bond

X-sectional analysis is also conducted for flip chip package to understand the package and die thickness, laminate, vias, bump height, voids, intermetallics etc. Figure 19 shows an X-section of a flip chip package.

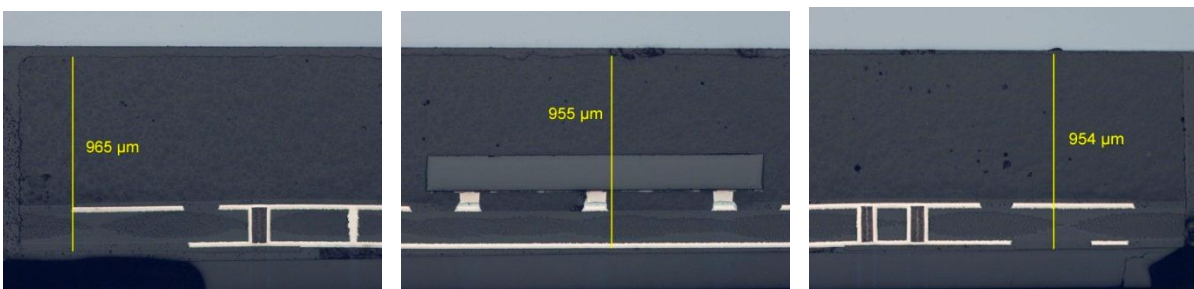


Figure 19- X-section Flip chip package

The controls on the production floor or at a subcontract operation need to be reviewed frequently to minimize defect occurrence and escape. When a failure mode is understood and corrected, the FMEAS and control plans should be updated to reflect the changes and the "lessons learned". Yield targets and yield improvement plan should be defined prior to production launch.

and reviewed on an ongoing basis. Yield data review using top 3 yield detractors by part number is helpful in DPPM reduction efforts. Manufacturing line audits and training review and refresher are also a means for continuous improvement. Monitoring Cp/Cpk for each critical process and 10- 15 production lots after launch provides an effective source of issues to focus for continuous process improvement and optimization.

**Conclusion:**

Wire bonded and flip chip bumped interconnects are a reliable form of interconnect if bond parameters, reflow process, mold material sets, substrate pads and solder mask are optimized. Successful assembly and reliability of these packages can be achieved with careful understanding of failure modes, clear, concise documentation, training and teamwork with subcontract facilities.

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