UCC3819 250-W Power Factor Corrected (PFC) Boost Follower Preregulator Design

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ABSTRACT

This paper reviews the benefits of a boost follower topology and the design of a 250-W PFC boost follower preregulator.

Contents

1 Introduction

Conventionally PFC off-line power converters are designed with two power stages. The first stage is typically a boost converter. This is because the boost converter topology has continuous input current that can be shaped through the use of a multiplier and average current mode control to achieve near-unity power factor (PF). However the boost converter requires a higher output voltage than the input and requires a second converter to step this voltage down to a useable level.

The boost converter is traditionally designed to have a fixed output voltage greater than the maximum peak line voltage. However, the boost voltage does not have to be well regulated or fixed because the step down converter can be designed to handle the variations in voltage. As long as the boost voltage is above the peak input voltage the converter will regulate properly. There are actually some benefits that can be gained by having the boost voltage vary with variations in peak line voltage (i.e. boost follower preregulator). One is reduced inductor size and the other is lower switch loss at low line operation. This paper reviews the benefits of a boost follower topology and the design of a 250-W PFC boost follower preregulator.

NOTE: The reference design was generated using typical parameters rather than worst-case values. Please refer to the table in Figure 1 and Figure 2 for design specifications and component placement. Refer to Table 1 for all variable definitions.

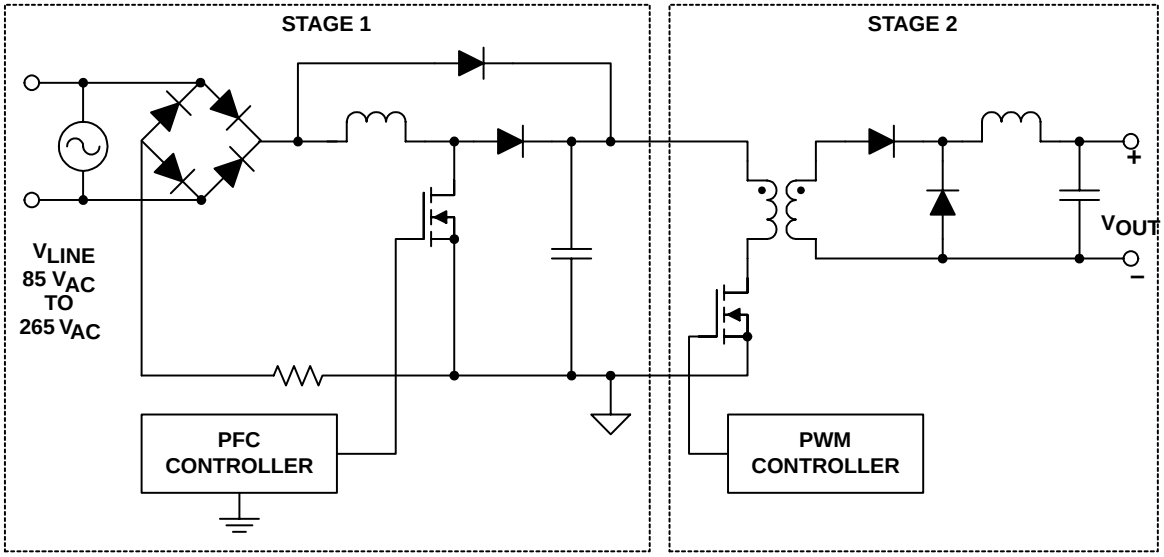


Figure 1. Functional Block Diagram

Table 1. Design Specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN}	Input offset voltage		85		265	V_{RMS}
f_{IN}	Input frequency			60		Hz
V_{OUT} dc	Output voltage	V_{IN} = 85 V_{RMS}	195	205	215	V
		V_{IN} = 265 V_{RMS}	370	390	410	
P_{OUT}	Output power		0		250	W
V_{RIPPLE}	Output voltage ripple	V_{IN} = 85 V_{RMS}			3%	
η	Efficiency	P_{OUT} = 250 W	93%			
THD	Total harmonic distortion	V_{IN} = 85 V_{RMS}, P_{OUT} = 250 W			5%	
		V_{IN} = 265 V_{RMS}, P_{OUT} = 250 W			7%	
f_{OSC}	Operating frequency			100		kHz
t_{HOLDUP}	Hold-up time		16.7			ms
V_{OVP}	Overvoltage protection threshold voltage	V_{OUT} = 400 V	409	416	422	V
P_{LIM}	Power limit	V_{IN} = 85 V_{RMS}	275	360	385	W
I_{LIM}	Peak current limit		5.335	5.500	5.665	A

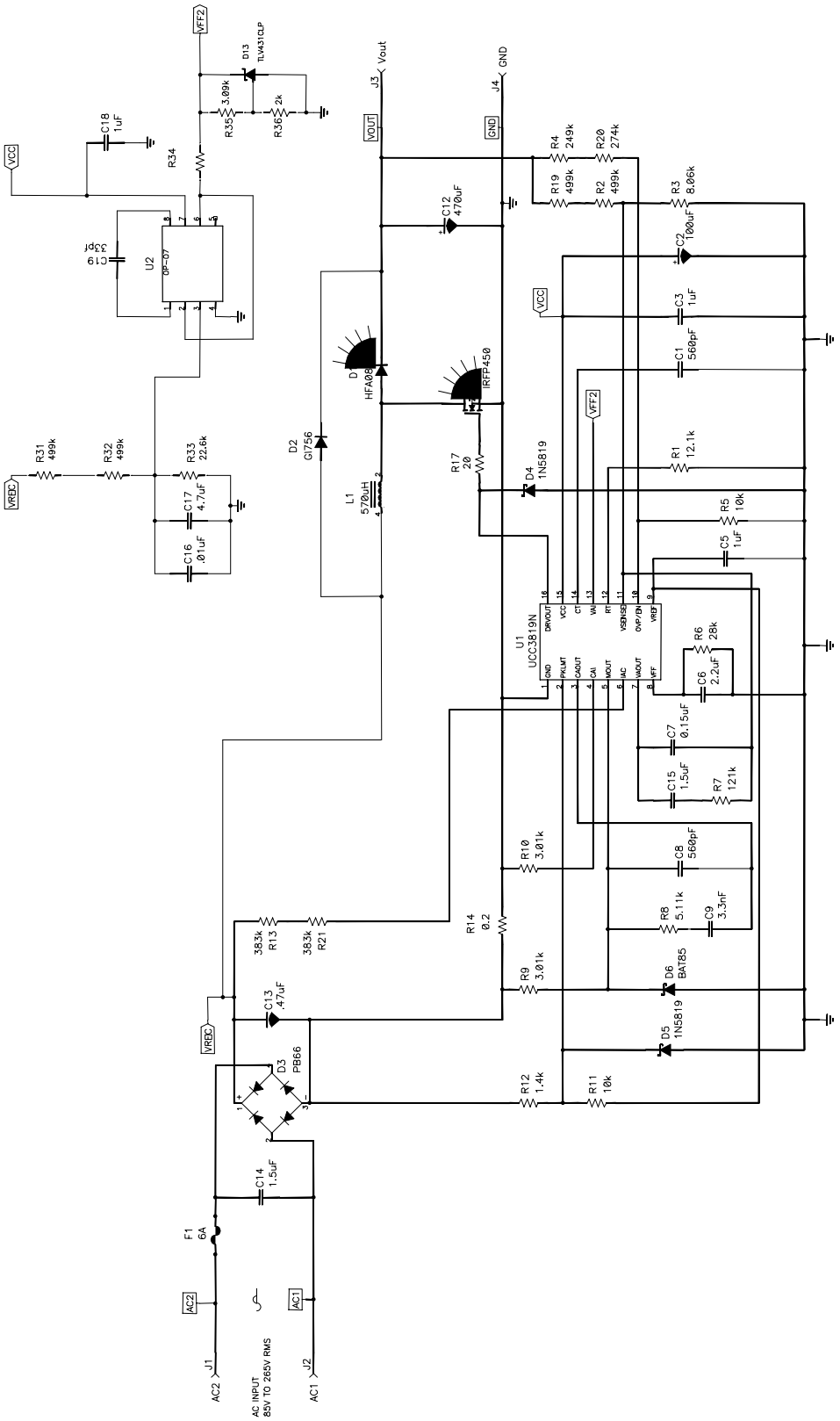


Figure 2. Reference Design Schematic

Table 2. Variable Definitions

VARIABLE	DEFINITIONS
C_{DIODE}	Boost diode capacitance
C_{OSS}	FET Drain to source capacitance
G_{VEA}	Gain of the voltage amplifier
D	Duty cycle
f_S	PWM switching frequency
G_{PID}	Control to output gain of the current loop at the desired crossover frequency
G_{PID} (f)	Control to output gain of the current loop
G_{PS}(f)	Voltage loop control to output gain
$I_{MO\_MAX(high\_line)}$	Peak I_{MO} current at high-line input
I_{RMS_DIODE}	Boost diode current
I_{RMS_FET}	RMS current in the FET
I_{RMS_L}	RMS inductor current
Osc_Amplitude	Typical oscillator ramp amplitude
P_{SEMI}	Power dissipated by a semiconductor device
P_{CON_FET}	Conduction losses in the FET
P_{COND_DIODE}	Diode conduction losses
P_{COSS}	Power dissipated by the FET's drain to source capacitance
P_{DIODE}	Total loss in the boost diode
P_{DIODE_CAP}	Loss due to boost diode capacitance
P_{DIODE_TR}	Boost diode transition loss
P_{FET_TR}	FET transition losses
P_{GATE}	Power dissipated by the FET gate
P_{OUT}	Maximum output power
P_{Q1}	Total FET losses
Q_{GATE}	FET gate charge
$R_{DS(on)}$	On resistance of the FET
$R\theta_{CS}$	Thermal impedance case to sink
$R\theta_{JC}$	Thermal impedance junction to case
$R\theta_{SA}$	Thermal impedance sink to air
T_A	Ambient temperature
t_{HOLDUP}	Boost capacitor holdup time
$T_{J(max)}$	Maximum semiconductor temperature
t_F	FET fall time
t_R	FET rise time
t_{RR}	Reverse recover time for a boost diode
$T_{S(f)}$	Voltage loop frequency response
$V_{AI(max)}$	Maximum voltage amplifier reference
$V_{AI(min)}$	Minimum voltage amplifier reference voltage
V_{CLAMP}	Voltage reference clamp to ensure the boost voltage is not exceeded
$V_{EA(max)}$	Maximum voltage amplifier output.
$V_{EA(min)}$	Minimum voltage amplifier output
V_{GATE}	Gate drive voltage
V_{DROP}	Amount of voltage the boost capacitor is allowed to drop during holdup.
$V_{IN(max)}$	Maximum RMS input voltage

VARIABLE	DEFINITIONS
$V_{IN(min)}$	Minimum RMS input voltage
$V_{OUT(max)}$	Maximum dc output voltage
$V_{OUT(min)}$	Minimum dc output voltage
V_{PP}	Output peak-to-peak ripple voltage
V_{REF_TL431}	Reference voltage of the TL431
ΔI	Change in boost inductor ripple current
η	Efficiency
%THD	Percentage of allowable total harmonic distortion

2 Power Stage Design

2.1 Inductor Selection

The boost inductor is selected based on the maximum allowed ripple current at maximum duty cycle at the peak of minimum line voltage. The following equations can be used to calculate the required inductor for the power stage with ripple current that is 20% of the peak input current. The calculated inductance for this design was roughly 570 μH. In traditional application the boost voltage ($V_{OUT(min)}$) would be fixed at roughly 390 V. For the same power levels and input conditions for the traditional boost converter would require and inductance of roughly 1 mH. To make the design process easier the inductor was designed by Cooper Electronics.

$$\Delta I = \frac{P_{OUT} \times \sqrt{2} \times 0.2}{V_{IN\,(min)}} \tag{1}$$

$$D = 1 - \frac{V_{OUT\,(min)} - V_{IN\,(min)} \times \sqrt{2}}{V_{OUT\,(min)}} \tag{2}$$

$$L1 = \frac{V_{IN\,(min)} \times \sqrt{2} \times D}{\Delta I \times f_S} \tag{3}$$

2.2 Boost Switch Selection (D1) and Boost Diode Selection (Q1)

To properly select D1 and Q1 a power budget is generally set for these devices to maintain the desired efficiency goal. Equations (4), (5), and (6) are used to estimate power loss in the switching devices. To meet the power budget for this design an IRFP450 HEX FET and HFA08TB60 fast recovery diode from International Rectifier were chosen for this design to meet the power constraints.

To calculate the loss in Q1:

$$I_{RMS\_FET} = \frac{P_{OUT}}{V_{IN\,(min)} \times \sqrt{2}} \times \sqrt{2 - \frac{16 \times V_{IN(min)} \times \sqrt{2}}{3 \times \pi \times V_{OUT(min)}}} \qquad I_{RMS\_L} = \frac{P_{OUT}}{V_{OUT\,(min)}} \tag{4}$$

$$P_{GATE} = Q_{GATE} \times V_{GATE} \times f_S \tag{5}$$

$$P_{COSS} = \frac{1}{2} C_{OSS} \times \left(V_{OUT(min)}\right)^2 \times f_S \tag{6}$$

$$P_{COND\_FET} = R_{DS(on)} \times \left(I_{RMS\_FET}\right)^2 \quad (7)$$

$$P_{FET\_TR} = \frac{1}{2} V_{OUT(min)} \times I_{RMS\_L} \times 0.9 \times \left(t_R + t_F\right) \times f_S \quad (8)$$

$$P_{Q1} = P_{GATE} + P_{COSS} + P_{COND\_FET} + P_{FET\_TR} \quad (9)$$

To calculate the loss in D1:

$$I_{RMS\_DIODE} = \frac{P_{OUT}}{V_{OUT\ (min)}} \times \sqrt{\frac{16 \times V_{OUT(min)}}{3\ \times \pi \times V_{IN(min)} \times \sqrt{2}}} \quad (10)$$

$$P_{COND\_DIODE} = V_F \times I_{RMS\_DIODE} \quad (11)$$

$$P_{DIODE\_CAP} = \frac{C_{DIODE}}{2} \times \left(V_{OUT(min)}\right)^2 \times f_S \quad (12)$$

$$P_{DIODE\_TR} = \frac{1}{2} V_{OUT(min)} \times I_{RMS\_DIODE} \times \left(t_{RR}\right) \times f_S \quad (13)$$

$$P_{DIODE} = P_{COND\_DIODE} + P_{DIODE\_CAP} + P_{COND\_TR} \quad (14)$$

2.3 Benefits of the Boost Follower Topology on the Power Stage at Low-Line

The more traditional PFC preregulator topology has a fixed output voltage that is greater than the peak line voltage. The fixed boost voltage for a universal input is typically set at 390 V. The boost follower is designed so that the output voltage is greater than the peak input voltage. For this design the output tracks the input from 206 V to 390 V. From the equations for transition loss and capacitance loss for the boost switch (Q1), it can be observed that these losses should be less at lower line voltages for the boost follower topology as compared to the traditional preregulator. The calculated losses for Q1 and D1 in the traditional topology were approximately 25 W and the calculated losses for switch and diode for the boost follower was approximately 17.4 W. The boost follower topology should be at least 3% more efficient at low line than the traditional topology. When compared to that of a traditional converter with the same power levels, the finished converter's low-line efficiency is approximately 5% more efficient. (See Figure 3.)

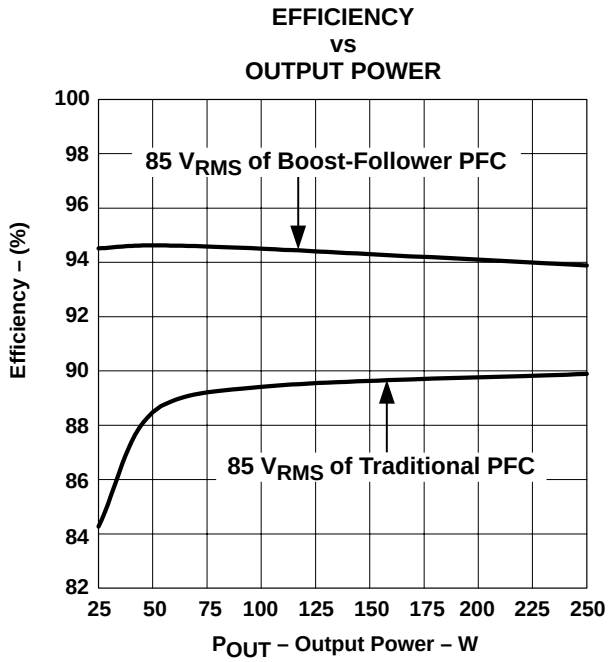


Figure 3.

2.4 Heat Sinks

Equation (15) calculates the minimum required thermal impedances of the heat sinks ($R\theta_{SA}$) required for this design. The heat sinks are designed to ensure that the junction tempature stays below 75% of the rated maximum. The heat sinks require a fan capable of forcing 40°C air at 150 LFPM. The heat sink required for Q1 using the traditional topology required an AVVID heat sink part number 53002 that is approximately 4.125 cubic inches. The heat sink for the boost follower topology required an AVVID heat sink part number 531202 of approximately 1.38 cubic inches which is about 66% smaller than the heat sink used in the traditional design.

$$R\theta_{SA} = \frac{T_{J(max)} - T_A - P_{SEMI} \times \left(R\theta_{CS} + R\theta_{JC}\right)}{P_{SEMI}} \tag{15}$$

2.5 Holdup Capacitor Selection

Equation (16) is used to estimate the size of the hold-up capacitor and the maximum allowable RMS current through the boost capacitor. The hold-up capacitor was designed for 16.7 ms of holdup time (t_{HOLDUP}) allowing the output 85 V of drop (V_{DROP}). For this design the calculated minimum hold-up capacitance was approximately 330 µF requiring roughly 1.7 A of RMS current at low-line operation. This minimum calculated capacitance value is roughly double of what is required in the traditional design. This is one of the negative aspects of using a boost follower topology.

$$C12 \geq 2 \times P_{OUT} \times \frac{t_{HOLDUP}}{\left[V_{OUT(min)}\right]^2 - \left[V_{OUT(min)} - V_{DROP}\right]^2} \tag{16}$$

$$I_{RMS\_C12} = \frac{P_{OUT}}{V_{OUT\,(min)}} \times \sqrt{\frac{16 \times V_{OUT(min)}}{3 \times \pi \times V_{IN(min)} \times \sqrt{2}} - 1} \quad (17)$$

2.6 Multiplier Setup

The multiplier is used to shape the input current waveform and must be set up correctly to get proper PFC. Equations (18) and (19) are used to set up the multiplier.

$$R13 + R21 = \frac{V_{IN(max)} \times \sqrt{2}}{500\ \mu A} \quad (18)$$

$$R6 = \frac{1.4\ V}{\frac{V_{IN(min)}}{(R13+R21)\times 2} \times 0.9} \quad (19)$$

Three voltage signals in this circuit, having a 120-Hz ripple component, contribute to input current total harmonic distortion (THD). The voltage feedforward (VFF) of the multiplier is one that contribute to THD. To meet the design goal of less than 5% THD, each signal is allowed to contribute only 1.5% allowable 120-Hz distortion (%THD). To meet the current THD requirements, C6 is set to attenuate the 120-Hz voltage ripple present on the VFF input of the multiplier to 1.5% (%THD) of the VFF pin's voltage range.

$$C6 = \frac{1}{2 \times \pi \times \frac{\%THD}{66\%} \times 120\ Hz \times R6} \quad (20)$$

2.7 Peak Current Limit

The UCC3819 has a peak current limit comparator that can be set up with a voltage divider using the VREF pin of the PWM controller. R14, R12 and R11 are selected to have the peak limit comparator trip at 110% of the maximum output power to protect Q1. This comparator limits only the current through the switch and not the current drawn by the output.

2.8 Power Limiting

Resistor R9 is selected to achieve soft power limiting at maximum output power[1].

$$R9 = \frac{\frac{P_{OUT} \times \sqrt{2}}{\eta \times V_{IN(max)}} \times R14}{I_{MO\_MAX(high\_line)}}, \qquad R9 = R10 \tag{21}$$

2.9 Current Amplifier

Equations (22) and (23) are used to compensate the current loop with a desired crossover frequency at 1/10 of the switching frequency. Resistor R8 and capacitor C9 form a zero at the desired crossover frequency that gives an added 45 degrees of phase margin for circuit stability. Capacitor C8 and and resistor R8 form a high-frequency pole to attenuate any high-frequency noise that may be present in the system.

$$G_{PID} = \frac{V_{OUT(max)} \times R14}{2 \times \pi \times \left(\frac{f_S}{10}\right) \times L1 \times Osc\_Amplitude} \tag{22}$$

$$R8 = \frac{1}{G_{PID}}, \; C9 = \frac{1}{2 \times \pi \times \left(\frac{f_S}{10}\right) \times R8}, \; C8 = \frac{1}{2 \times \pi \times \left(\frac{f_S}{2}\right) \times R8} \tag{23}$$

3 VAI Input Sensing Circuit with Clamp

The UCC3819 PWM controller allows the user to set the reference voltage (VAI) externally. It is this feature that allows the designer to use an integrated PWM controller with a boost follower topology. With a few external components, a circuit can be constructed that sets VAI proportional to the input voltage. This reference voltage is then used to make the output voltage track the input voltage. Figure 4 shows the external components that are required to generate the VAI voltage.

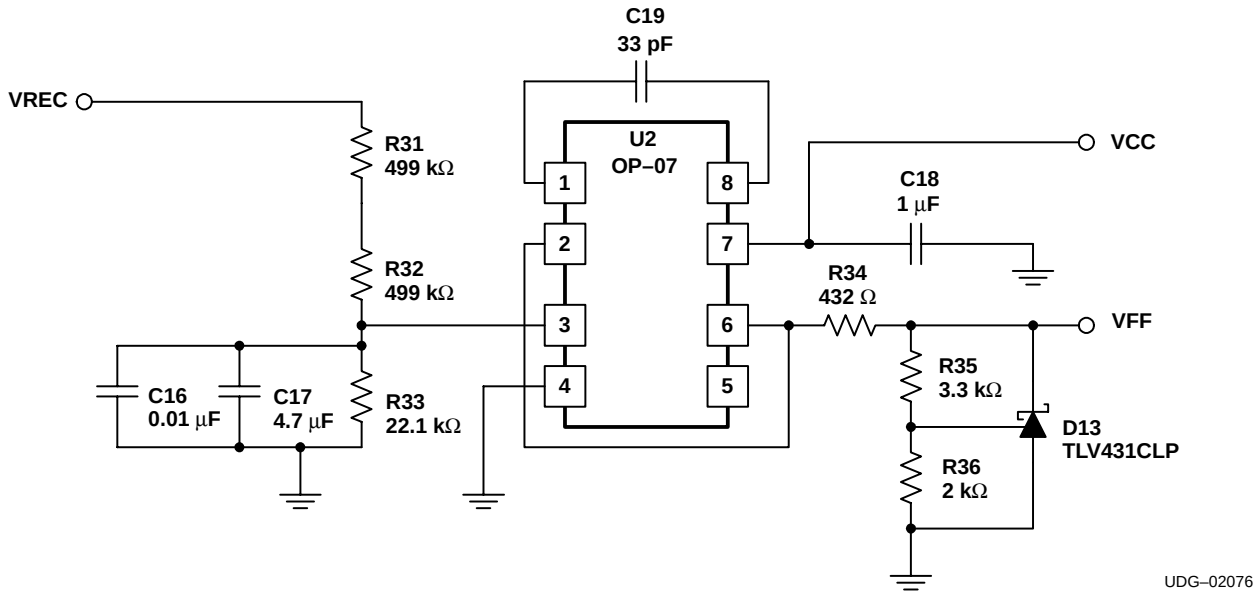


Figure 4. VAI Output Sensing Schematic

R31, R32, R33 and C17 form a voltage divider with a single-pole filter that is used to monitor the line voltage. R35, R36, and D13 form a VAI clamp to ensure the boost voltage does not exceed the design specification of 390 V. Equations (24) and (25) can be used to select the proper components for the circuit.

$$V_{AI(min)} = \frac{V_{AI(max)}}{2} \tag{24}$$

$$R33 = \frac{V_{AI(min)} \times (R31 + R32)}{V_{IN(min)} \times \left(0.9 - V_{AI(min)}\right)} \tag{25}$$

The VAI signal includes a 120-Hz component that can contribute to THD. Capacitor C17 is selected to keep its contribution to less than 1.5% THD.

$$C17 = \frac{1}{2 \times \pi \times \frac{V_{AI(max)} \times \%THD}{V_{IN(max)} \times \sqrt{2} \times 66\%} \times 120\ Hz \times R33} \tag{26}$$

Setting up the clamp voltage requires that the divider to the VSENSE pin be set up first.

$$R3 = \frac{V_{AI(min)} \times (R19 + R2)}{V_{OUT(min)} - V_{AI(min)}} \tag{27}$$

$$V_{CLAMP} = \frac{V_{OUT(max)} \times R3}{R19 + R29 + R3} \tag{28}$$

$$R35 = \frac{\left(V_{CLAMP} - V_{REF\_TL431}\right) \times R36}{V_{REF\_TL431}} \tag{29}$$

3.1 Voltage Amplifier

The voltage amplifier is compensated to attenuate the 120-Hz boost-ripple voltage (V_{PP}) in order to reduce it's contribution to THD.

$$V_{PP} = \frac{\frac{P_{OUT}}{\eta}}{\pi \times 120\ Hz \times C12 \times V_{OUT(min)}} \tag{30}$$

$$G_{VEA} = \frac{\%THD \times \left(V_{EA(max)} - V_{EA(min)}\right)}{V_{PP} \times 100} \tag{31}$$

$$C8 = \frac{1}{2 \times \pi \times 120\ Hz \times G_{VEA} \times R9} \tag{32}$$

$$f_C = \sqrt{\frac{P_{OUT}}{\left(V_{EA(max)} - V_{EA(min)}\right) \times \left(V_{OUT(min)}\right) \times 2 \times \pi \times C12}} \times \frac{1}{2 \times \pi \times R9 \times C8} \tag{33}$$

$$R8 = \frac{1}{2 \times \pi \times \left(\frac{f_S}{10}\right) \times C8} \tag{34}$$

4 Slower Voltage Loop Small Signal Transient Response at High Line

Another drawback to using a boost follower topology is the small signal transient response is slower at lower line voltages. Equations (35) through (38) model the voltage loop frequency response of both a boost follower and traditional PFC offline voltage regulator. These equations describe the power stage gain ($G_{PS(f)}$) as inversely proportional to output voltage. In the boost-follower topology the voltage loop is compensated when the boost voltage is at its lowest to ensure circuit stability. As the input voltage increases, V_{OUT} increases, which decreases the overall loop gain ($T_{S(f)}$). As $T_{S(f)}$ decreases the loop crosses over at a lower f_C, resulting in slower transient response. The traditional topology has a fixed output voltage and a fixed $T_{S(f)}$, which results in a fixed transient response, independent of line voltage.

$$s(f) = j \times 2 \times \pi \times f \tag{35}$$

$$G_{PS(f)} = \frac{P_{OUT}}{\left(V_{EA(max)} - V_{EA(min)}\right) \times V_{OUT} \times s(f) \times C12} \tag{36}$$

$$G_{EA(f)} = \frac{(s(f) \times R8 \times C9 + 1)}{S(f) \times R9 \times (C9 + C8) \times \left[S(f) \times R8 \times \frac{(C9 \times C8)}{(C9 + C8)} + 1\right]} \tag{37}$$

$$T_{s(f)} = -G_{PS(f)} \times G_{EA(f)} \tag{38}$$

Figures 5 and 6 show the measured voltage loop small-signal frequency response. The small signal transient response at low line is roughly twice as fast as it is at high line.

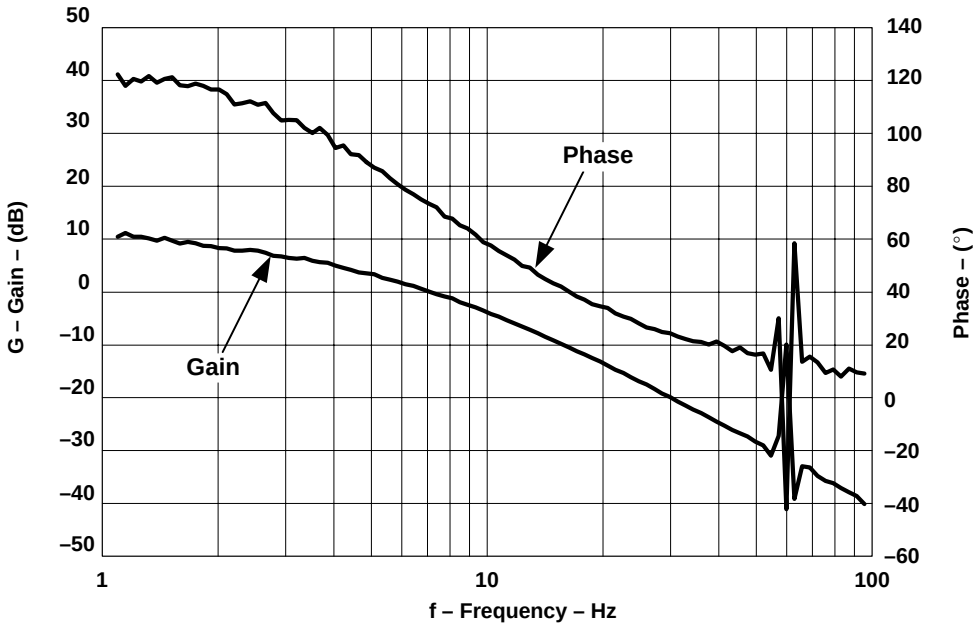


Figure 5. Voltage Loop Low-Line Frequency Response at Maximum Load

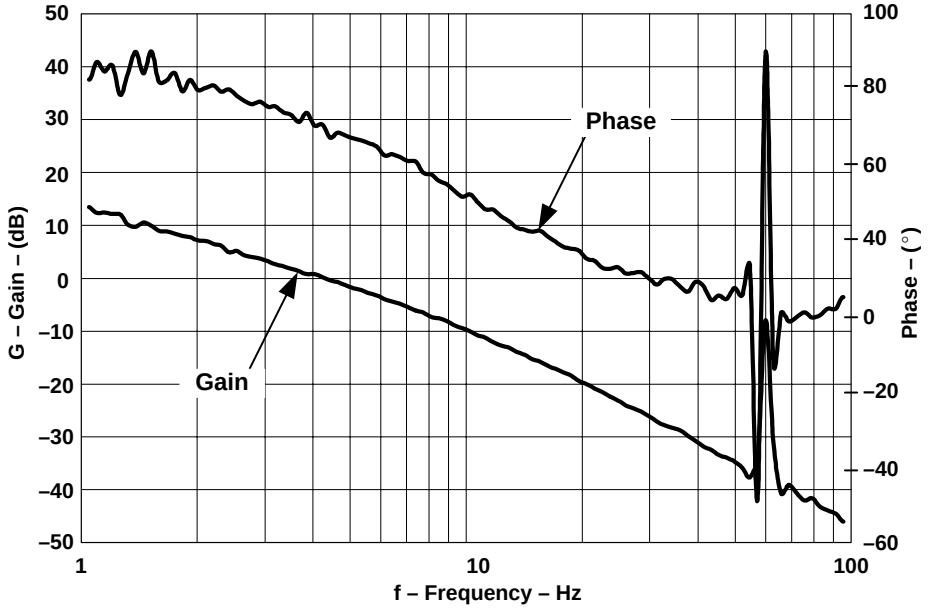


Figure 6. Voltage Loop High-Line Frequency Response at Maximum Load

5 Reference Design Performance Curves

The following graphs show the performance of the reference design.

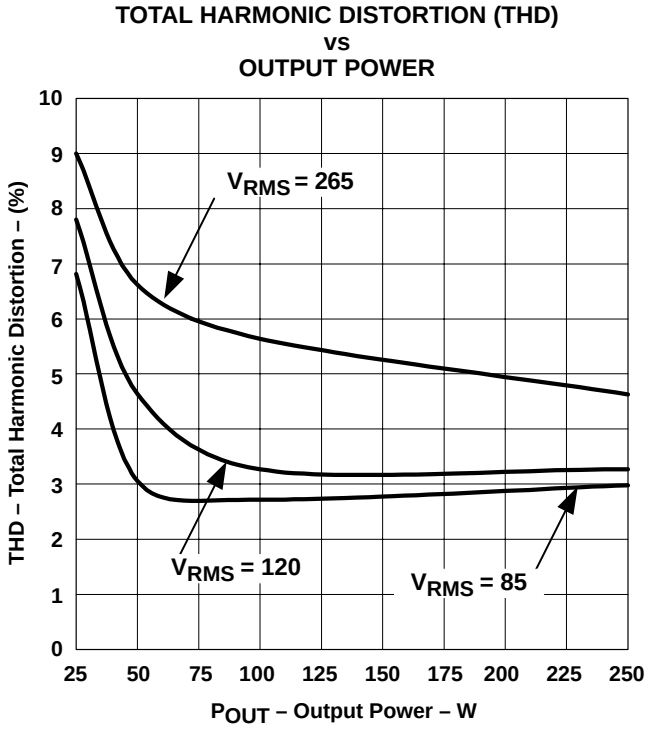


Figure 7.

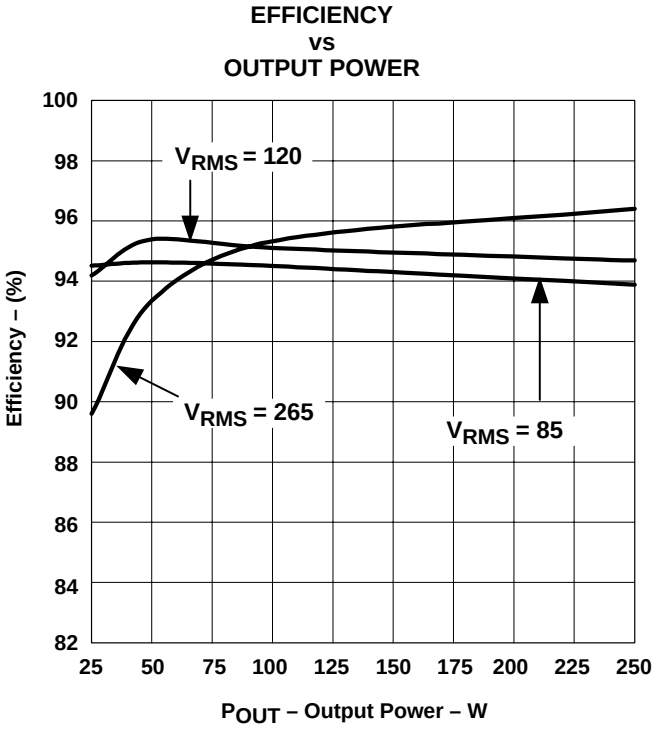


Figure 8.

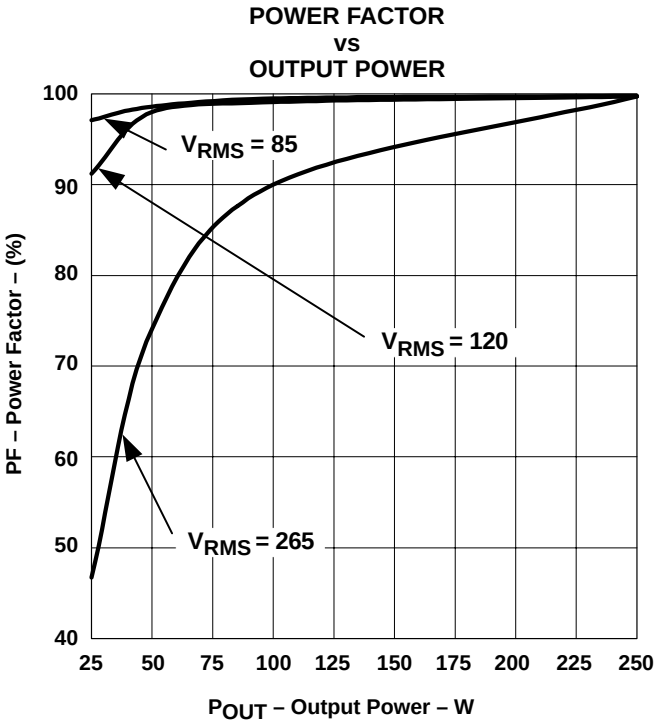
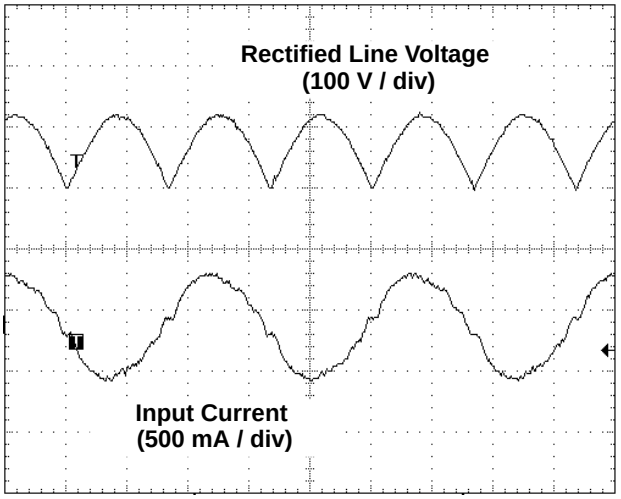


Figure 9.

LOW-LINE OPERATION

V_{IN} = 85 V
P_{OUT} = 25 W

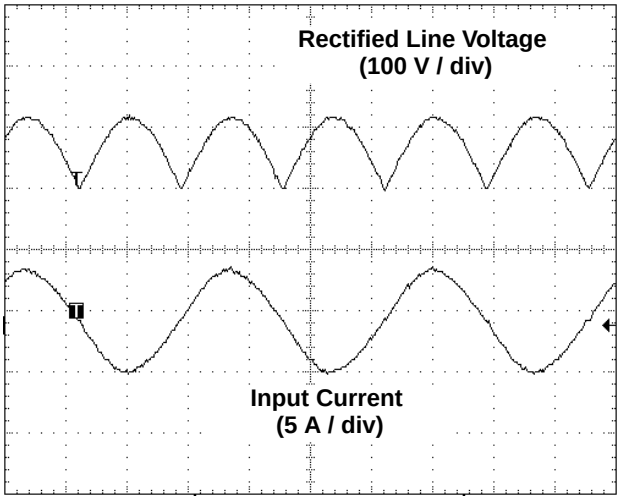


t – Time – 5 ms / div

Figure 10.

LOW-LINE OPERATION

V_{IN} = 85 V
P_{OUT} = 250 W

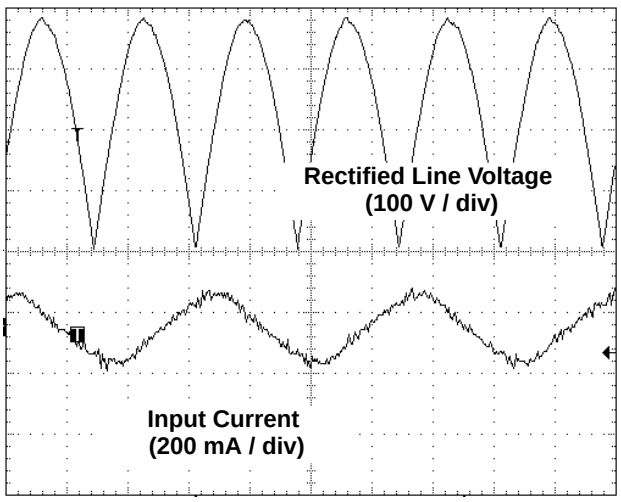


t – Time – 5 ms / div

Figure 11.

HIGH-LINE OPERATION

V_{IN} = 265 V
P_{OUT} = 25 W

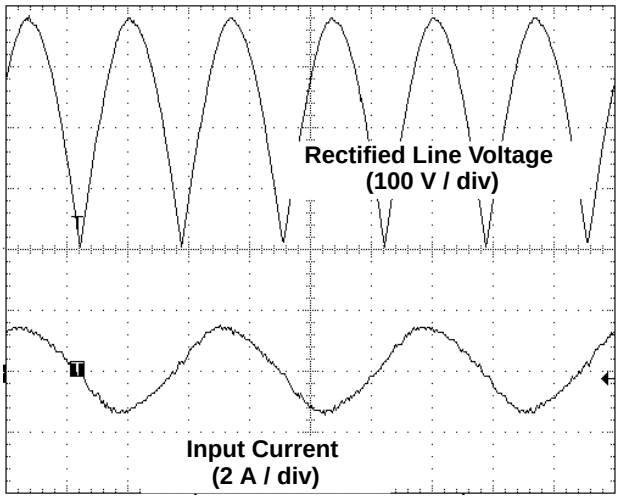


t – Time – 5 ms / div

Figure 12.

HIGH-LINE OPERATION

V_{IN} = 265 V
P_{OUT} = 25 W



t – Time – 5 ms / div

Figure 13.

6 References

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3. *POWER CONVERSION*, September 1992 Proceedings, (LIST PUBLICATION HERE) p. 67
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