

MODEL NAME : VAW00
 PROJECT CODE : ANRVAW0000
 PCB NO : LA-9104P (Thames XT)

DA60000VV00 LA-9104P M/B
 DA40001FO00 LS-9101P POWER BUTTON/B
 DA40001FP00 LS-9102P USB/B
 DA40001FQ00 LS-9103P TP BUTTON/B



Dell / Compal Confidential

Schematic Document

Intel Chief River

Ivy Bridge (BGA) + Panther Point

OAK 15" UMA/DIS AMD Thames XT

2012-08-22

Rev: 1.0

46@ : for 46 level
 @ : Nopop Component
 CONN@ : Connector Component
 KB9012@ : ENE KB9012 Implemented
 UMA@ : Only for UMA
 EMC@ : EMI/ESD parts

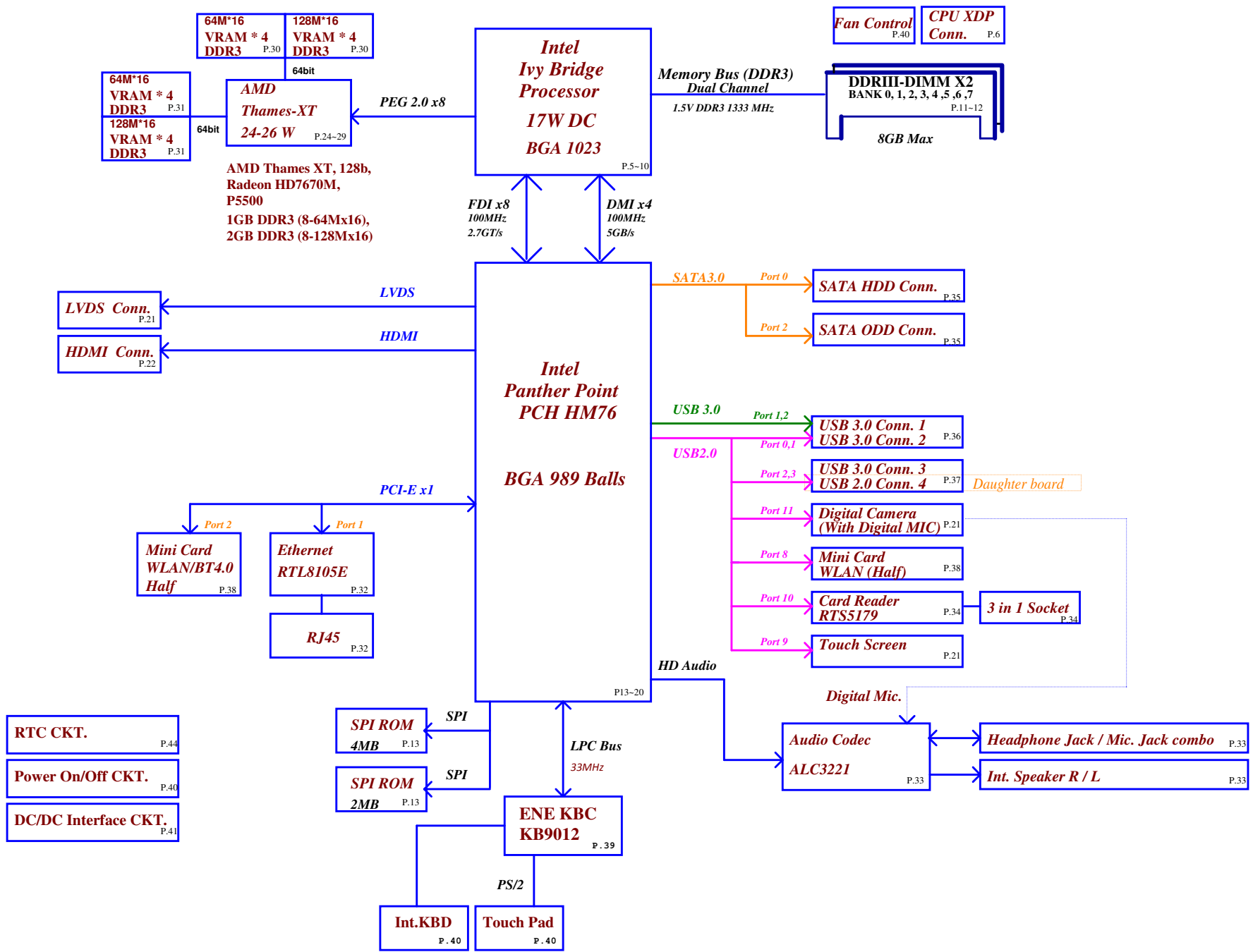
R1@ : R1 P/N
 R3@ : R3 P/N

i3R1@ : CPU i3-3217 1.8G
 i3VOSR1@ : CPU i3-2365 1.4G
 i5R1@ : CPU i5-3317 1.7G
 i7R1@ : CPU i7-3517 1.9G
 CELR1@ : CPU Celeron 887 1.5G
 PENR1@ : CPU Pentium 997 1.6G

DIS@ : Only for Discrete
 TH@/THR1@ : Thames-XT
 MS@/MSR1@ : Mars Pro
 X76@ :
 SPI-ROM & VRAM Group

GCLK@ : Green CLK implemented
 GCLKUMA@ : Green CLK for UMA
 GCLKDIS@ : Green CLK for DIS
 XTAL@ : X'tal implemented
 XTALDIS@ : X'tal with DIS implemented

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				Rev	1.0

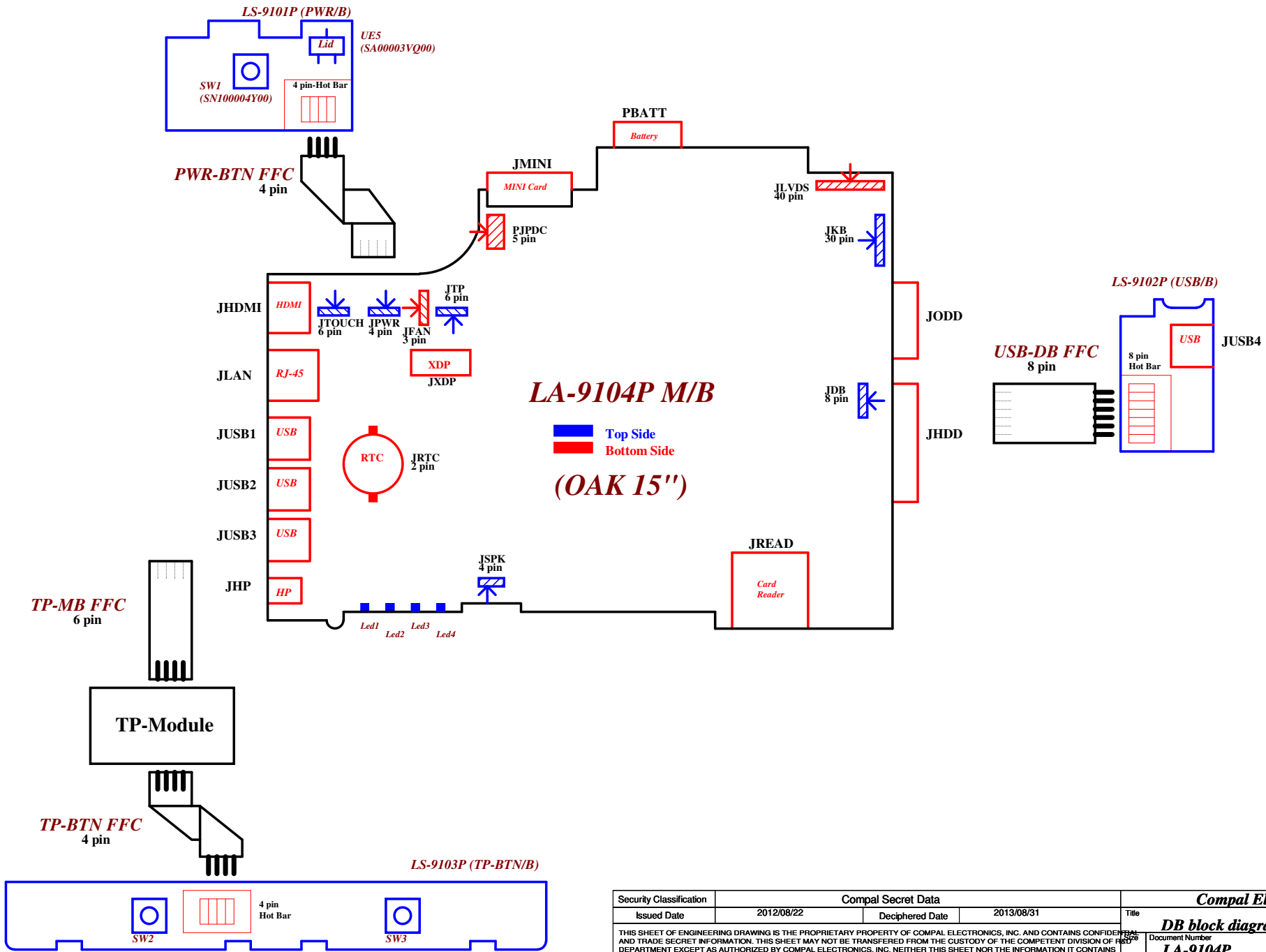


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Project Code : VAW00

File Name : LA-9104P



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Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

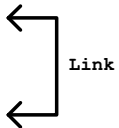
ID	PCB Revision
0	0.1
1	0.1
2	0.2
3	0.2
4	0.3
5	0.3
6	1.0
7	1.0

Project ID Table

ID	Project Revision
0	
1	
2	
3	
4	
5	UMA
6	DIS THAMES
7	DIS MARS PRO

SMBUS Control Table

	SOURCE	MINI1	MINI2	BATT	SODIMM	Express Card	Thermal Sensor	FFS	VGA Thermal Sensor	VGA	XDPA	Charger
EC_SMB_CK1 EC_SMB_DA1	KB9012			V								V
EC_SMB_CK2 EC_SMB_DA2	KB9012								V	V		
PCH_SML0CLK PCH_SML0DATA	PCH											
PCH_SML1CLK PCH_SML1DATA	PCH											
MEM_SMBCLK MEM_SMBDATA	PCH	V	V		V	V		V				V





PCH	USB PORT#	DESTINATION
	0	USB conn.2
	1	USB conn.1
	2	USB conn.3
	3	USB conn.4 (DB)
	4	NC
	5	NC
	6	NC
	7	NC
	8	MINI CARD (WLAN)
	9	Touch Screen
	10	Card Reader
	11	Camera
	12	NC
13	NC	

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	10/100 LAN	CLKOUTFLEX0	None
	CLKOUT_PCIE1	MINI CARD WLAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	None
	CLKOUT_PCIE3	None	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
CLKOUT_PEG_B	None			

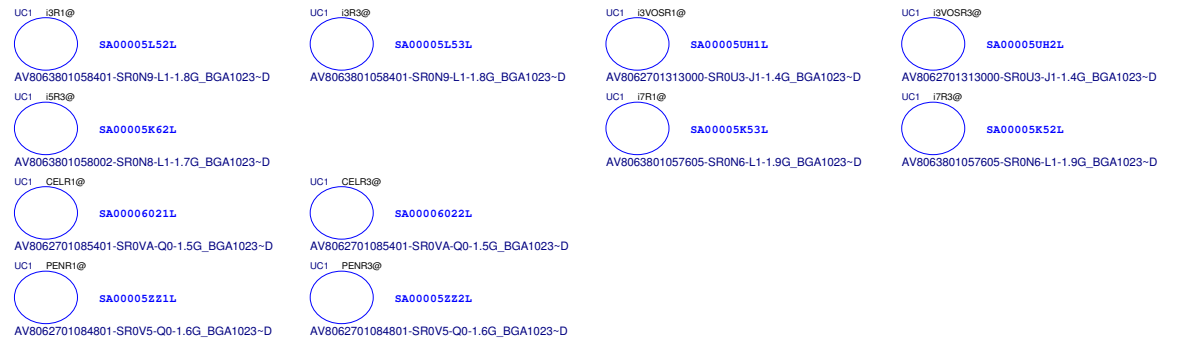
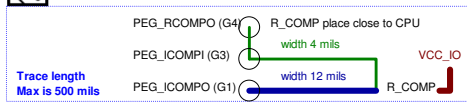
CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC LPC
PCI2	None
PCI3	None
PCI4	None

SATA	DESTINATION
SATA0	HDD
SATA1	None
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

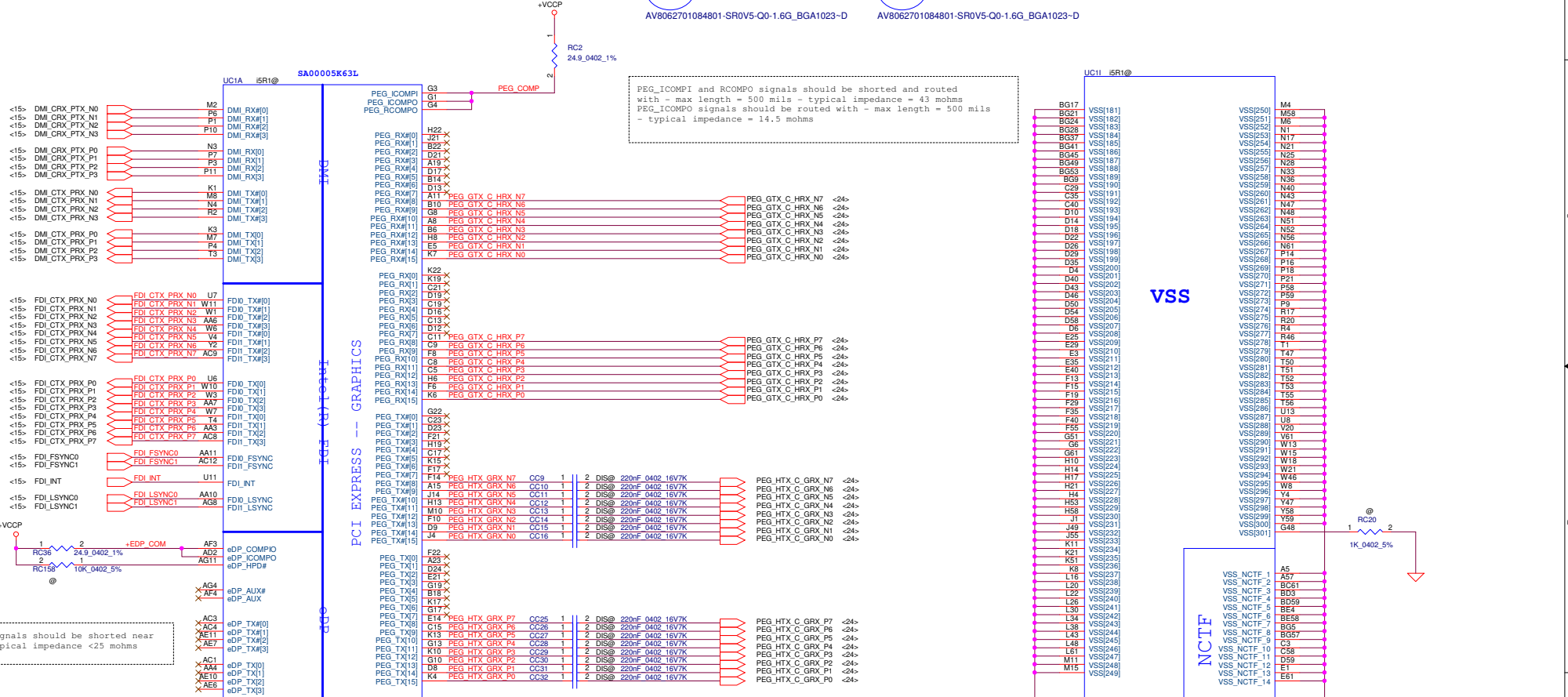
PCI EXPRESS	DESTINATION
Lane 1	10/100 LAN
Lane 2	MINI CARD (WLAN)
Lane 3	None
Lane 4	None
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

Symbol Note :
 : means Digital Ground
 : means Analog Ground

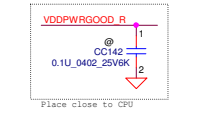
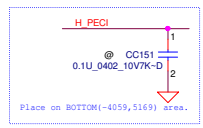
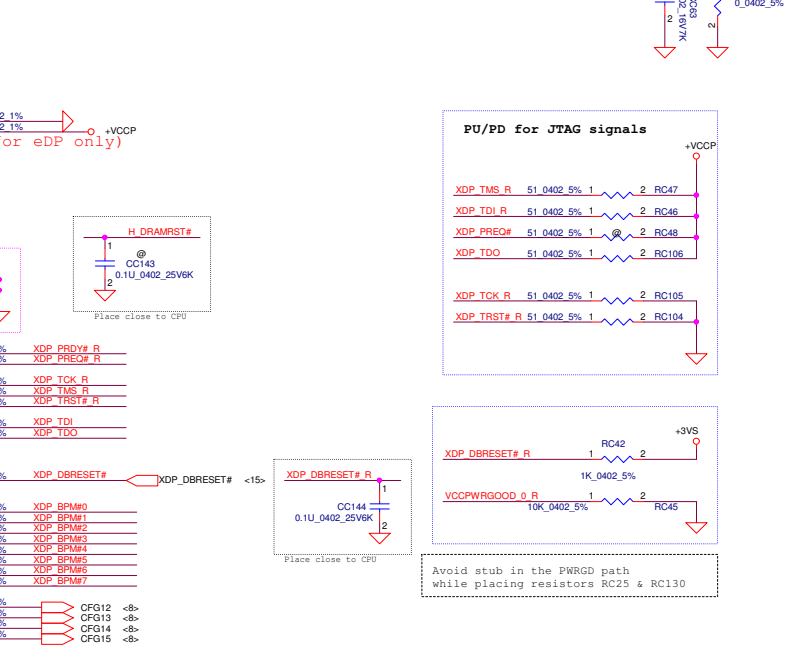
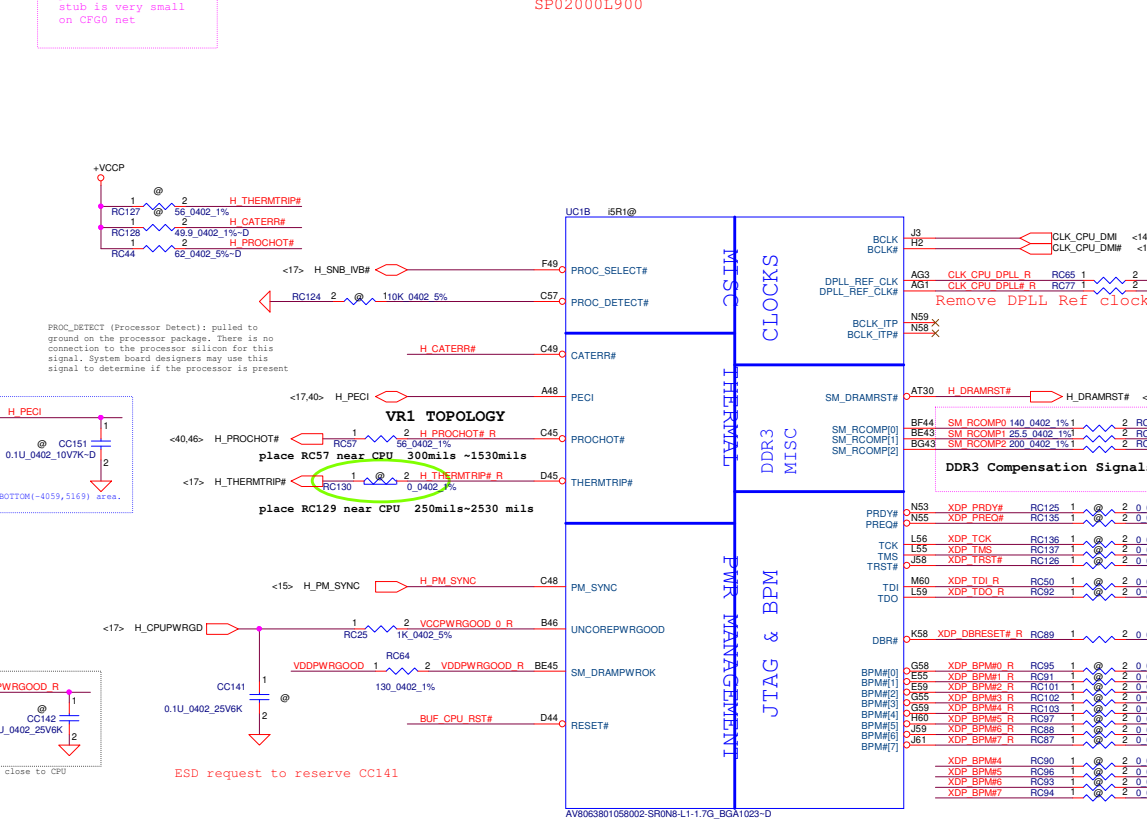
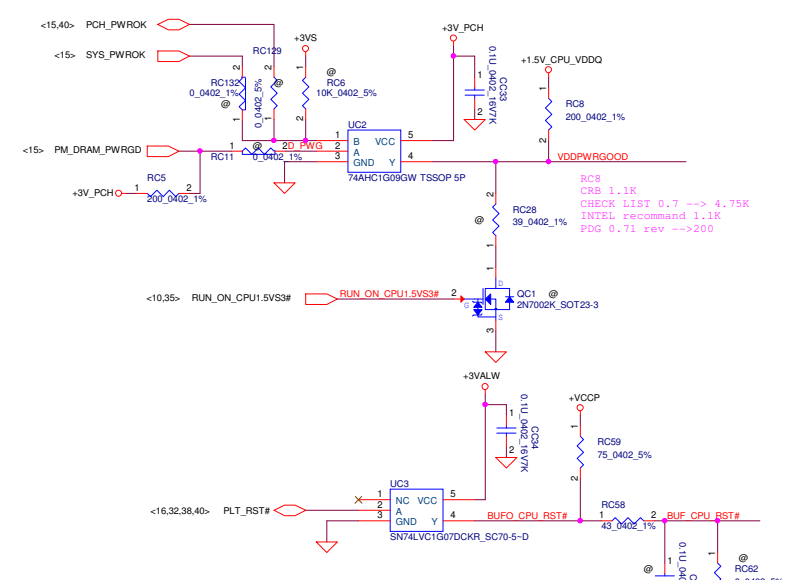
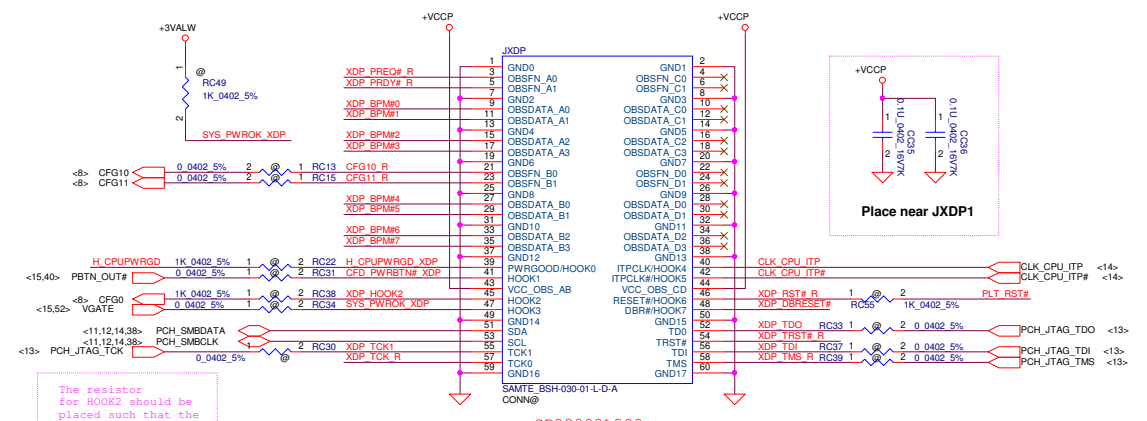
(1) PEG_RCOMP0 (G4) use 4mil connect to PEG_ICOMPU, then use 4mil connect to RC1.
 (2) PEG_ICOMPU use 12mil connect to RC1.



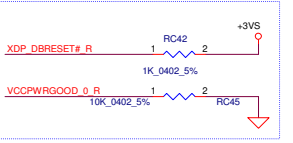
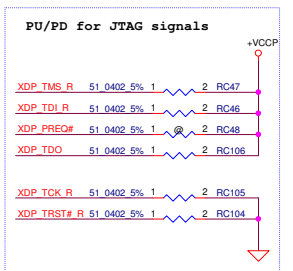
PEG_ICOMPI and RCOMP0 signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
 PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms



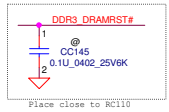
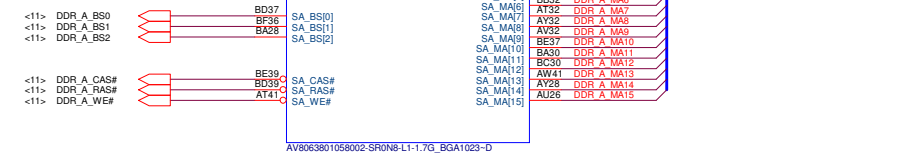
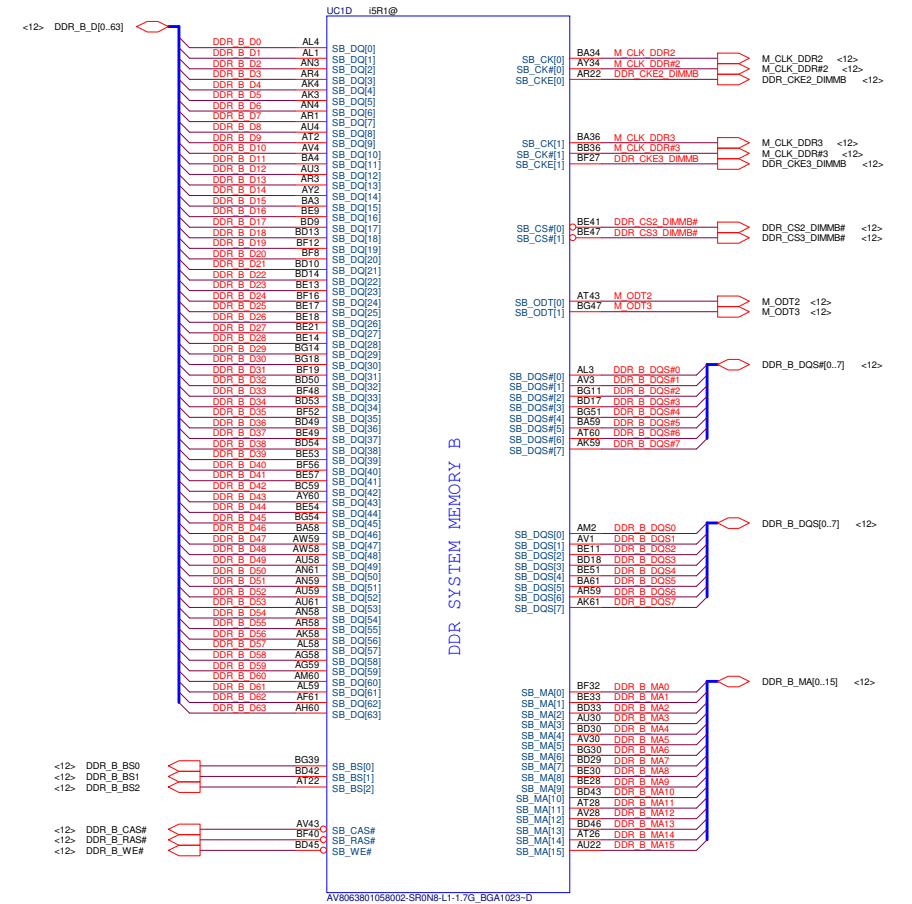
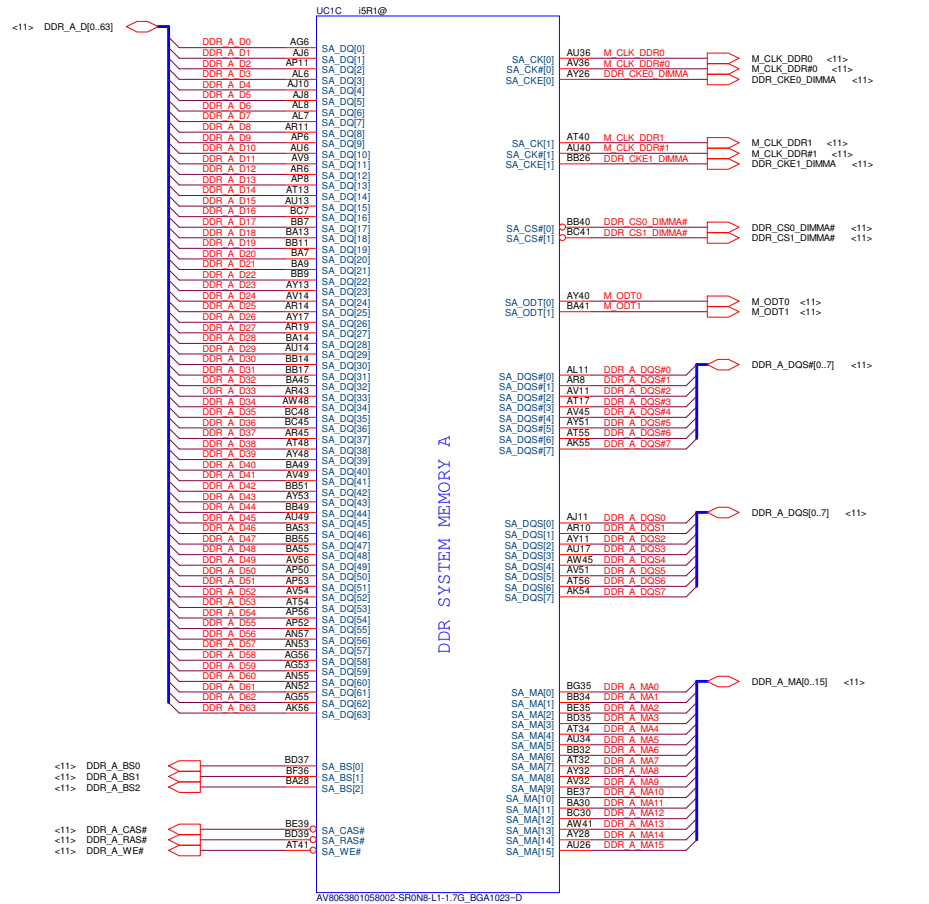
eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms



ESD request to reserve CC141

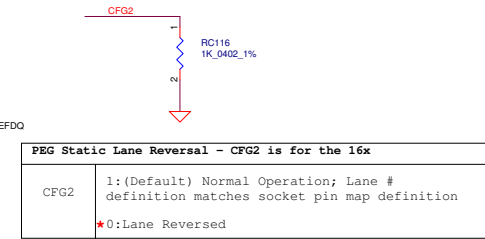
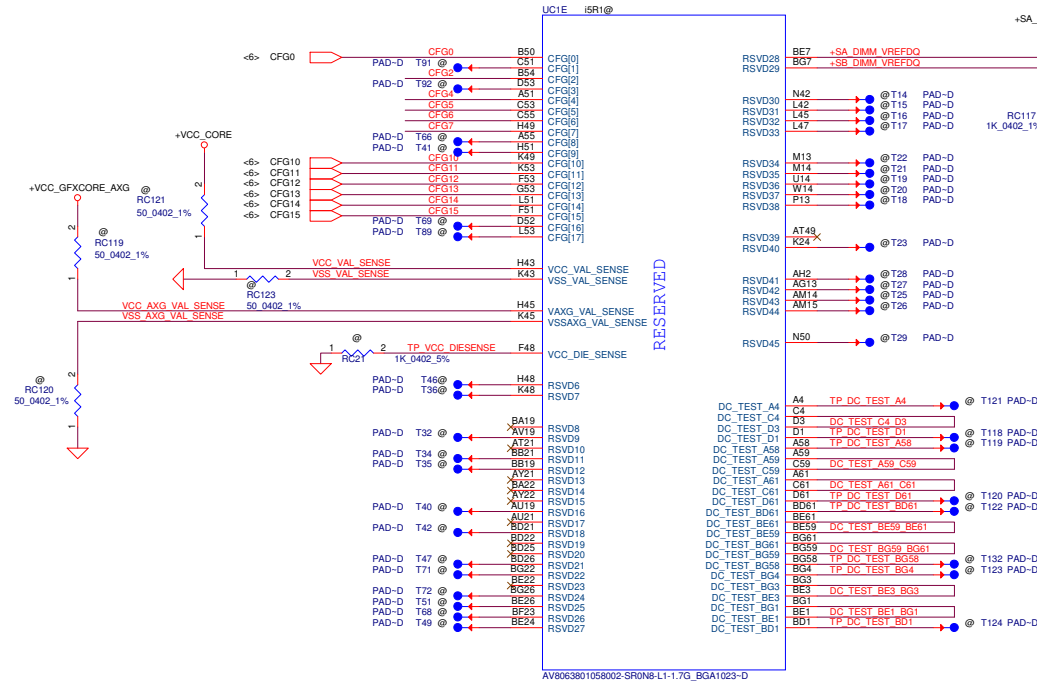


Avoid stub in the PWRGD path while placing resistors RC25 & RC130



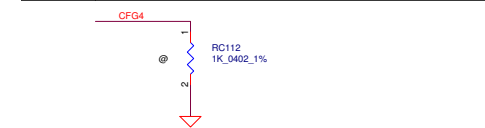
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CFG Straps for Processor



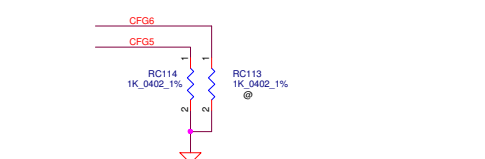
PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	1: (Default) Normal Operation; Lane # definition matches socket pin map definition
	* 0: Lane Reversed



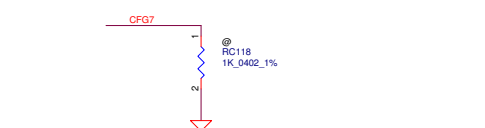
Display Port Presence Strap

CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port
	0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps

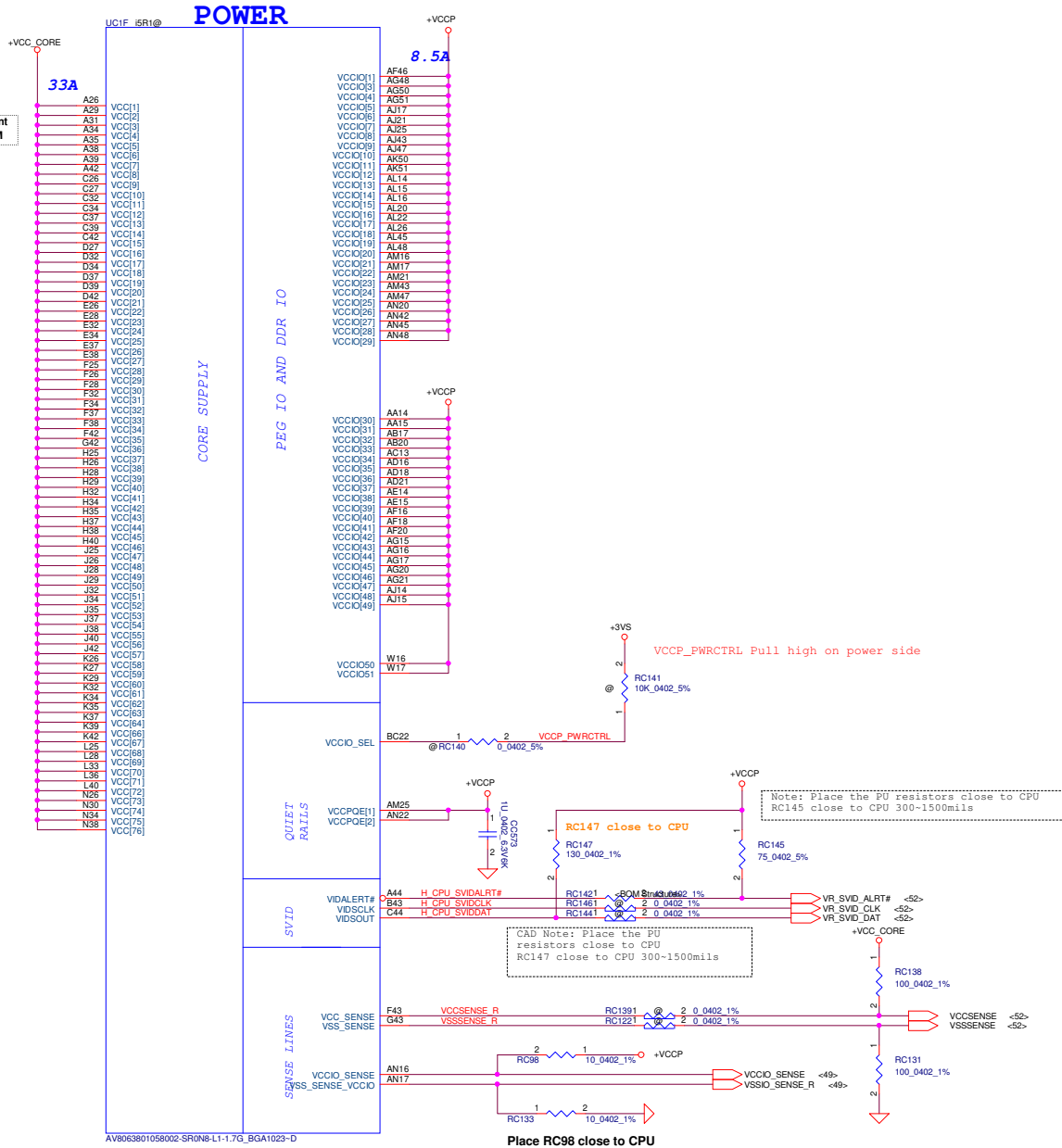
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled
	* 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
	01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
	00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING

CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion
	0: PEG Wait for BIOS for training

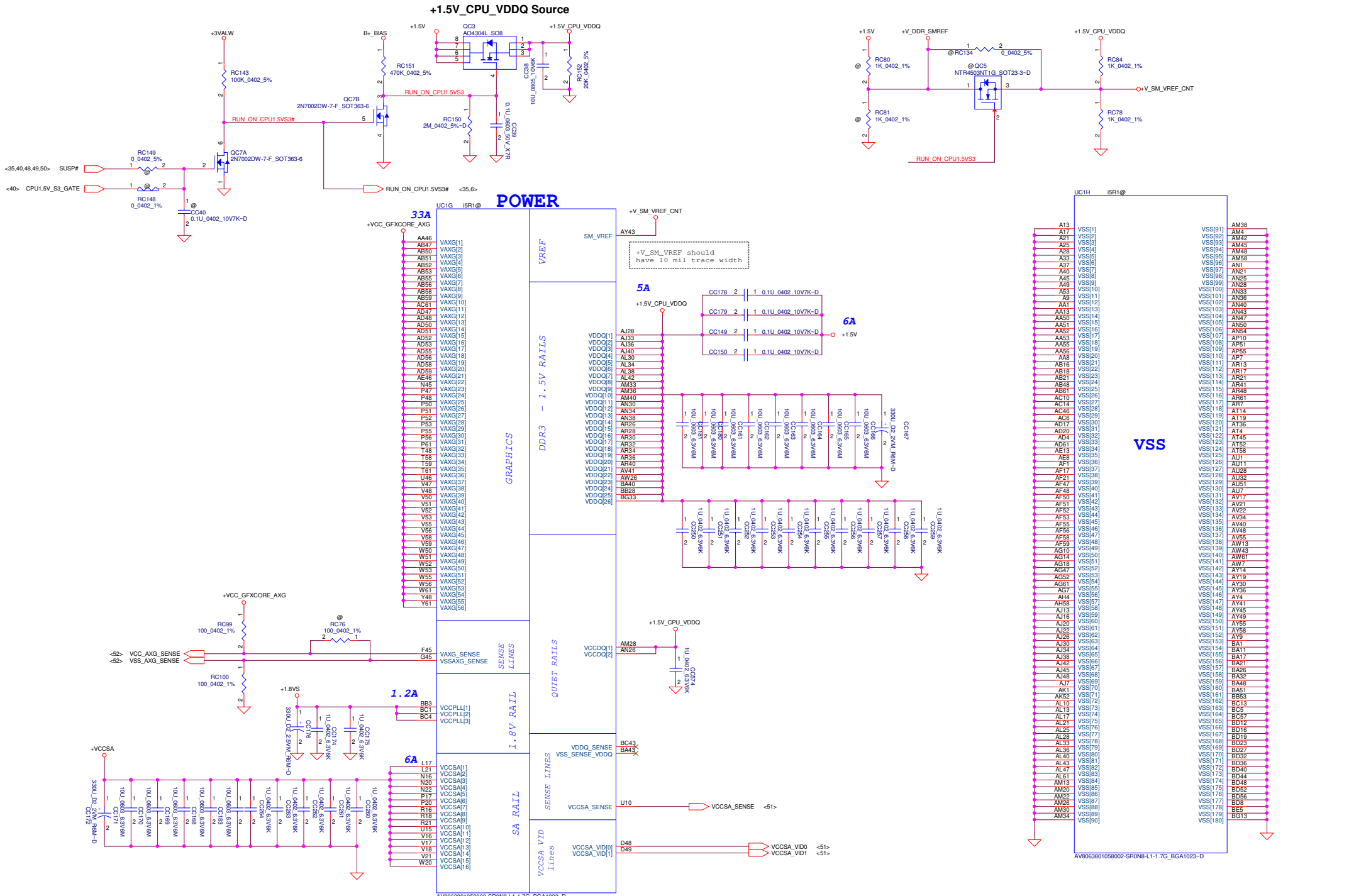
ULV 17W , Max Current
in Turbo Mode or HFM

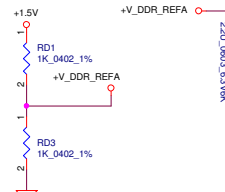
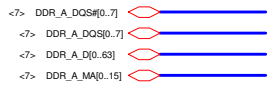


Iccmax current changed for PDDG Rev0.7

CPU Power Rail Table		
Voltage Rail	Voltage	SO Iccmax Current (A)
VCC	0.65-1.3	53
VCCIO	1.05/1	8.5
VAXG	0.0-1.1	33
VCCPLL	1.8	1.2
VDDQ	1.5	5
VCCSA	0.65-0.9	6
+1.5V_MEM	1.5	12-16 *

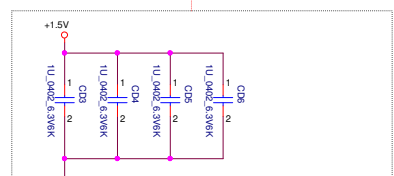
* Description
 5A to Mem controller (+1.5V_CPU_VDDQ)
 5-6A to 2 DIMMs/channel
 2-5A to +1.5V_RUN & +0.75V_DDR_VTT



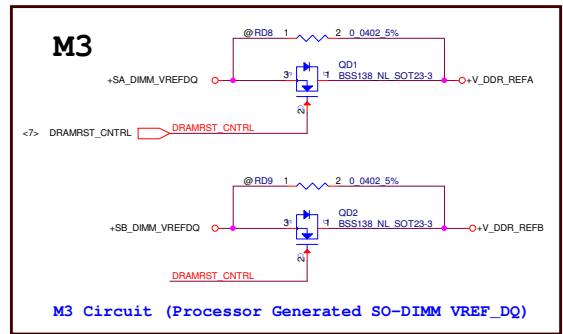
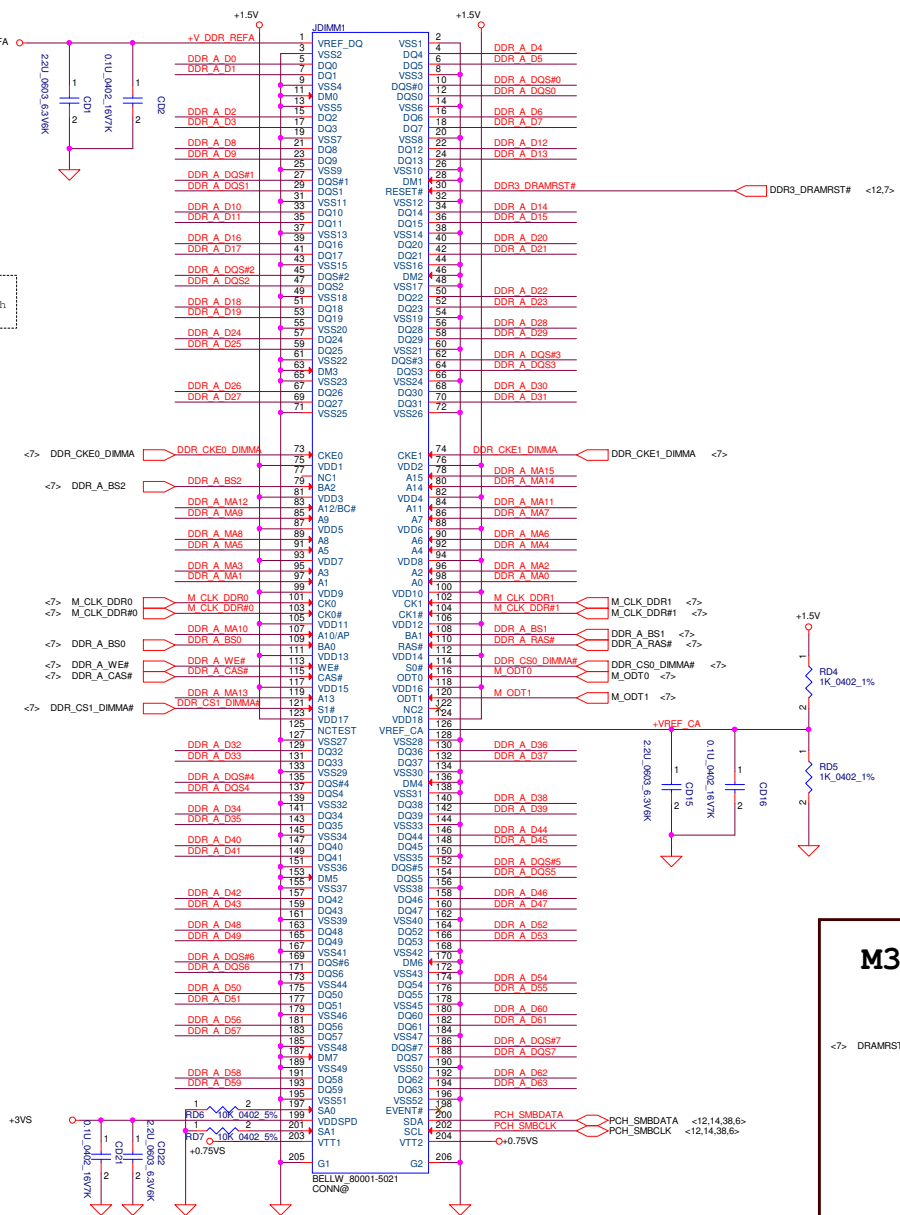
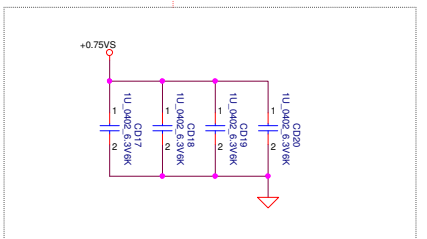


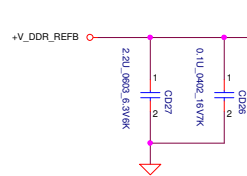
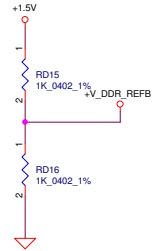
Layout Note:
Place near JDIMM1

All VREF traces should have 10 mil trace width



Layout Note:
Place near JDIMM1. 203, 204

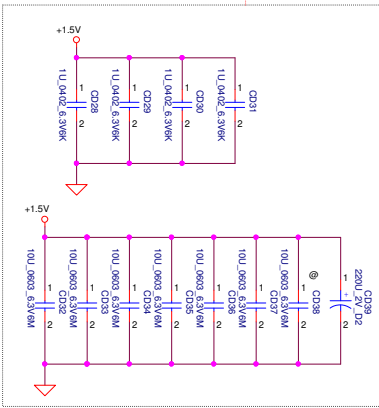




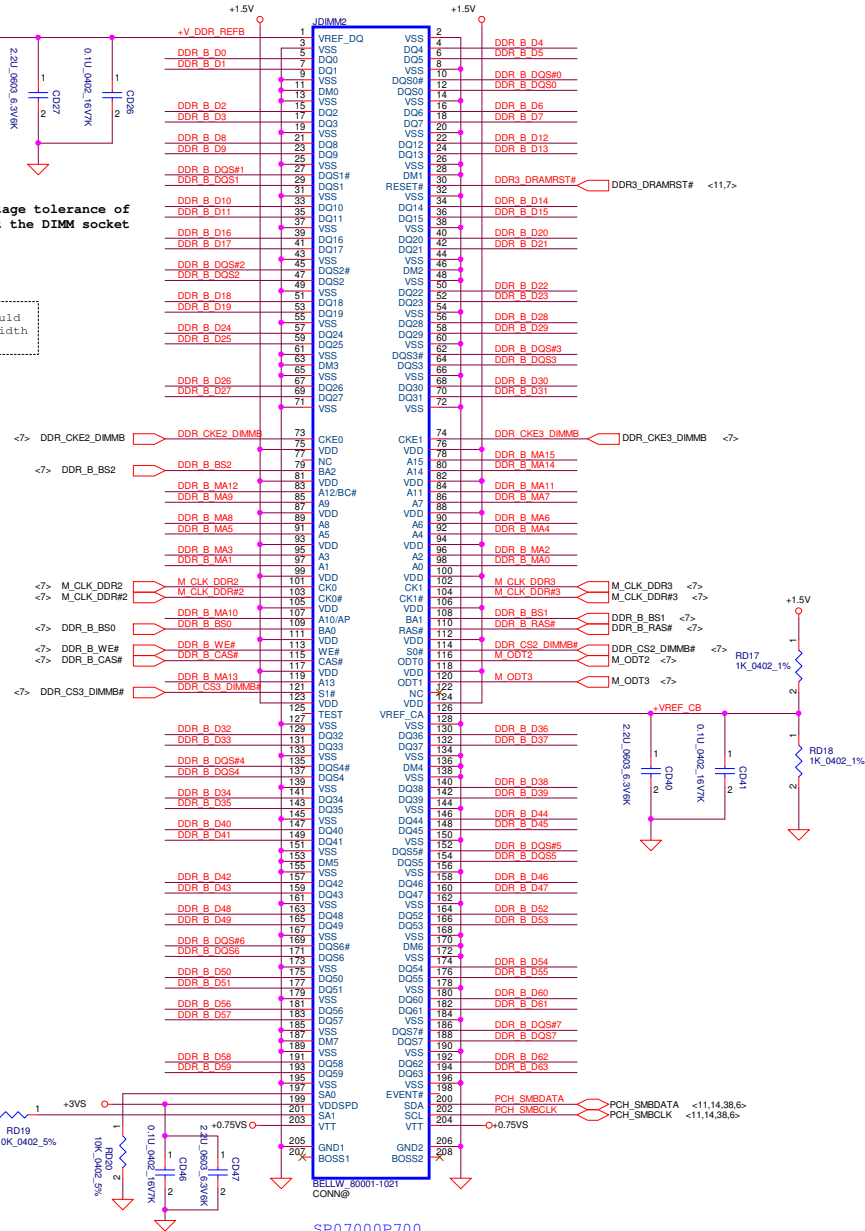
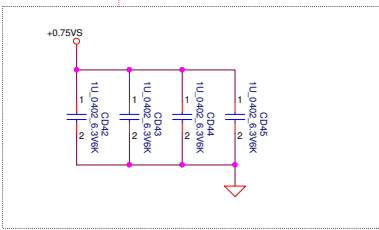
Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket

All VREF traces should
have 10 mil trace width

Layout Note:
Place near JDIMMB

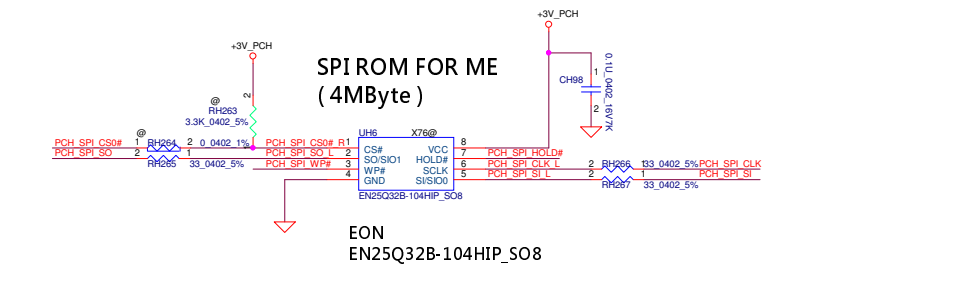
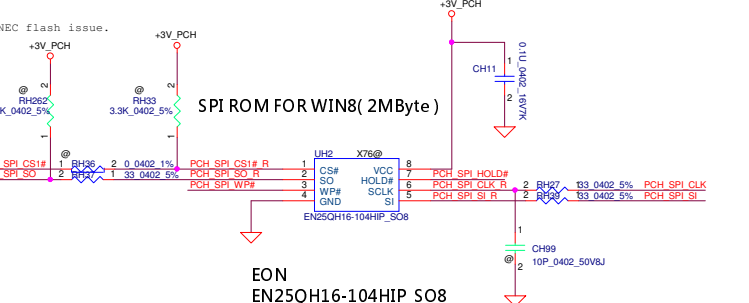
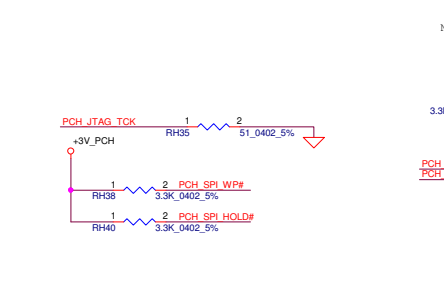
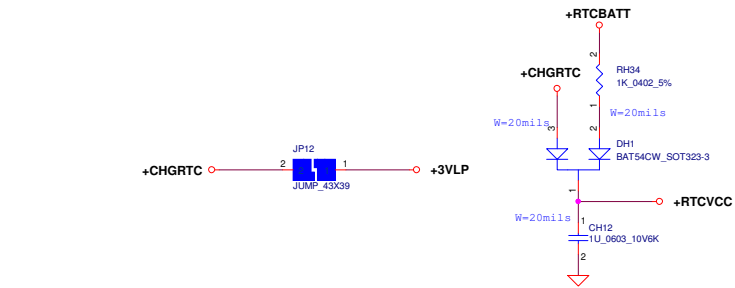
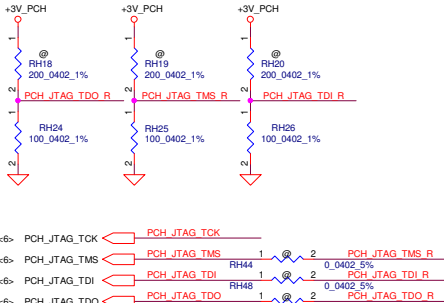
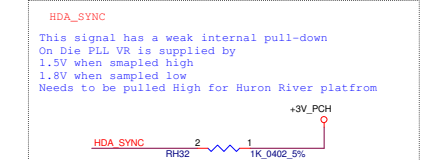
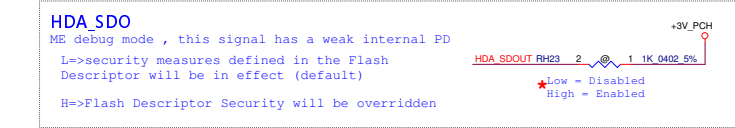
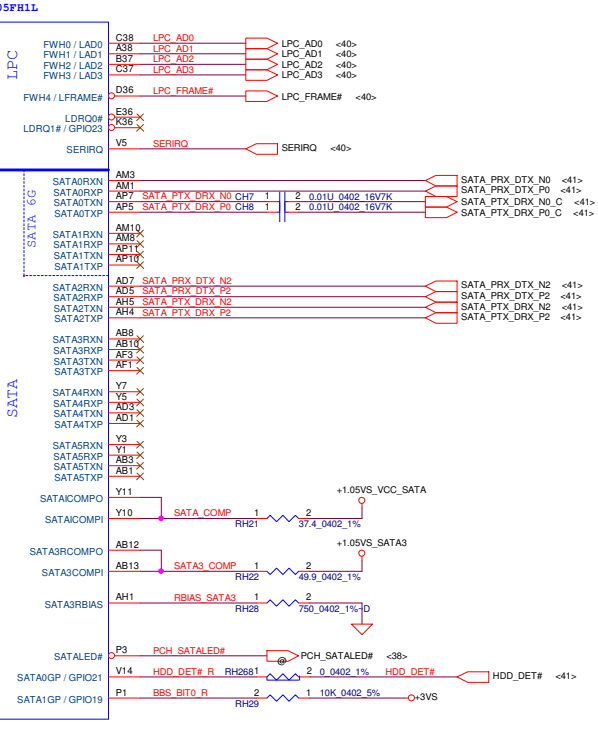
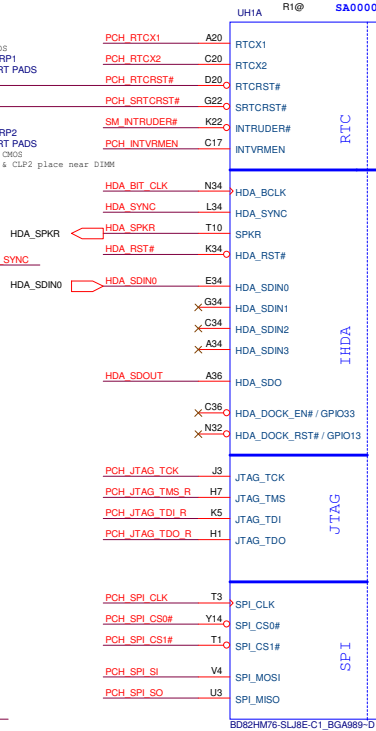
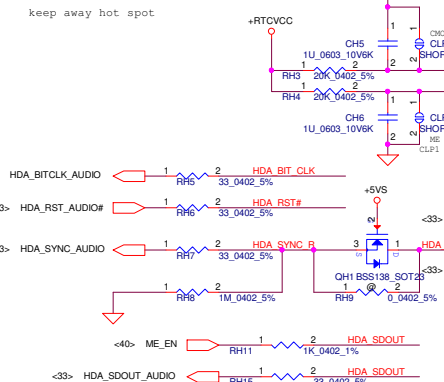
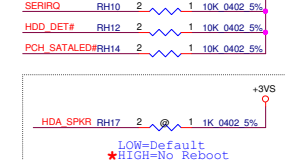
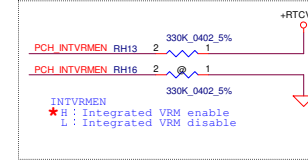
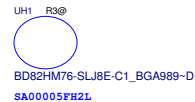
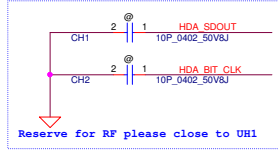
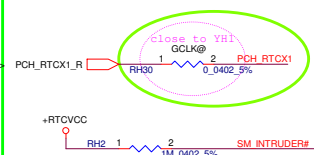
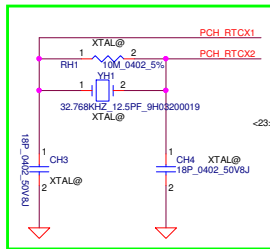


Layout Note:
Place near JDIMMB.203,204



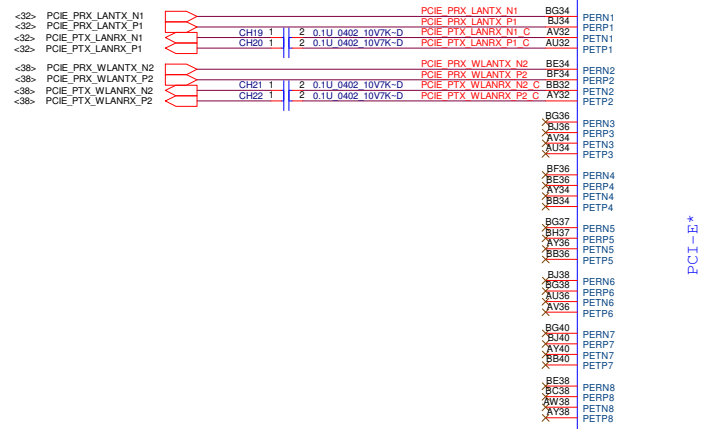
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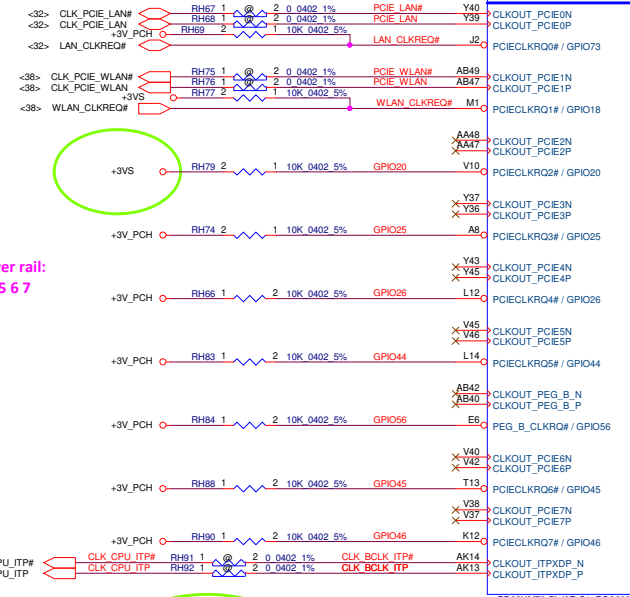


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Issued Date	2012/08/22	Deciphered Date	2013/08/31	PCH (I/8) SATA/HDA/SPI/LPC	
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Document Number	LA-9104P	Rev	1.0	Date	Wednesday, August 29, 2012
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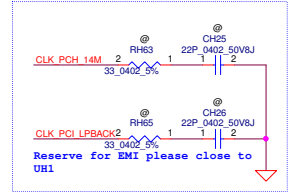
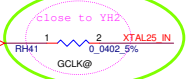
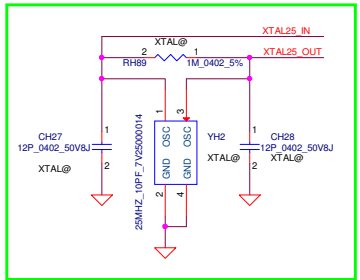
10/100 LAN
WLAN (Mini Card)



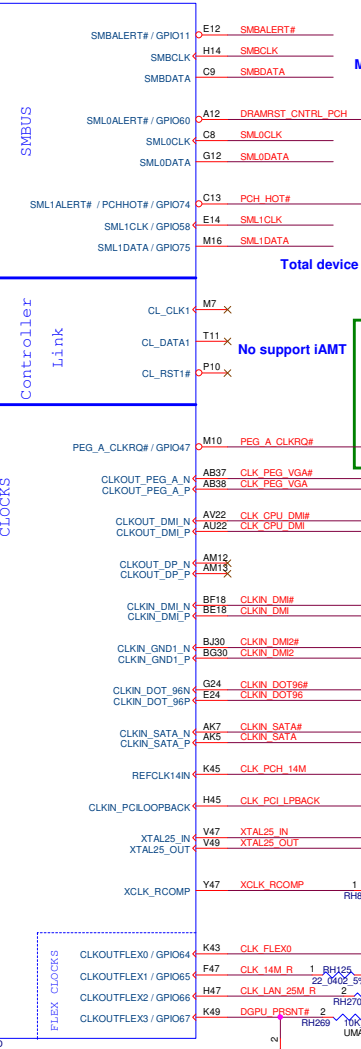
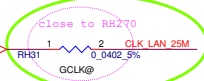
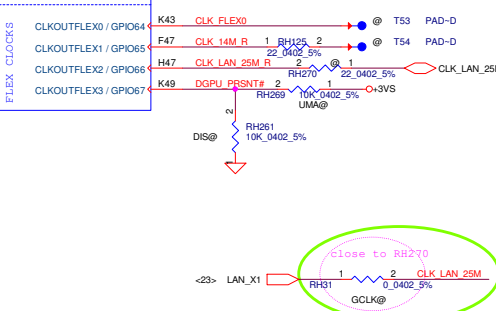
10/100 LAN
WLAN (Mini Card)



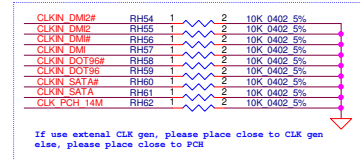
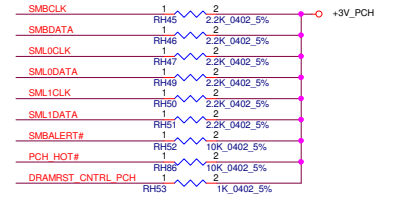
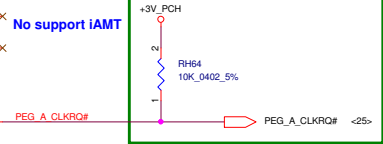
*PCIE REQ power rail:
suspend: 0 3 4 5 6 7
core: 1 2



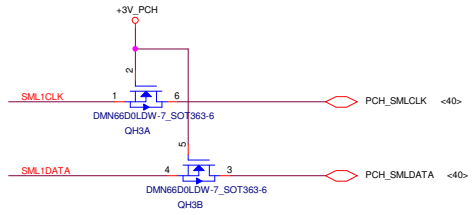
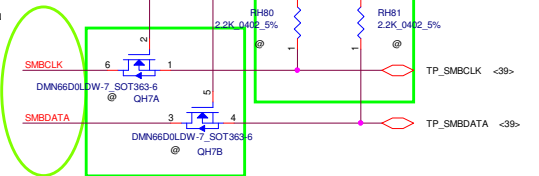
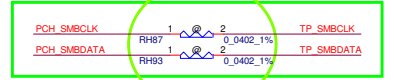
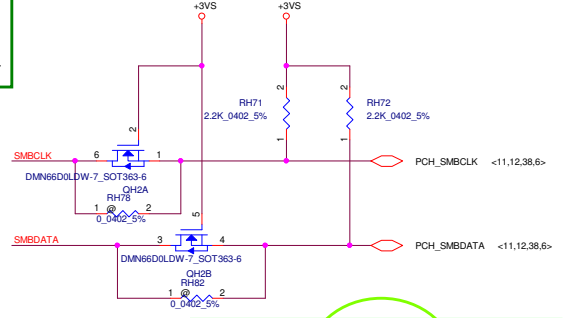
FLEX CLACKS



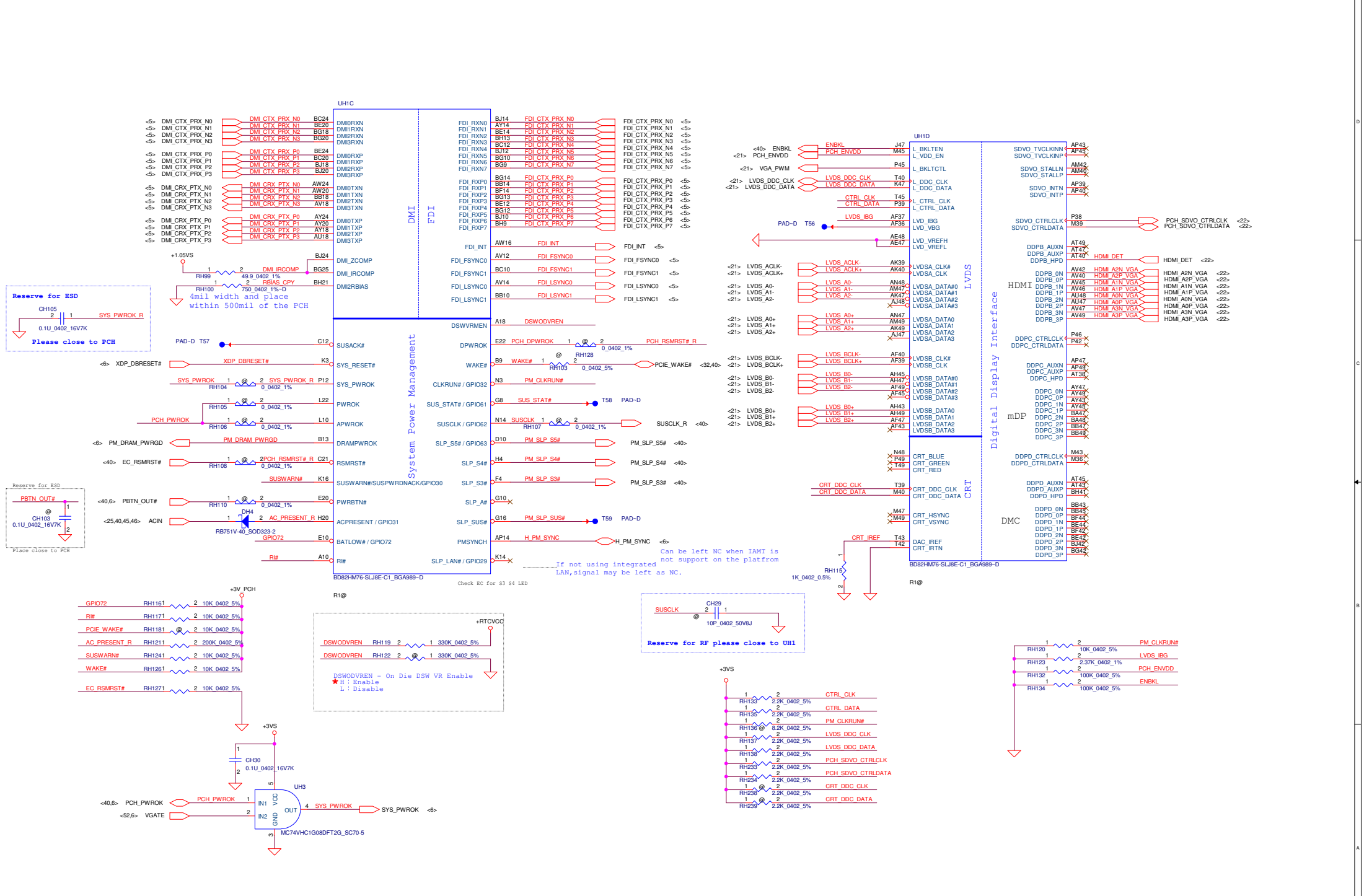
Total device
20090512
add double mosfet prevent
ATI M92 electric leakage

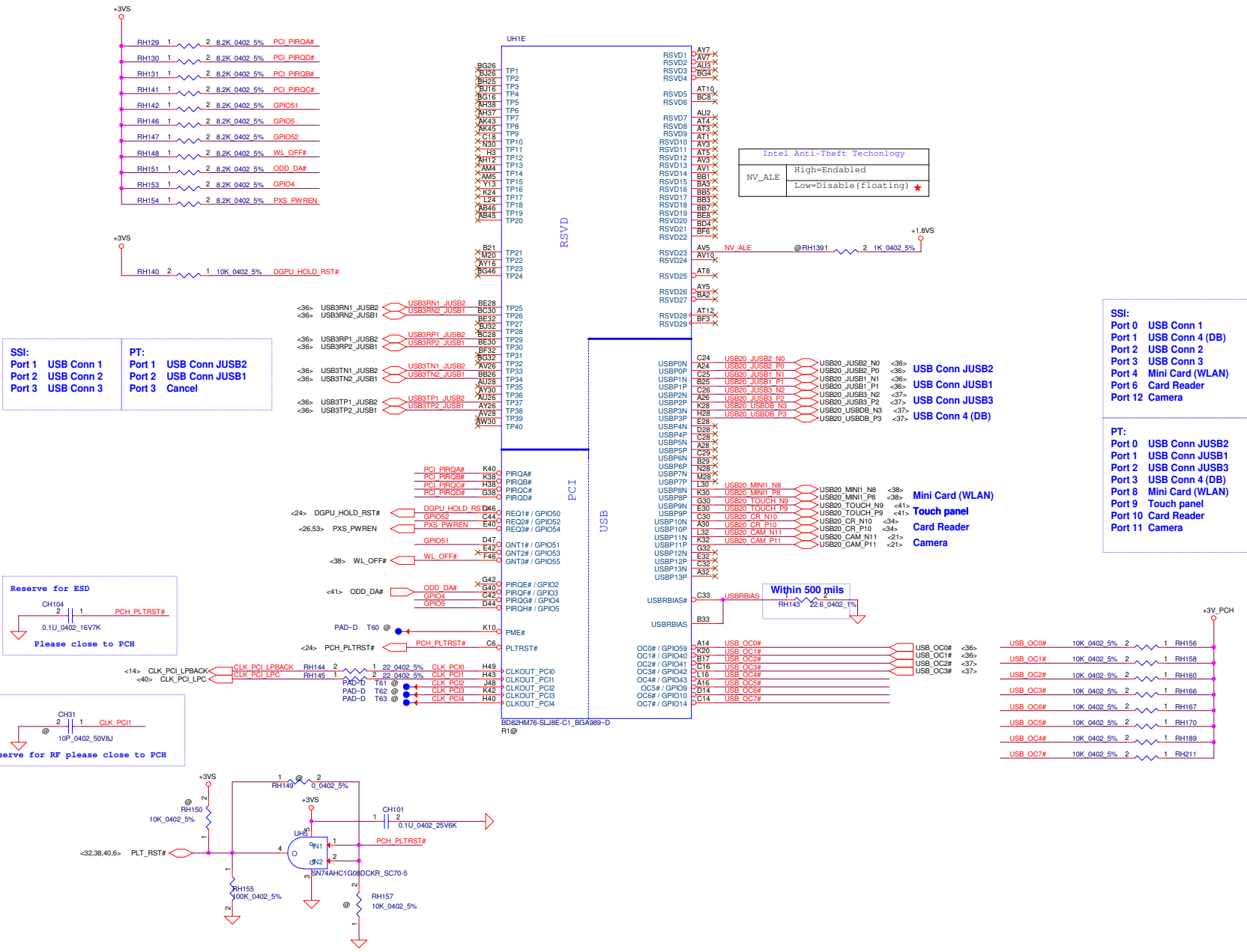


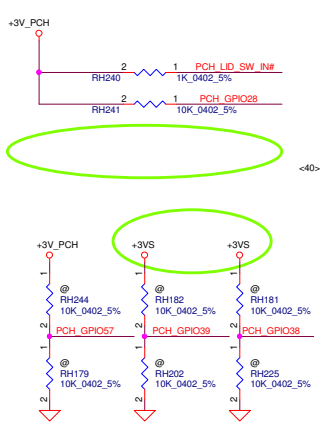
If use external clk gen, please place close to CLK gen else, please place close to PCH



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Issued Date	2012/08/22	Deciphered Date	2013/08/31	PCH (2/8) PCIE/SMBUS/CLK	
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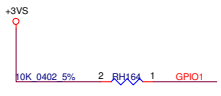






System ID

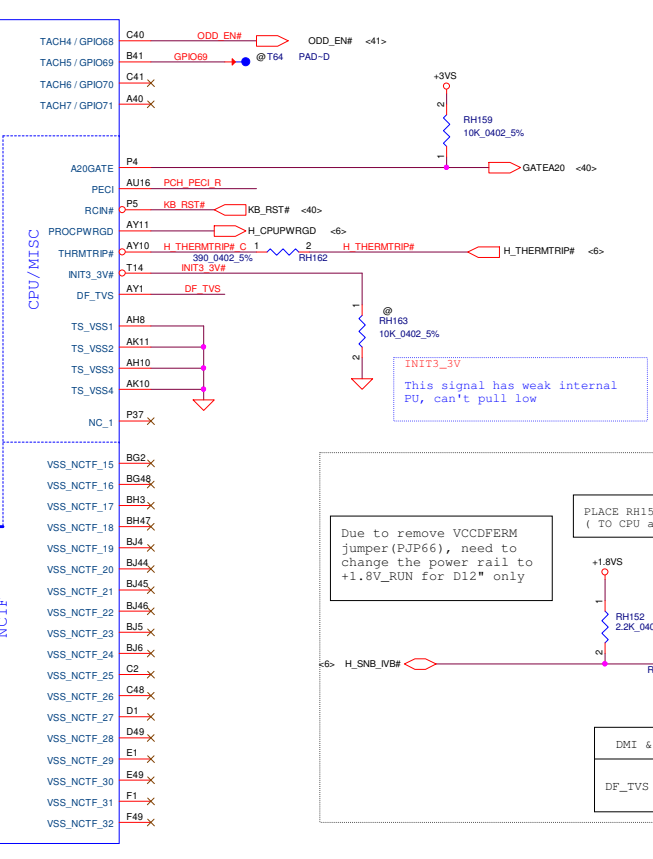
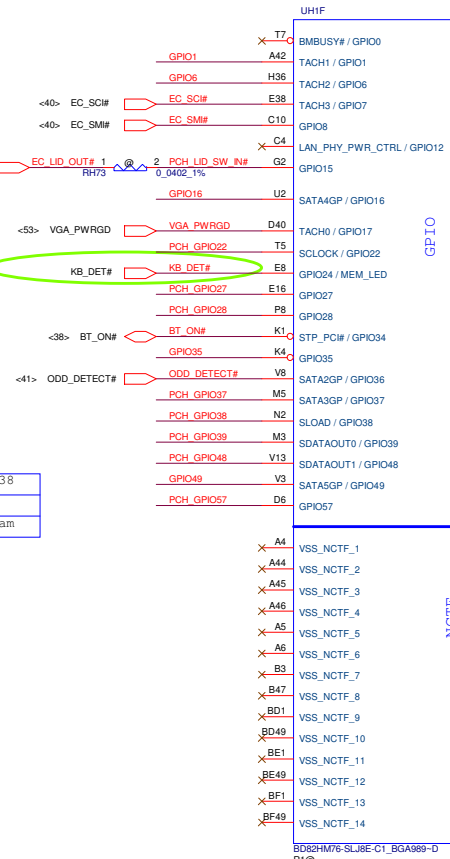
	PCH_GPIO57	PCH_GPIO39	PCH_GPIO38
LOW	VAW00 15''	INSPIRON	Entry
HIGH	VAW10 17''	VOSTRO	Mainstream



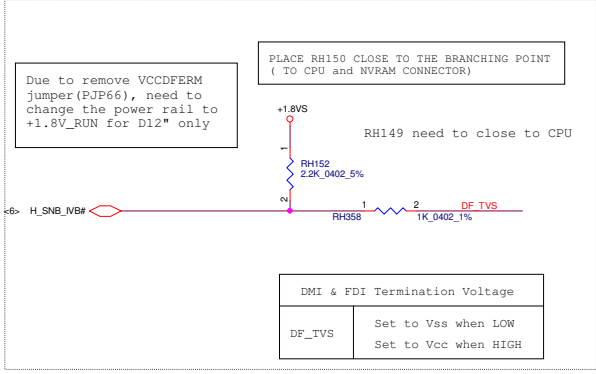
GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
* H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

PCH_GPIO37
FDI TERMINATION VOLTAGE OVERRIDE
* LOW - Tx, Rx terminated to same voltage (DC Coupling Mode)

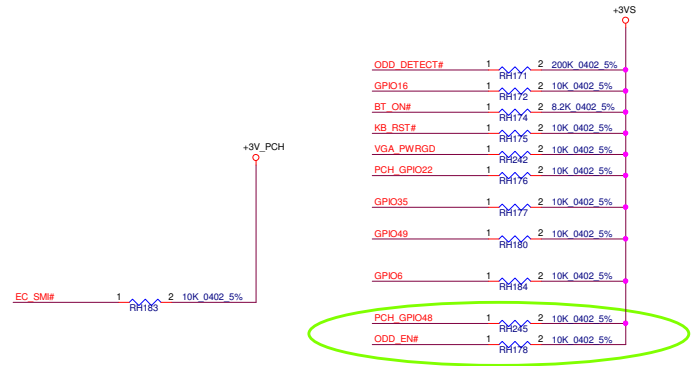
PCH_GPIO28 needs to be connected to XDP_FN8
PCH_GPIO35 needs to be connected to XDP_FN9
PCH_GPIO15 needs to be connected to XDP_FN16
Please refer to Huron River Debug Board DG 0.5

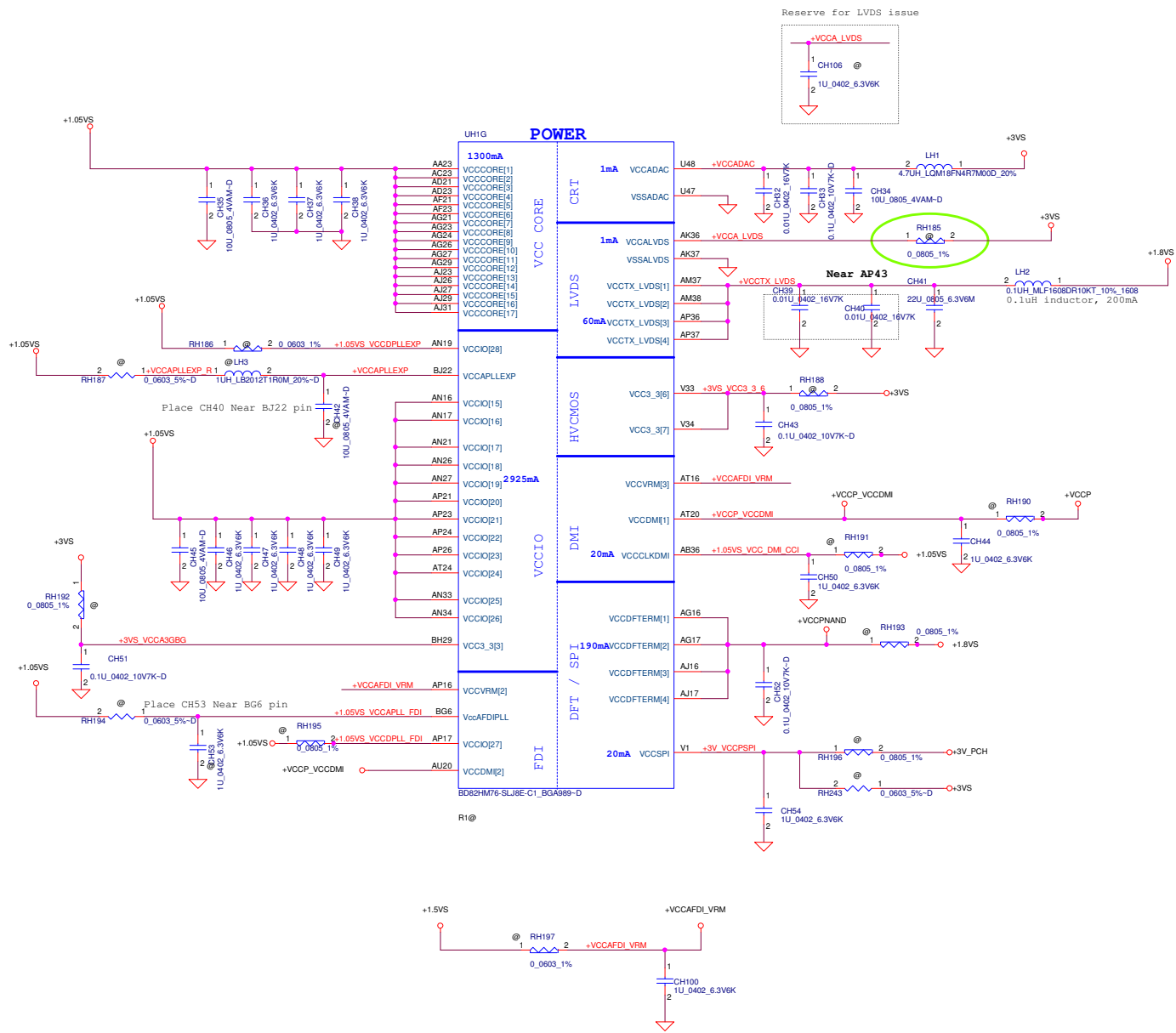


INIT3_3V
This signal has weak internal PU, can't pull low

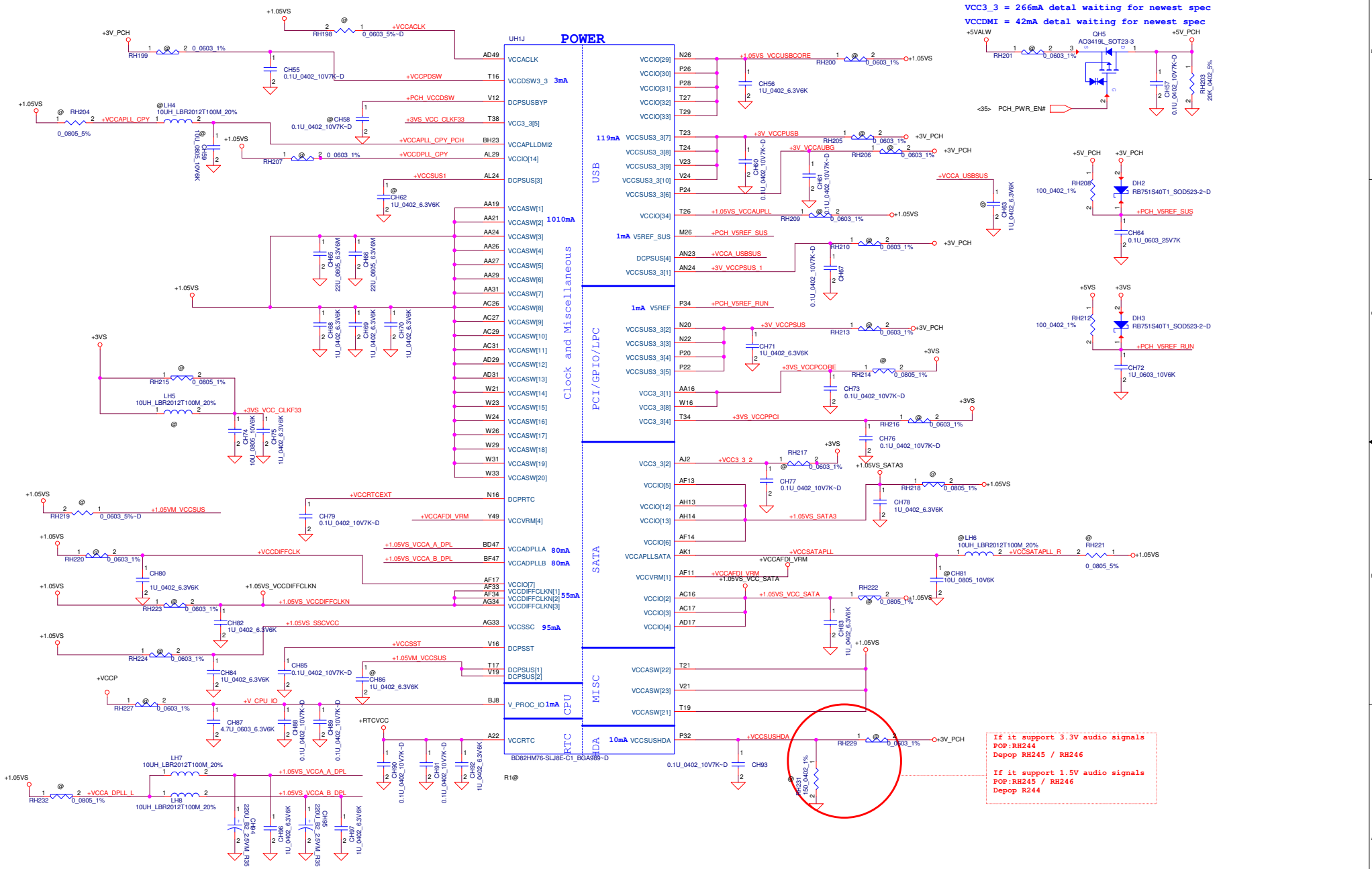


Place CH102 close to RH161 & PCH.

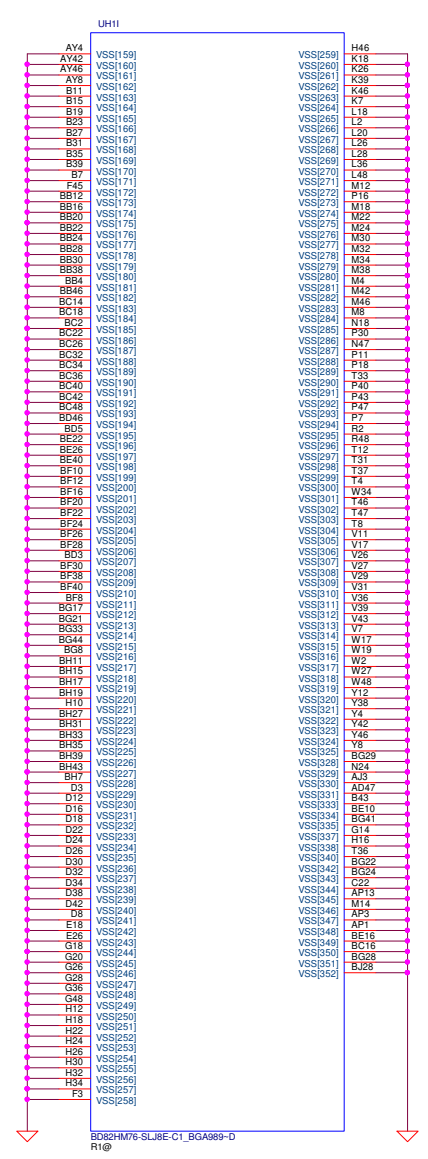
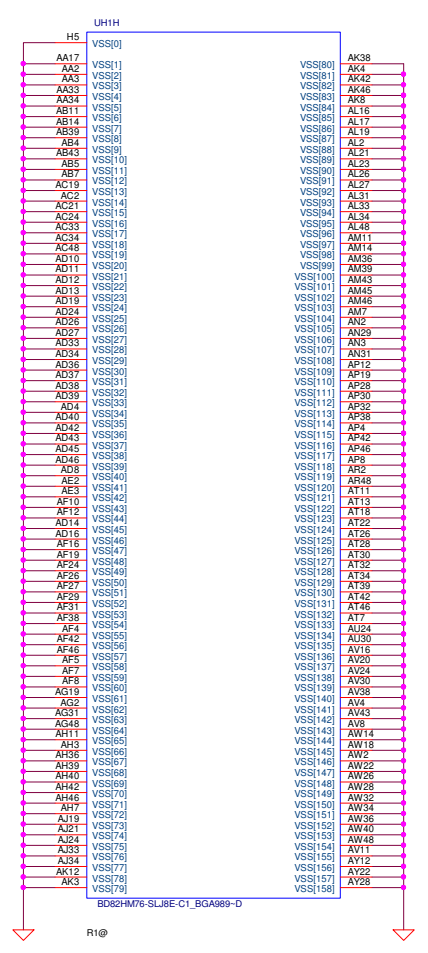




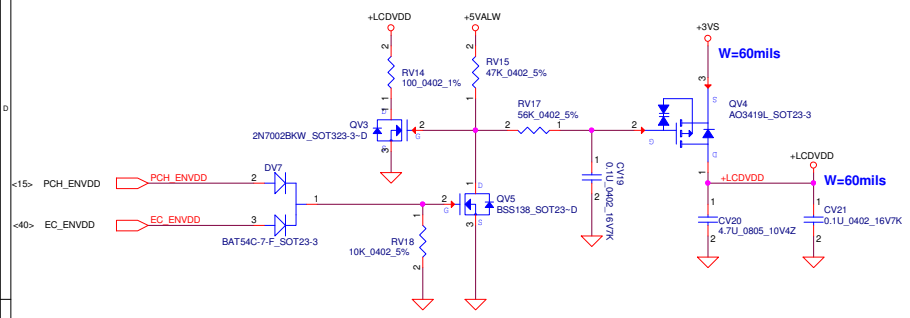
PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus_3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06



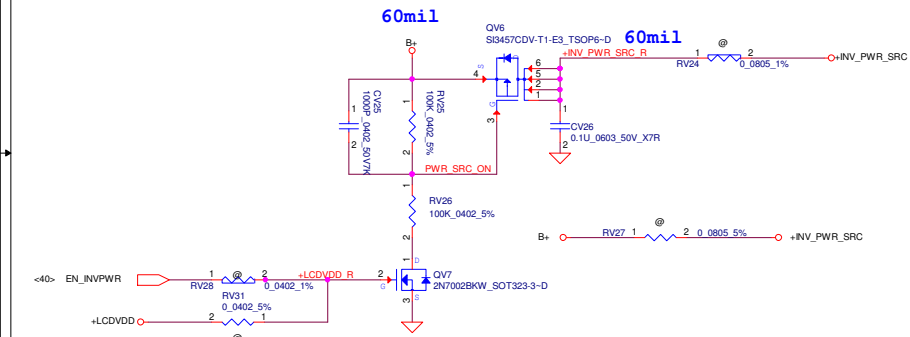
Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
Issued Date	2012/08/22	Deciphered Date	2013/08/31	PCH (7/8) PWR	
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			Date:	Wednesday, August 28, 2012	Sheet 19 of 57



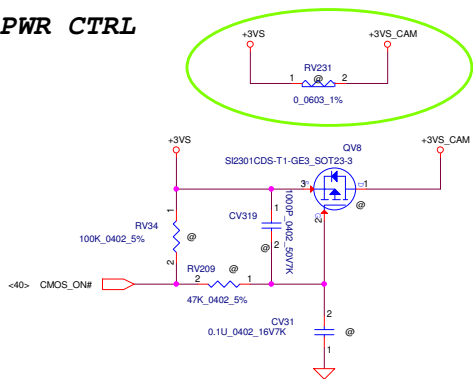
LCD PWR CTRL



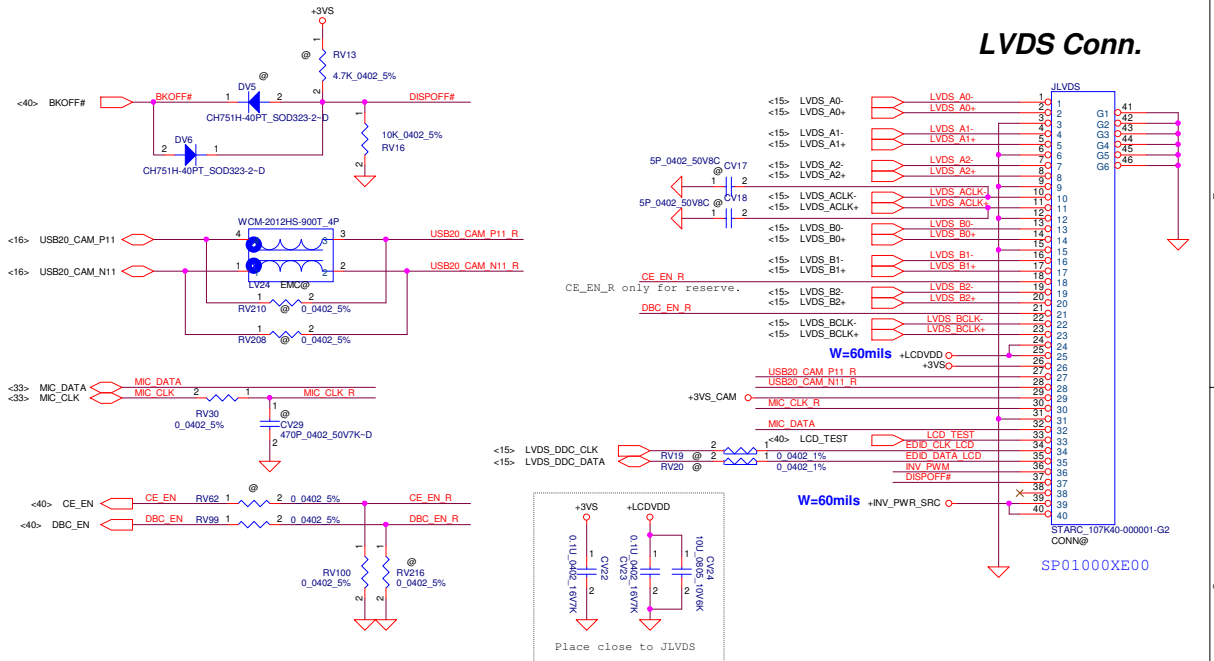
LCD backlight PWR CTRL



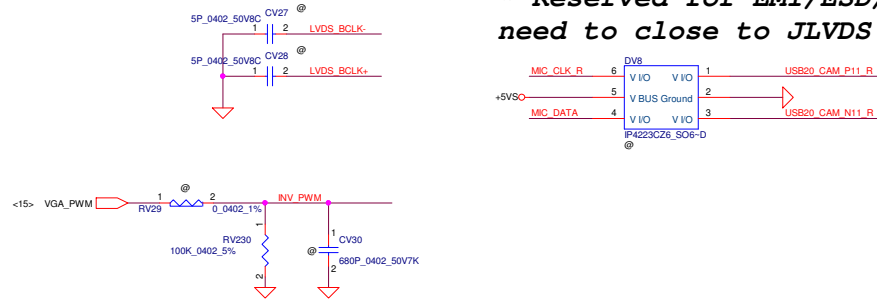
Webcam PWR CTRL



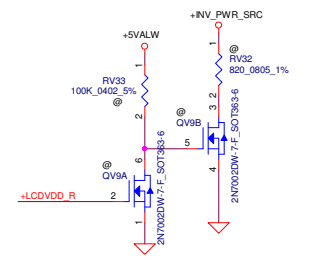
LVDS Conn.



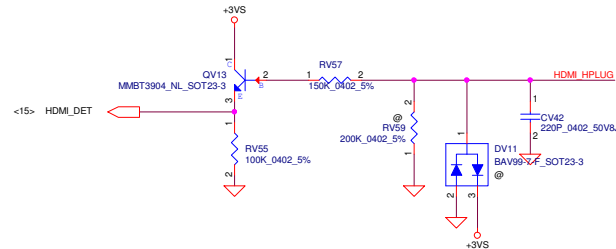
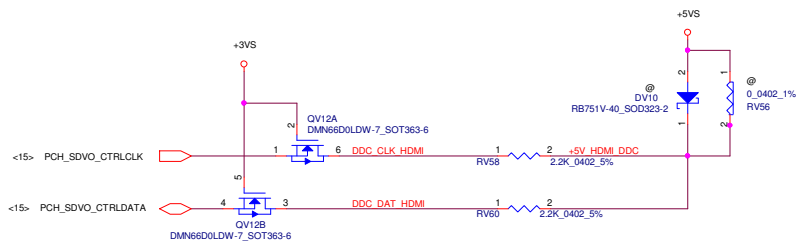
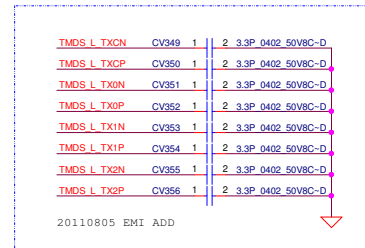
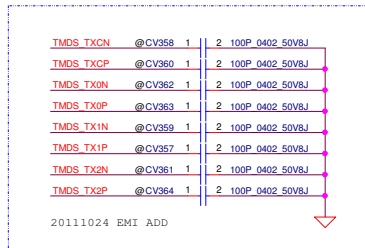
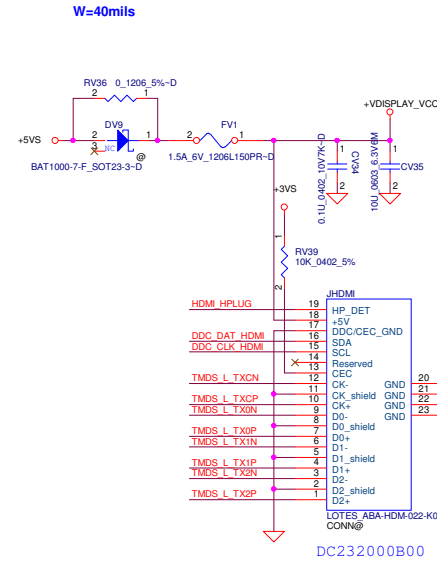
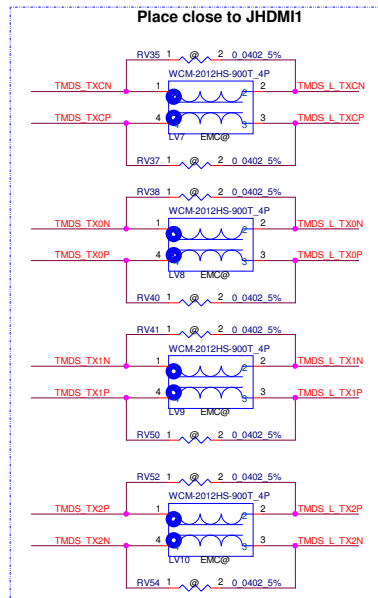
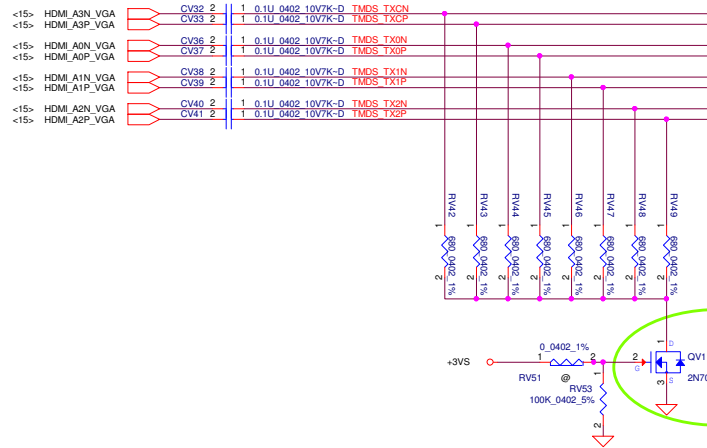
*** Reserved for EMI/ESD/RF need to close to JLVDS**



*** Reserved for LCD sequence tuning**

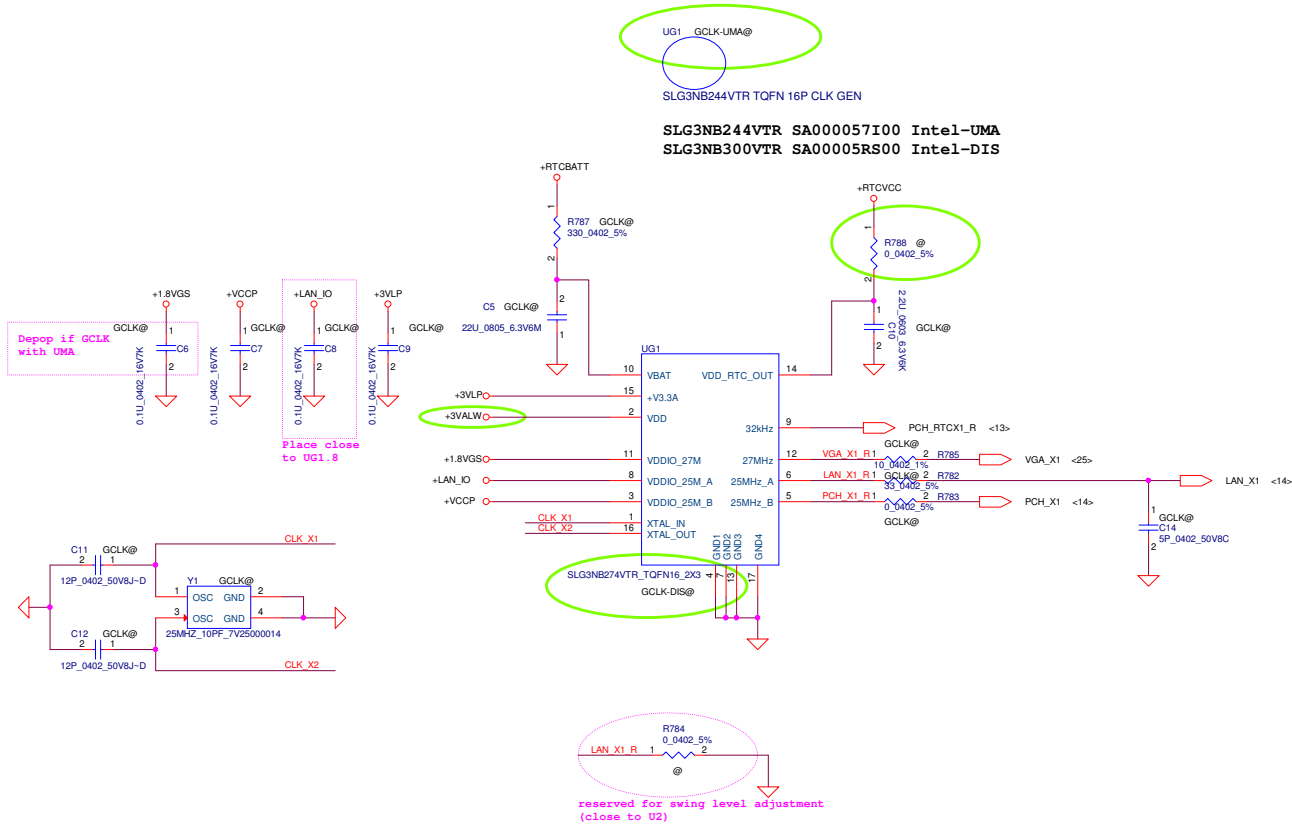


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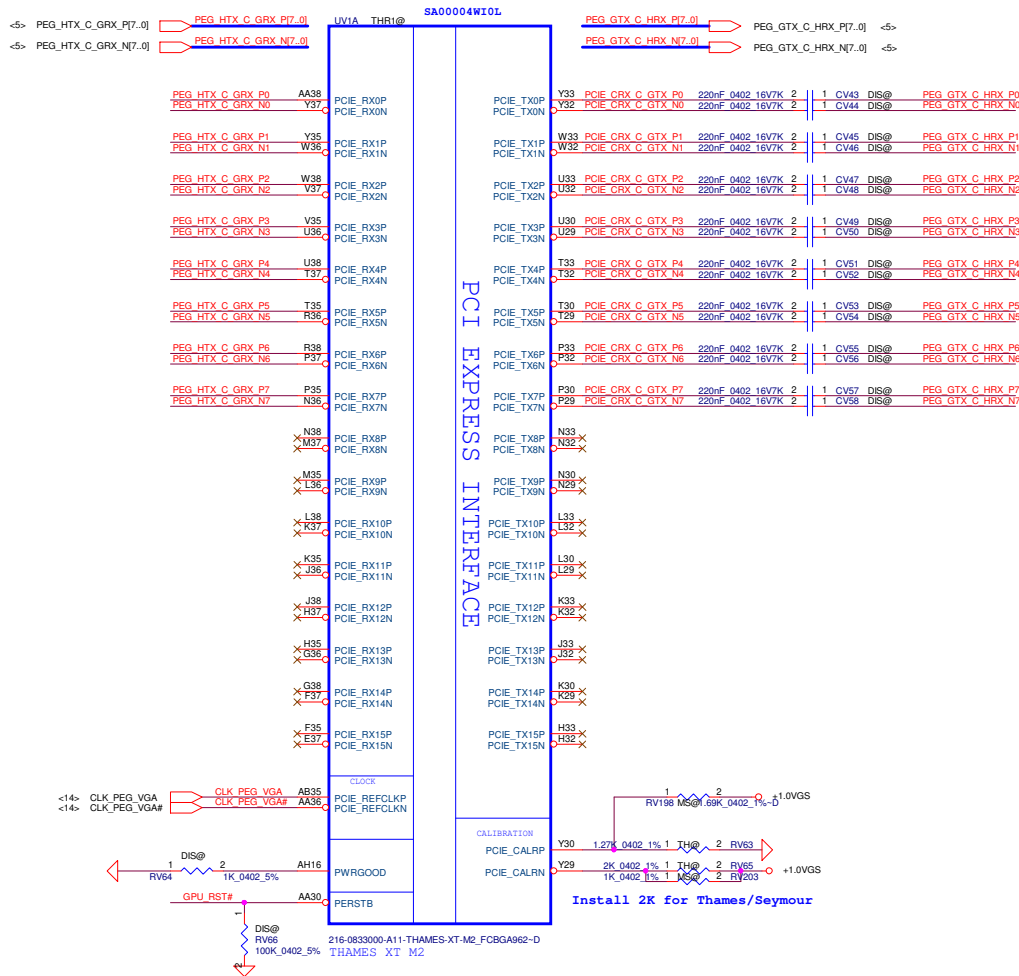
46@	ROYALTY HDMI W/LOGO
Part Number	Description
8000000023M	HDMI W/LogoR000000023M

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Date:	Wednesday, August 28, 2012	Sheet	22	of	57

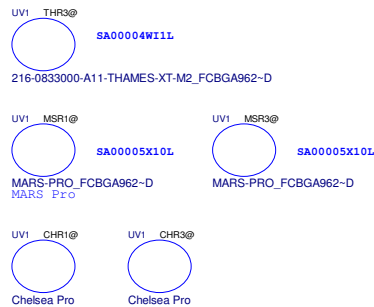
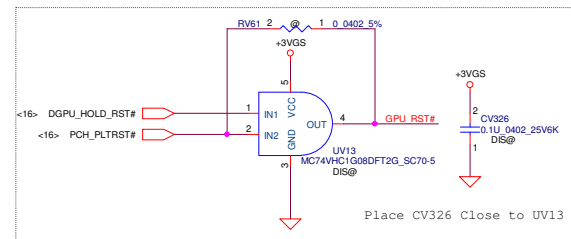
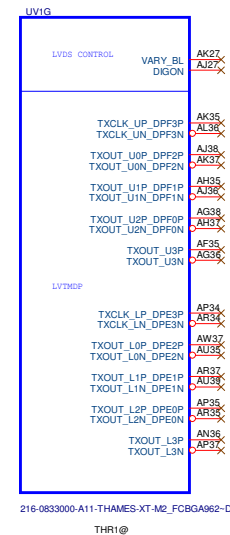


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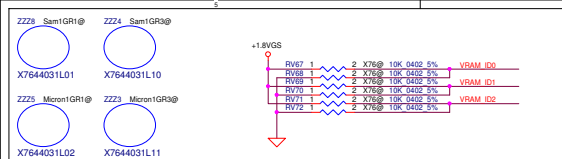
GFX PCIE LANE REVERSAL



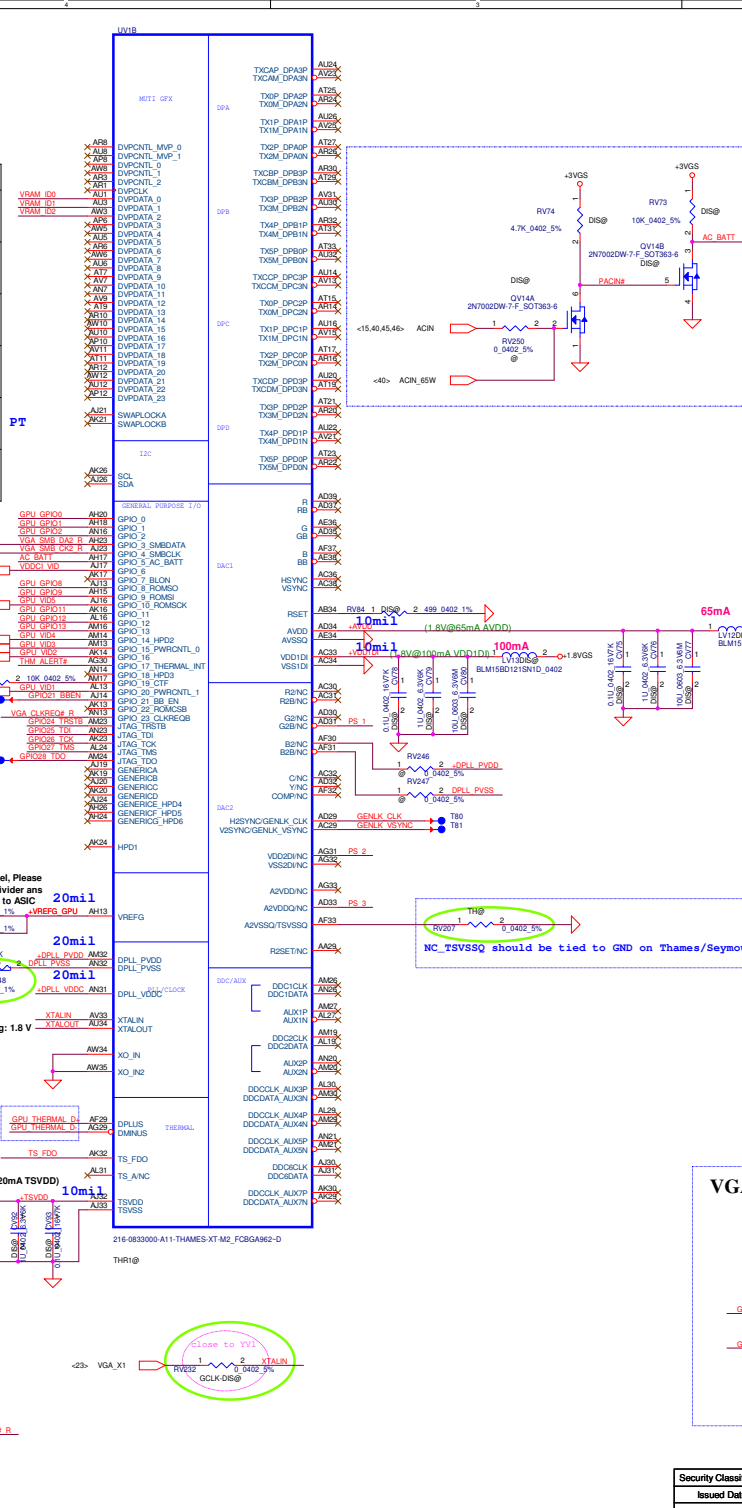
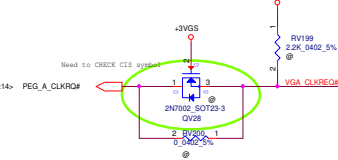
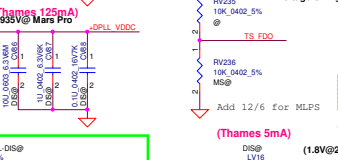
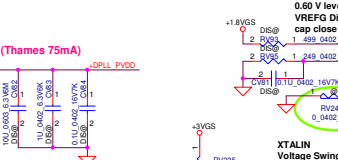
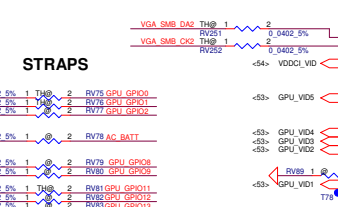
LVDS Interface



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Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2
Samsung 1GB SA00004GS1L(R1)	RV68	RV69	RV72
Samsung 1GB SA00004GS1L(R3)	0	1	0
Hynix 1GB SA000041S3L	RV67	RV70	RV72
Micron 1GB SA00004Y20L(R1)	RV67	RV69	RV71
Micron 1GB SA00004Y20L(R3)	1	1	1
Samsung 2GB SA00005SH1L(R1)	RV68	RV69	RV71
Samsung 2GB SA00005SH1L(R3)	0	1	1
Hynix 2GB SA00003Y02L(R1)	RV67	RV70	RV71
Hynix 2GB SA00003Y03L(R3)	1	0	1
Micron 2GB SA00005XB0L(R1)	RV68	RV69	RV71
Micron 2GB SA00005XB1L(R3)	0	1	1



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
 0 = DO NOT INSTALL RESISTOR
 1 = INSTALL 10K RESISTOR
 X = DESIGN DEPENDANT
 NA = NOT APPLICABLE

STRAPS	PN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWR5_ENB	GPIO0	GPIO FULL TX OUTPUT SWING	0: 50% swing 1: Full swing
TX_DEEMPH_EN	GPIO1	PCIe TRANSMITTER DE-EMPHASIS	0: disable 1: enable
RSVD	GPIO2	Advertise PCIe speed when compliance test	0: 2.5GT/s 1: 5.0GT/s
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0: disable 1: enable
ROMDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XXX
VP_DEVICE_STRAP_BNA	VS2VNC	IGNORE VIP DEVICE STRAPS	0
RSVD	HSYNCR	0	0
RSVD	GENERIC	0	0
AUD[1]	HSYNC	AUD[1]AUD[0] 0: No audio function 0: 1 Audio for DisplayPort and HDMI if dongle is detected 1: 0 Audio for DisplayPort only 1: 1 Audio for both DisplayPort and HDMI	11
AUD[0]	VS2VNC	0	0

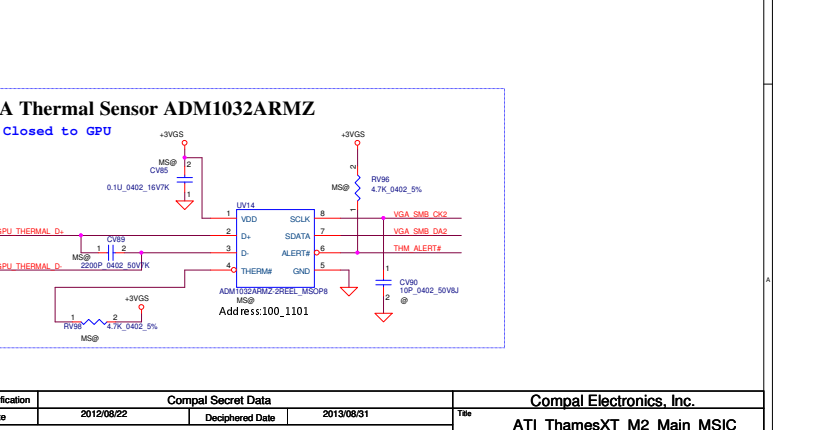
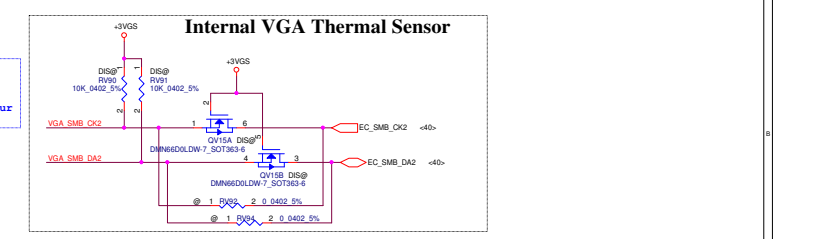
AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

GPIO21	HSYNC	GENERIC	GPIO2	GPIO8
--------	-------	---------	-------	-------

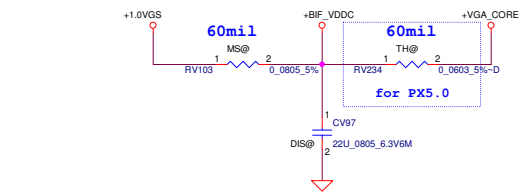
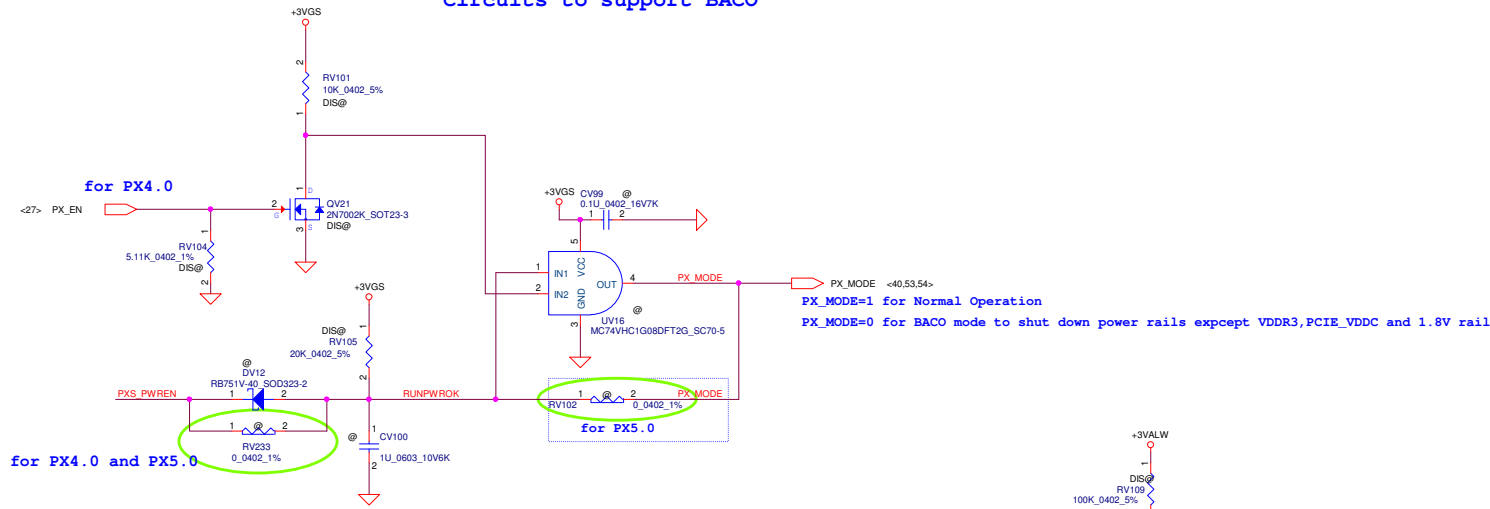


Mars Pro MLPs	RV241	RV242	BHs [3:1]
Hynix	NC	4.75k	000
Samsung	8.45k	2k	001
Micron	4.75k	NC	111

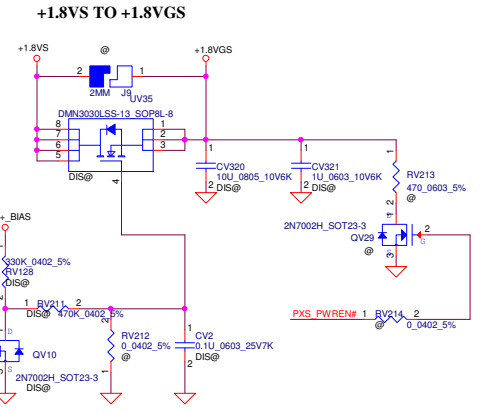
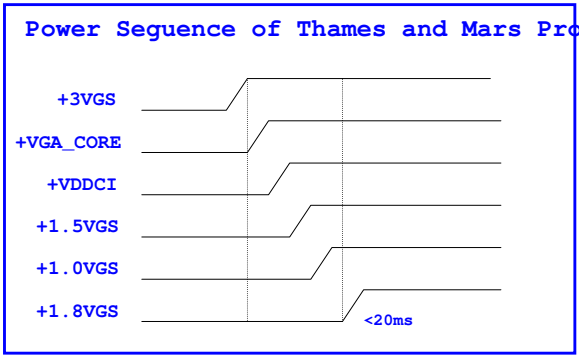


55mA@1.0V, in BACO mode

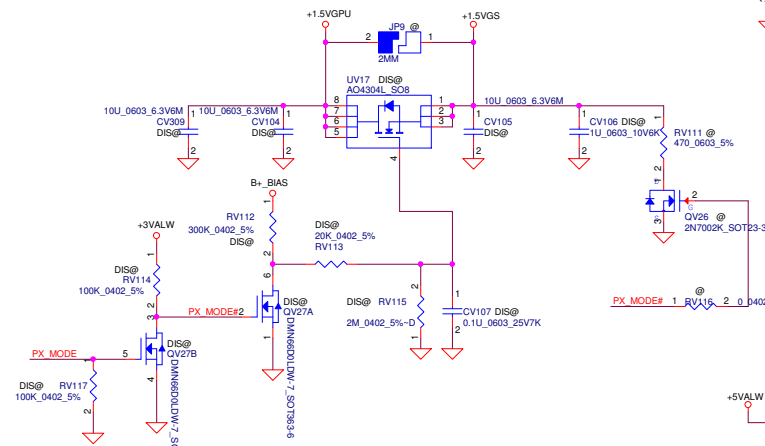
Circuits to support BACO



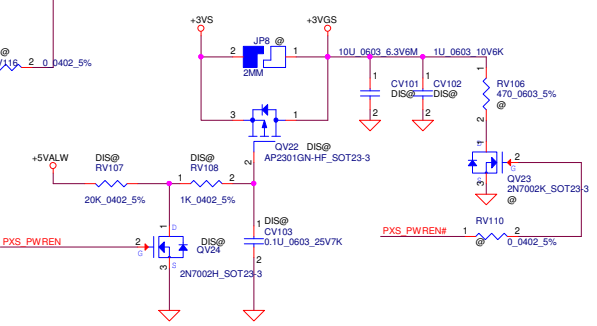
Note:
 PX4.0 +VGA_CORE, VDDCI, +1.5VGS ON
 PX4.0 +3VGS, +1.0VGS, +1.8VGS OFF
 PX5.0 +3VGS, +VGA_CORE, VDDCI, +1.5VGV, +1.0VGS, +1.8VGS OFF



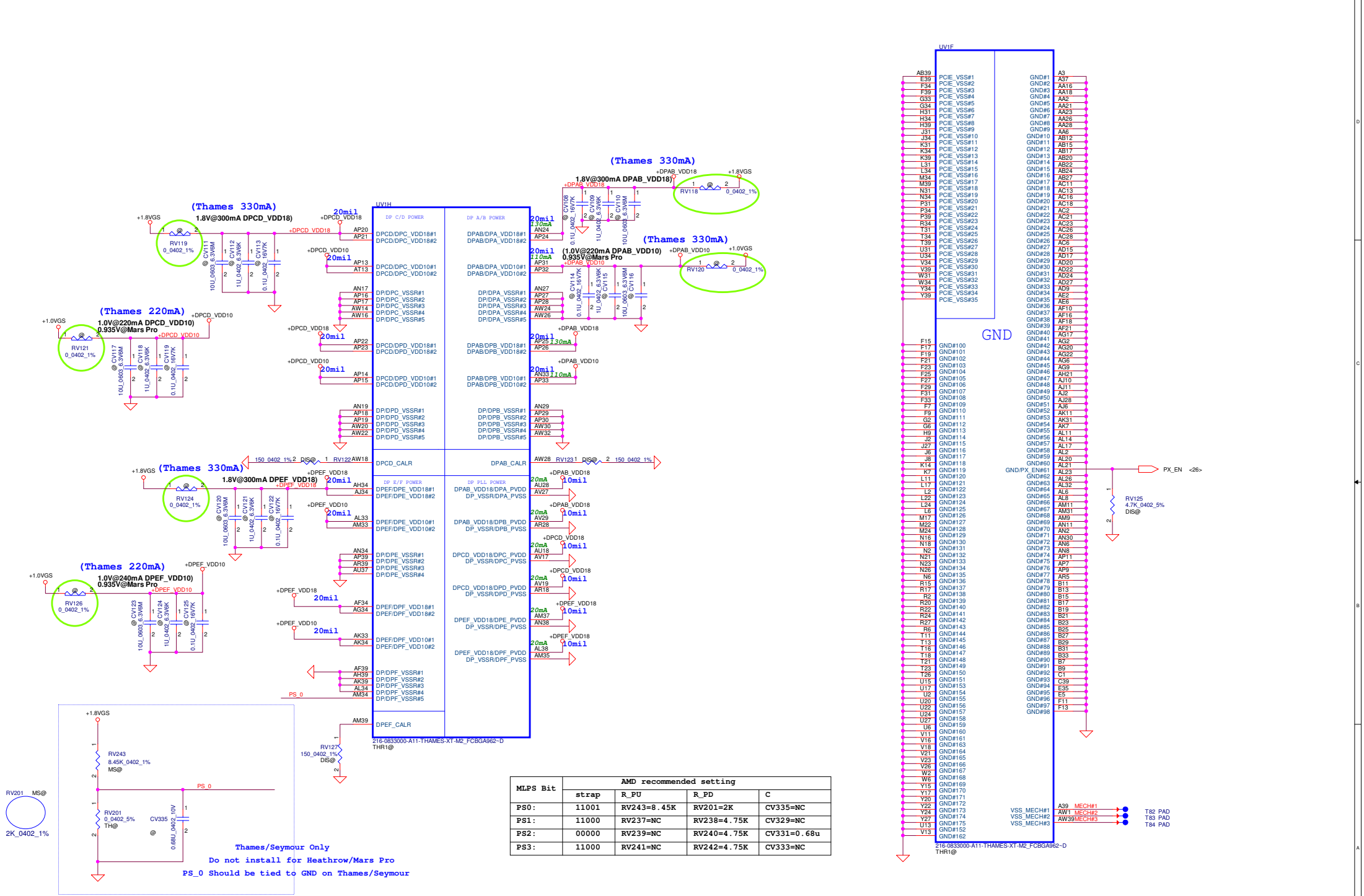
+1.5VGPU TO +1.5VGS



+3.3VS TO +3.3VGS

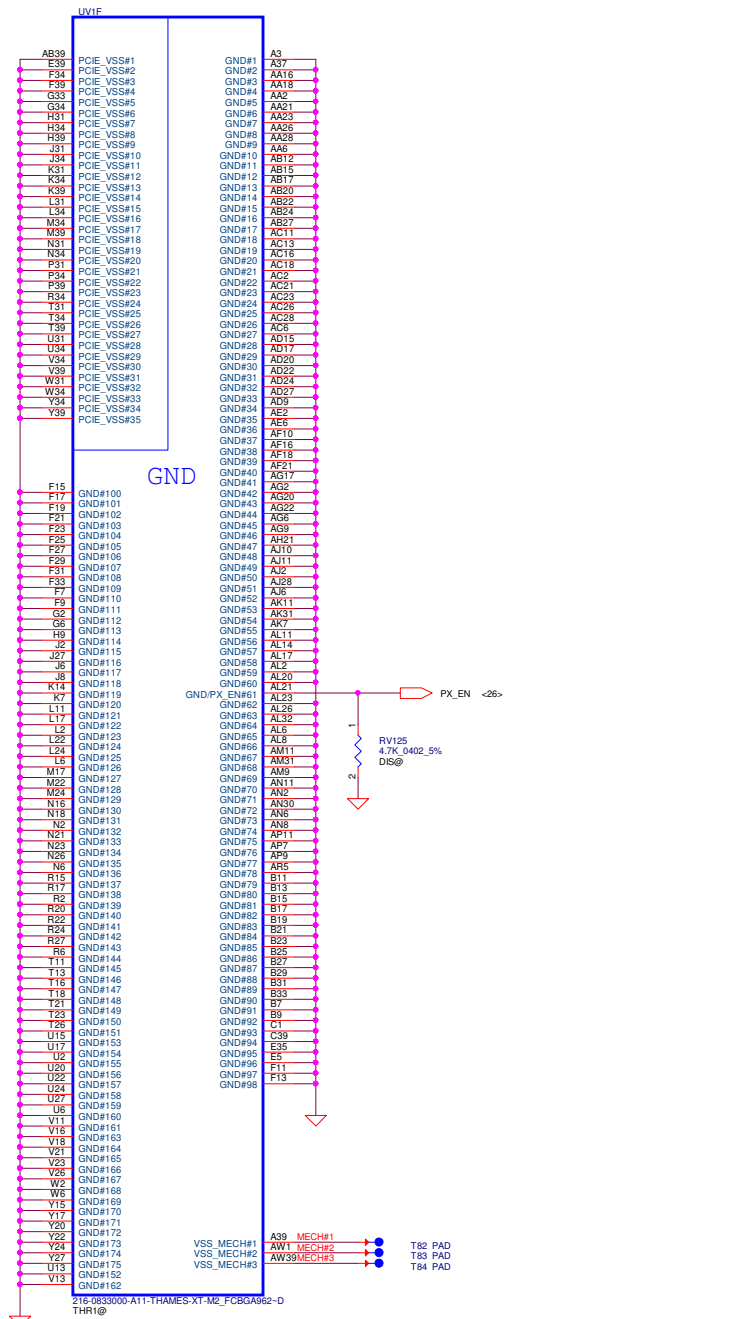


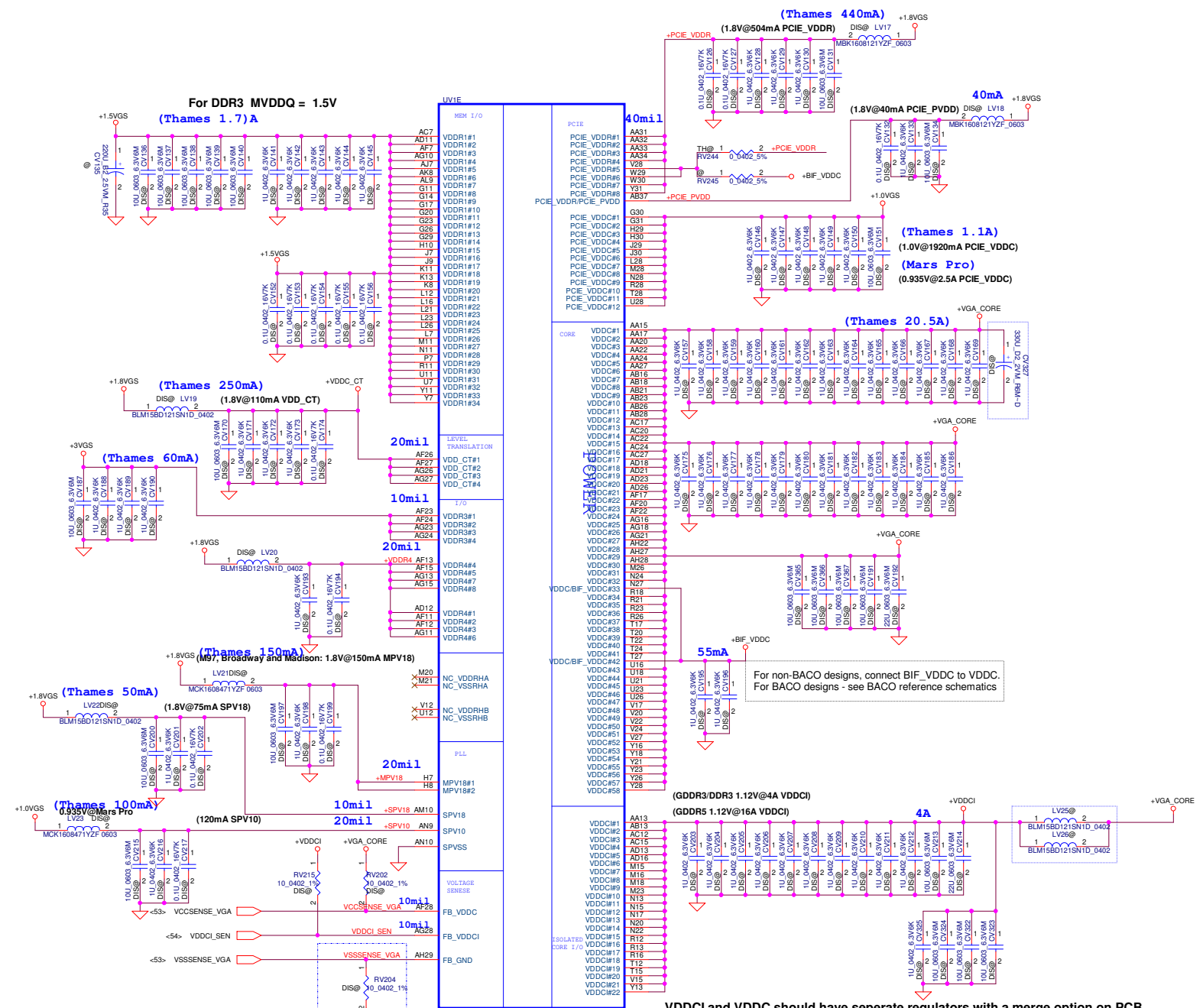
Security Classification	Compal Secret Data		Title	
Issued Date	2012/08/22	Deciphered Date	2013/08/31	ATI ThamesXT_M2_BACO POWER
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Date: Wednesday, August 28, 2012				Rev 1.0
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MLPS Bit	AMD recommended setting			
	strap	R_RU	R_FD	C
PS0:	11001	RV243=8.45K	RV201=2K	CV335=NC
PS1:	11000	RV237=NC	RV238=4.75K	CV329=NC
PS2:	00000	RV239=NC	RV240=4.75K	CV331=0.68u
PS3:	11000	RV241=NC	RV242=4.75K	CV333=NC

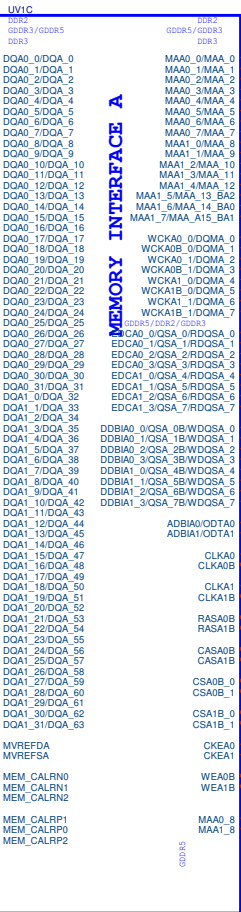
Thames/Seymour Only
Do not install for Heathrow/Mars Pro
PS_0 Should be tied to GND on Thames/Seymour



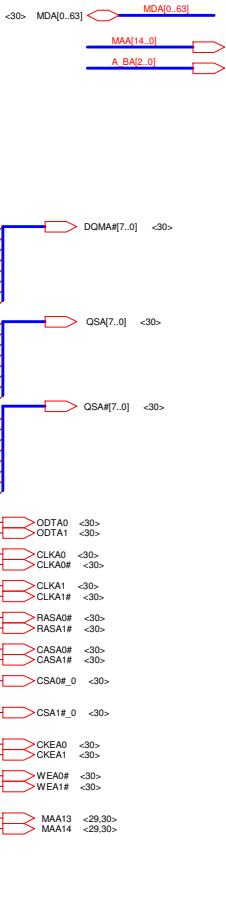


VDDCI and VDDC should have separate regulators with a merge option on PCB
 For Madison, Park, Capilano, Robson, Seymour and Whistler, VDDCI and VDDC can share one common regulator

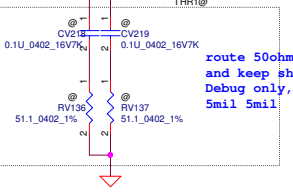
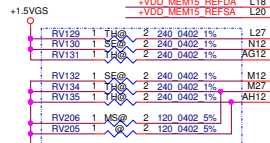
Security Classification	Compal Secret Data		Title	
Issued Date	2012/08/22	Deciphered Date	2013/08/31	ATI ThamesXT M2 Power
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Date:	Wednesday, August 28, 2012	Sheet	28	of 57



MEMORY INTERFACE A



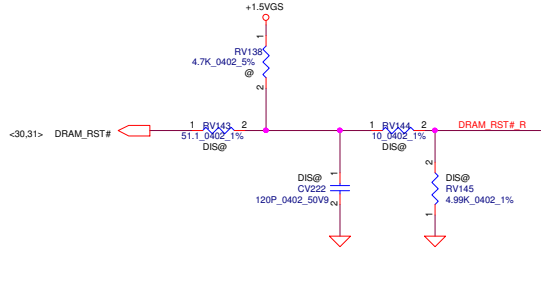
MEMORY INTERFACE B



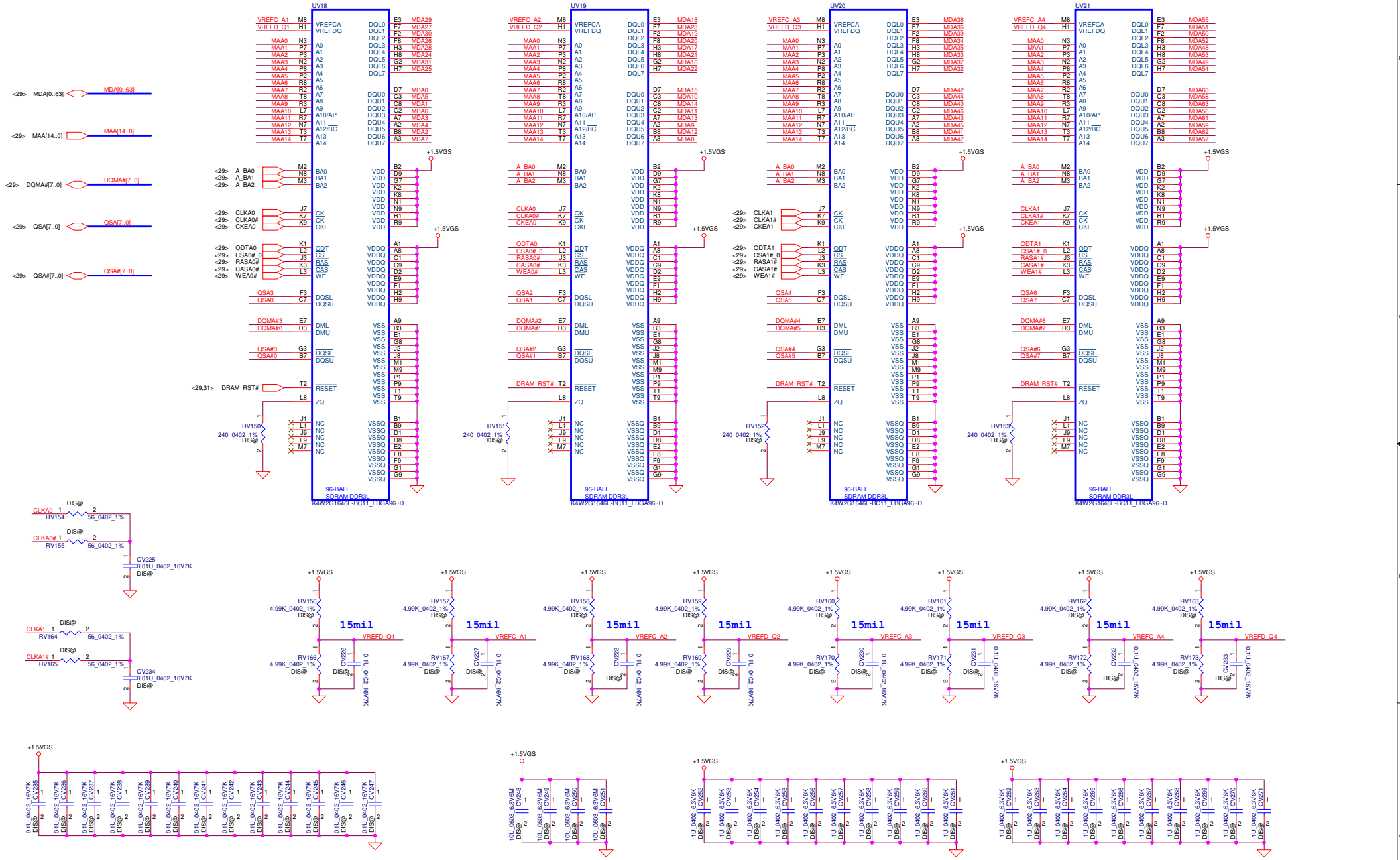
Co-lay Thames/Seymour/Mars Pro

	Thames M2	Seymour M2	Mars Pro
RV129	TH@	@	@
RV130	@	SE@	@
RV131	TH@	@	@
RV132	@	SE@	@
RV134	TH@	@	@
RV135	TH@	@	@
RV206	@	@	MS@
RV205	@	@	@

This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and |) Cap values will depend on the DRAM load and will have to be calculated for different Memory, DRAM load and board to pass Reset Signal Spec. Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2



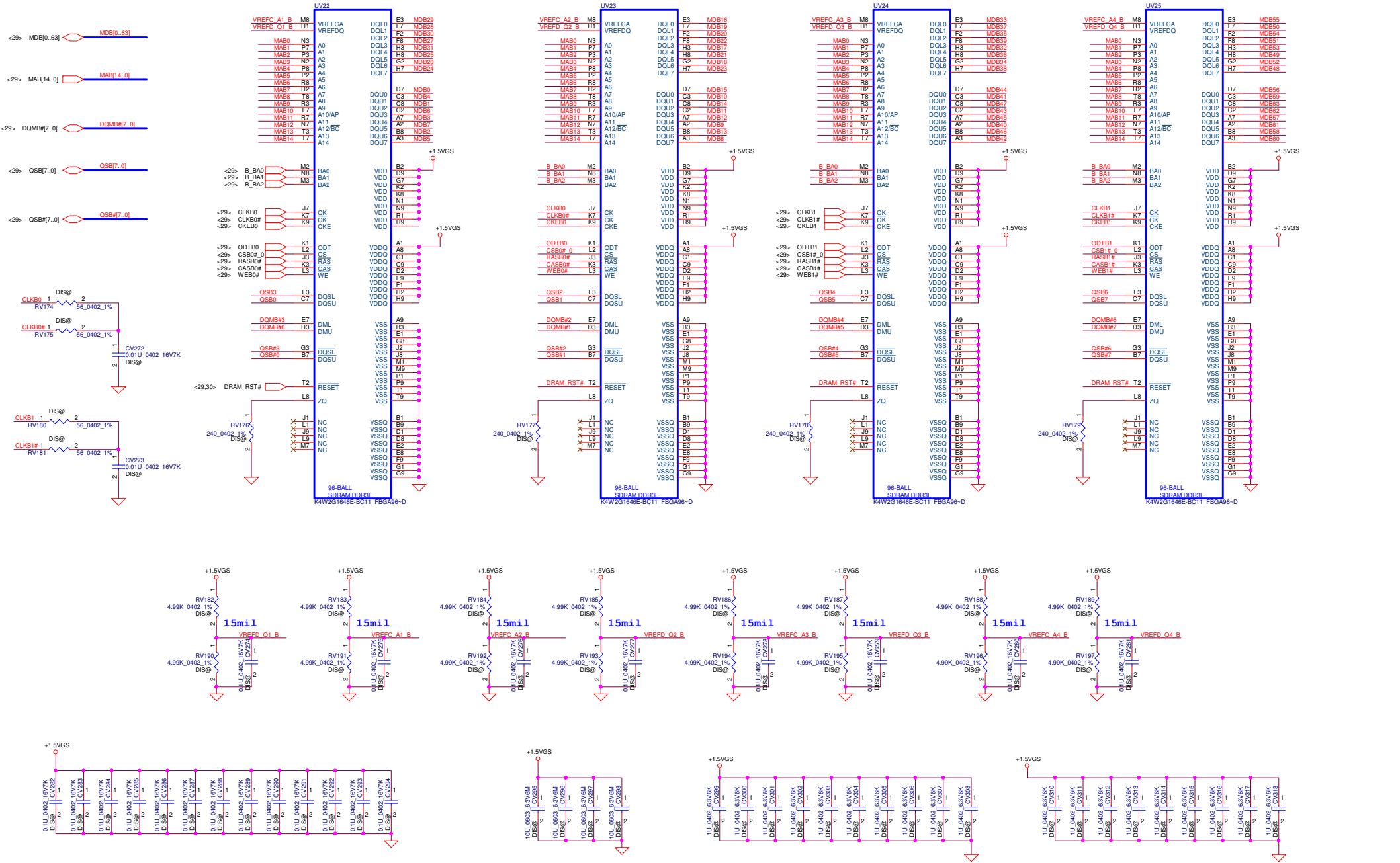
CHANNEL A: 256MB/512MB DDR3



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2012/08/22		2013/08/31		ATI ThamesXT M2 VRAM A	
Size		Document Number		LA-9104P	
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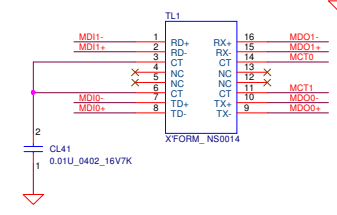
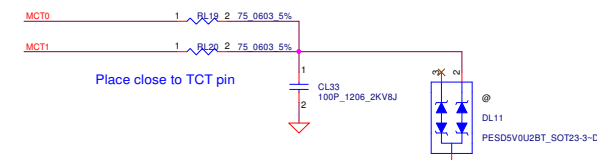
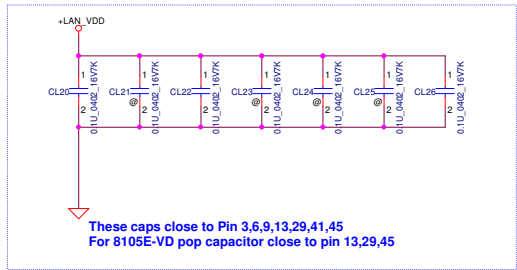
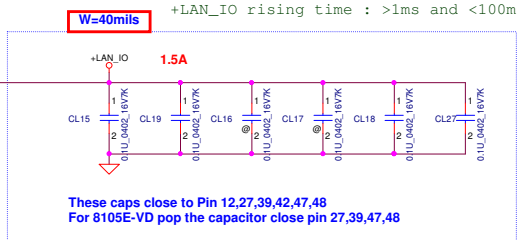
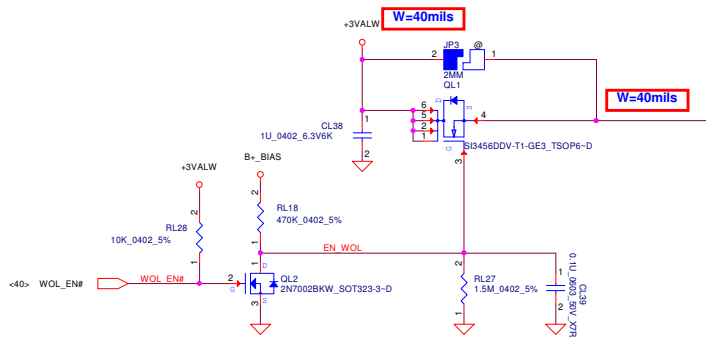
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CHANNEL B : 256MB/512MB DDR3

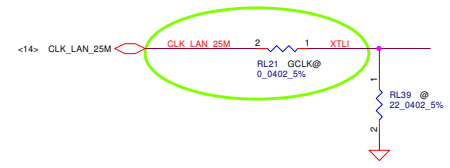
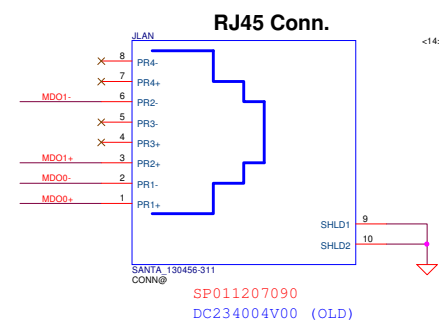
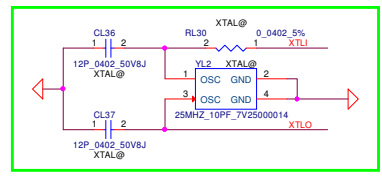
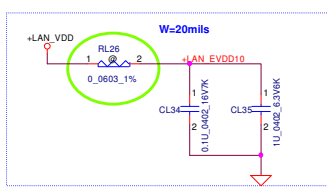
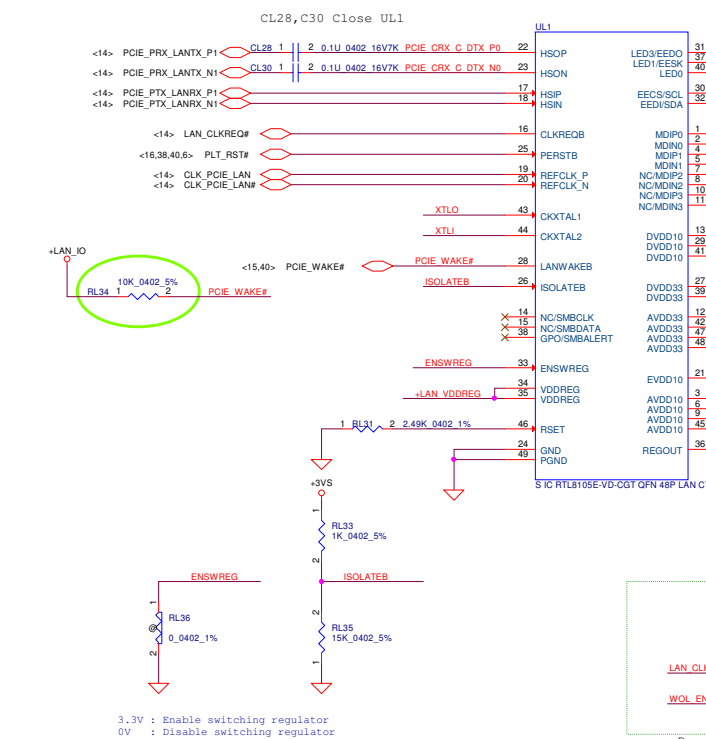


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Compal Electronics, Inc.
ATI ThamesXT M2 VRAM B
 LA-9104P

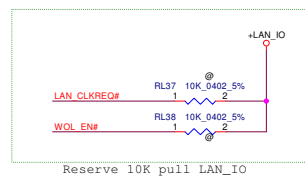


DL11 as close as possible to C27 and C32

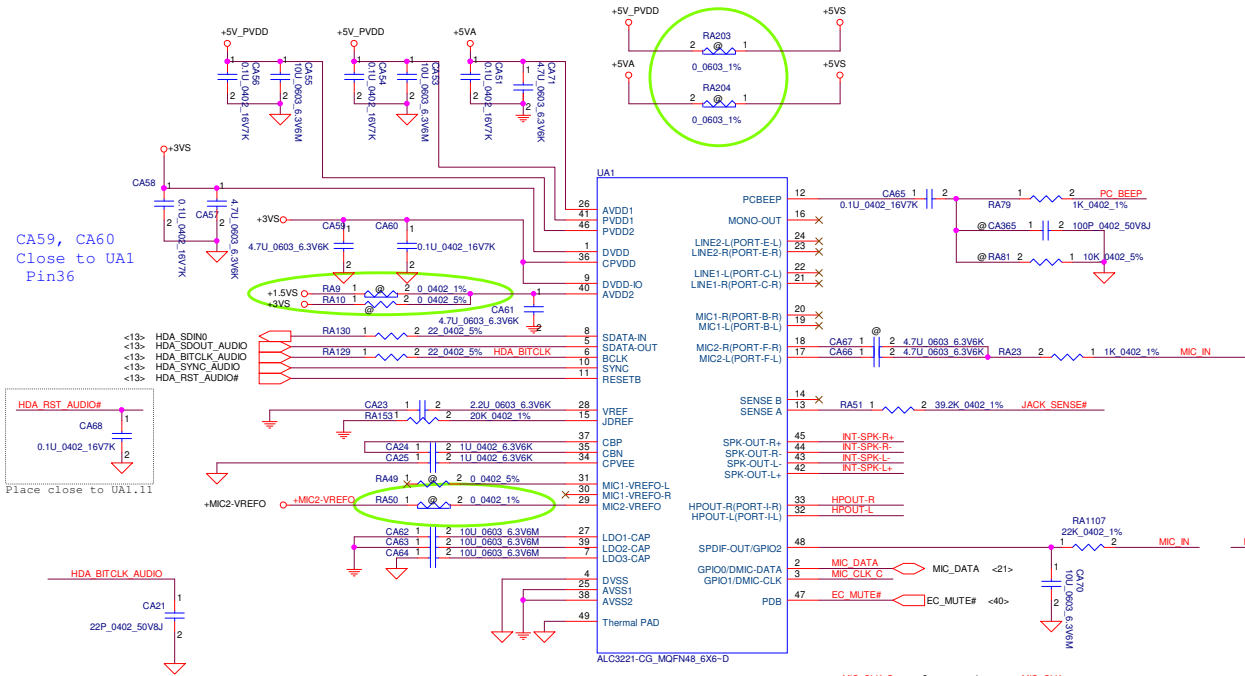


3.3V : Enable switching regulator
0V : Disable switching regulator

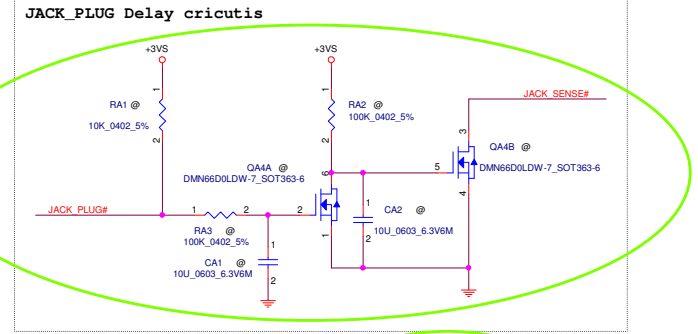
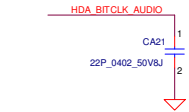
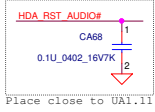
10/100 : 100@ (LDO mode used)



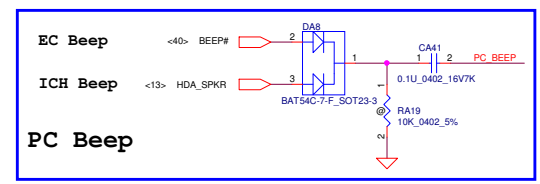
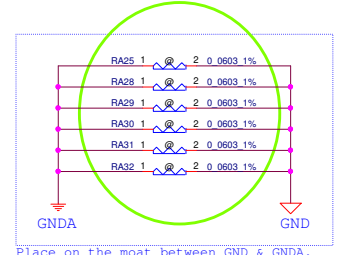
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Size	Document Number LA-9104P	Rev 1.0	Date: Wednesday, August 29, 2012 Sheet 32 of 57



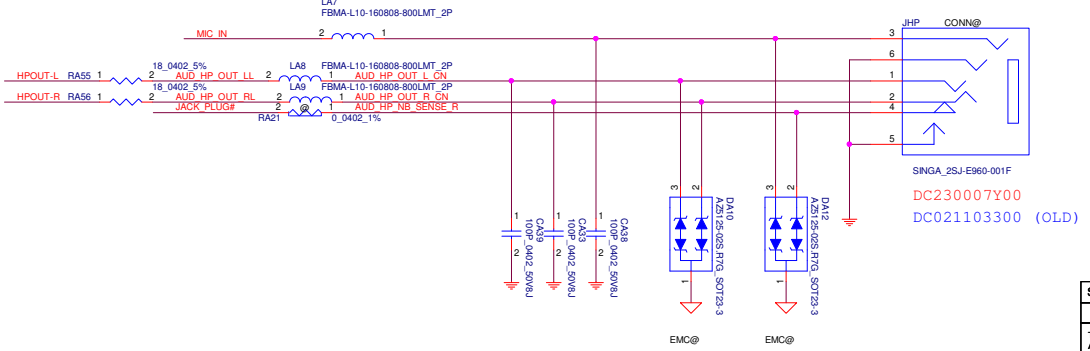
CA59, CA60
Close to UA1
Pin36



Reserve for cancel Delay circuitis

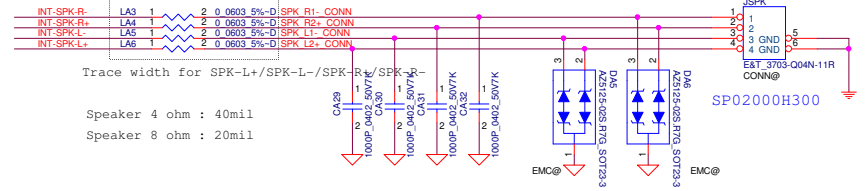


iPhone type Combo Jack



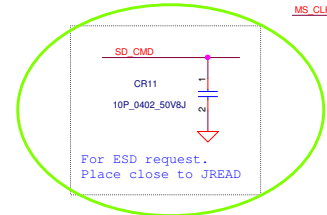
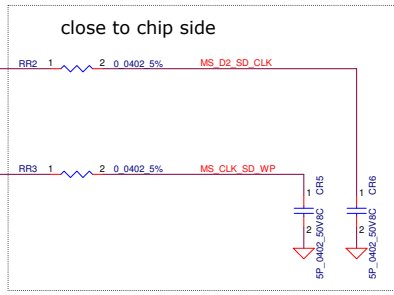
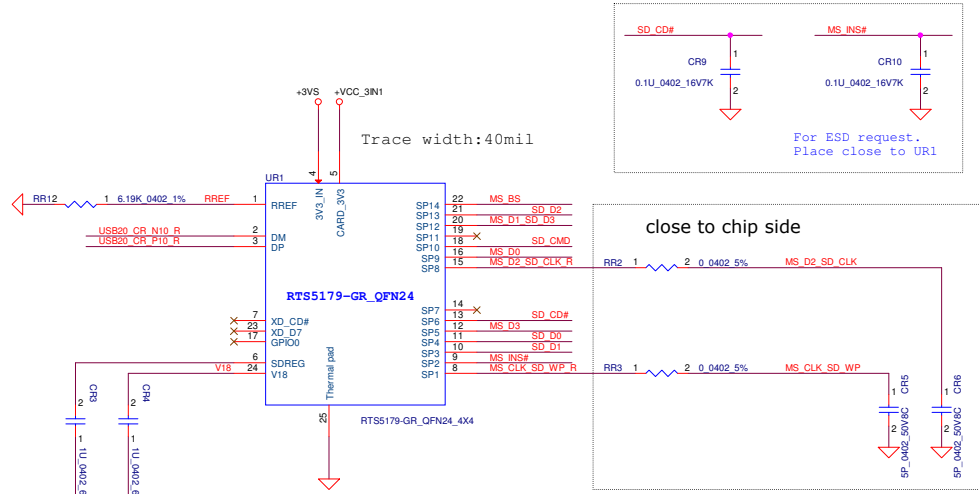
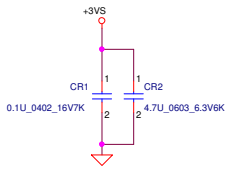
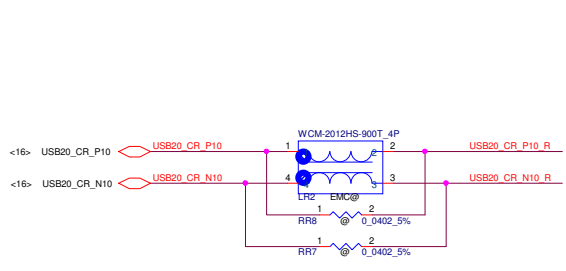
Close to UA1
Pin11,13,14,16

close to Codec



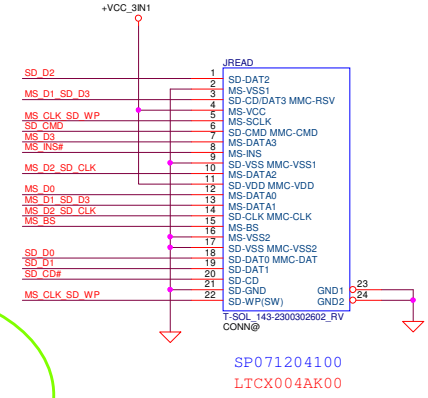
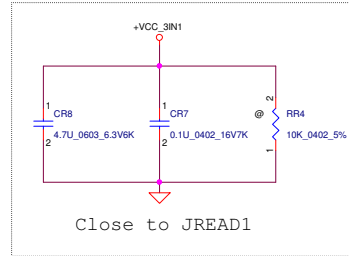
Speaker 4 ohm : 40mil
Speaker 8 ohm : 20mil

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拉MS_D2_SD_CLK到Conn pin 13 SD_CLK
再打Via拉到pin 10 MS_D2

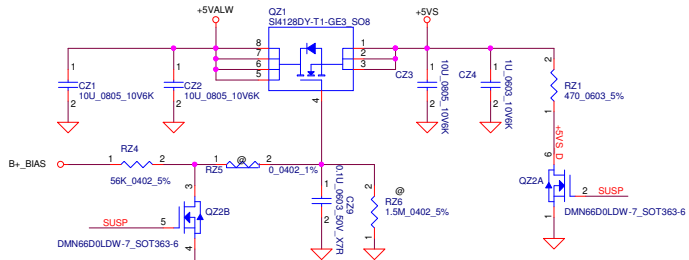
拉MS_CLK_SD_WP到Conn pin 5 MS_CLK
再打Via拉到pin 20 SD_W



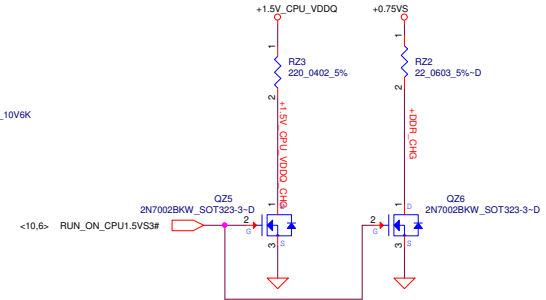
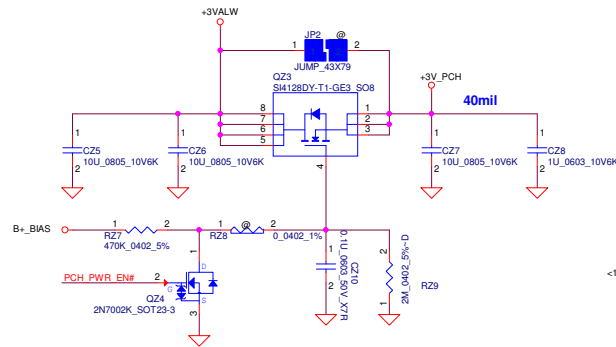
SP071204100
LTCX004AK00

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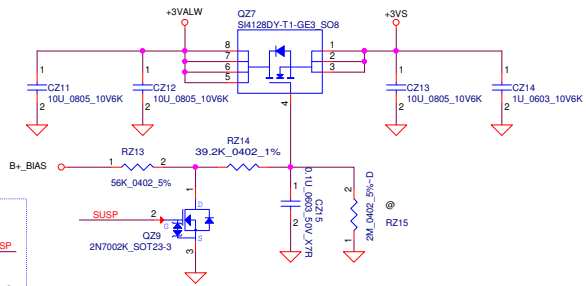
+5VALW to +5VS



+3VALW to +3V_PCH

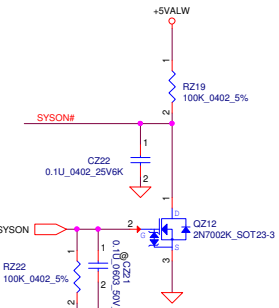
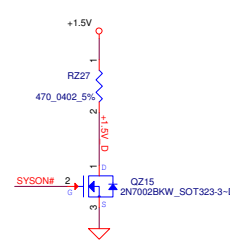
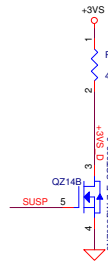
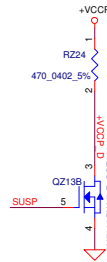
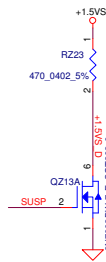
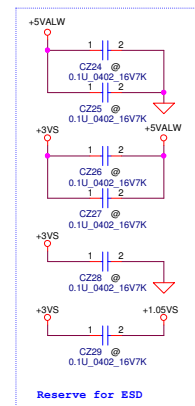
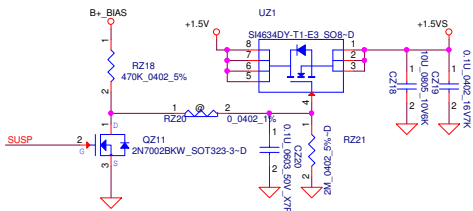


+3VALW to +3VS

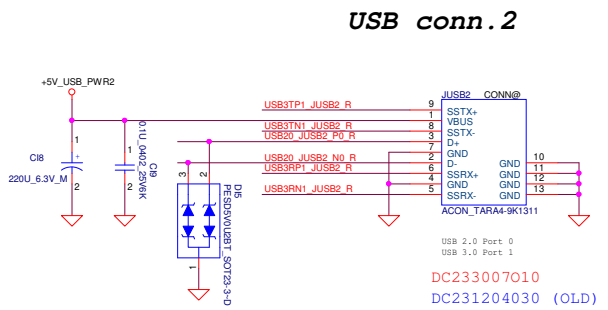
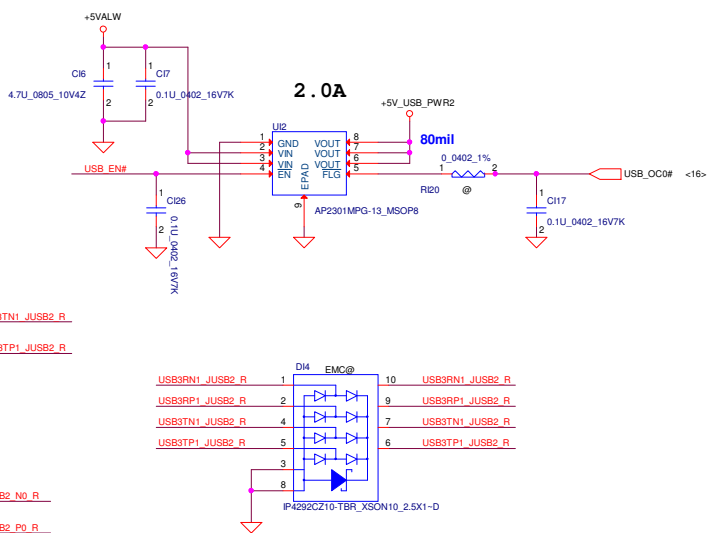
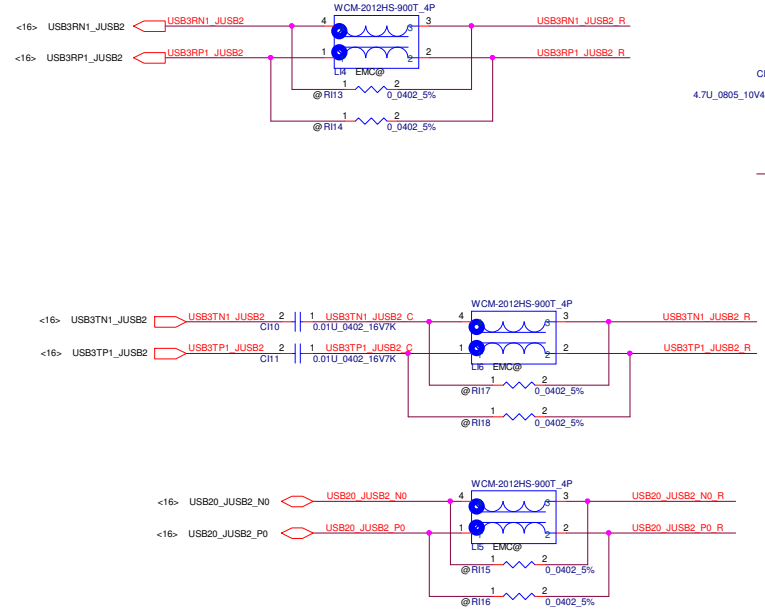
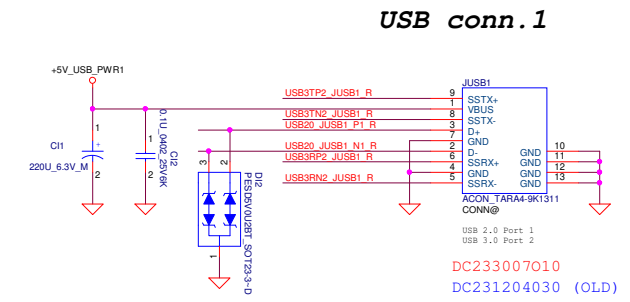
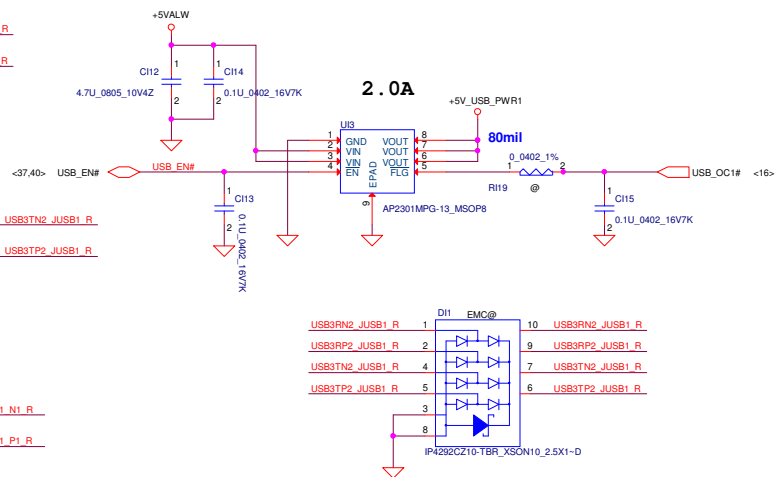
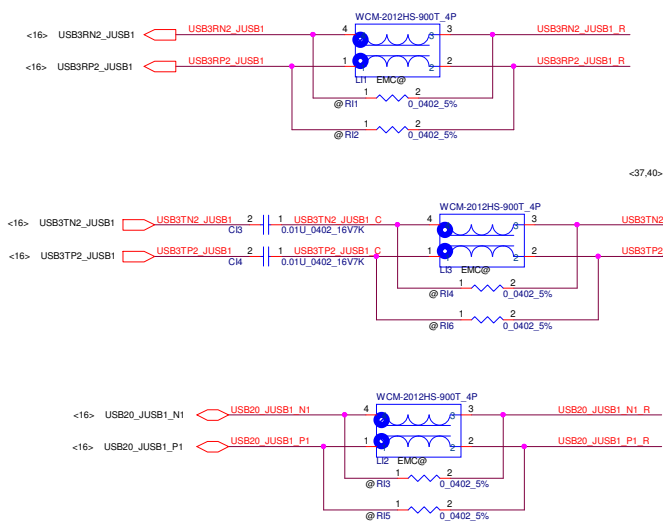


Reserve for ESD
CZ23
0.1U_0402_16V7K
Please close to QZ9

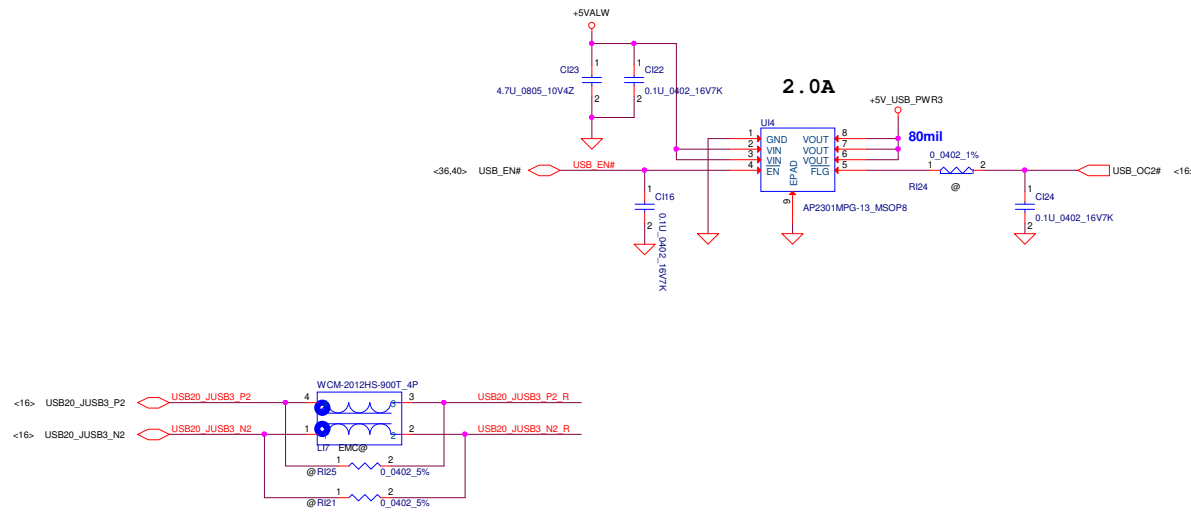
+1.5V To +1.5VS



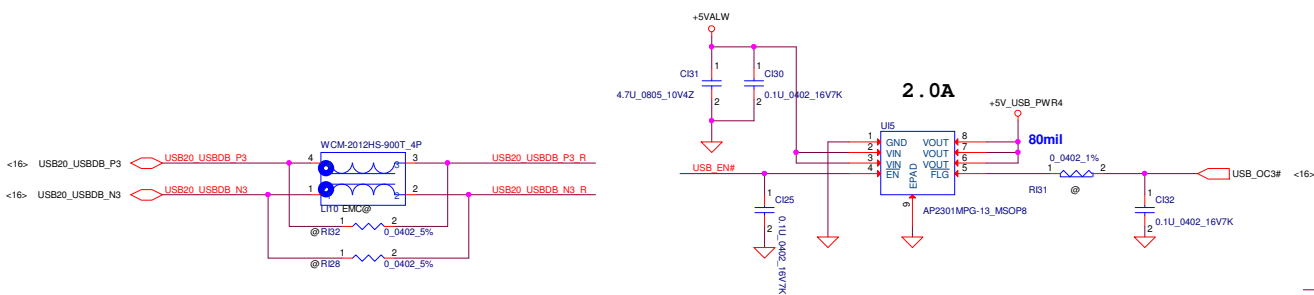
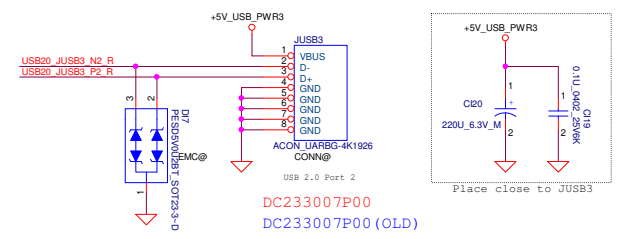
Security Classification	Compal Secret Data		Title	
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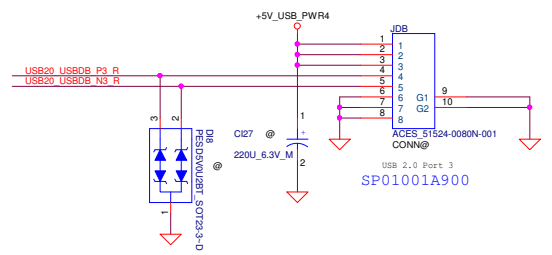
Security Classification		Compal Secret Data		Title	
Issued Date	2012/08/22	Deciphered Date	2013/08/31	USB3.0	
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USB conn. 3

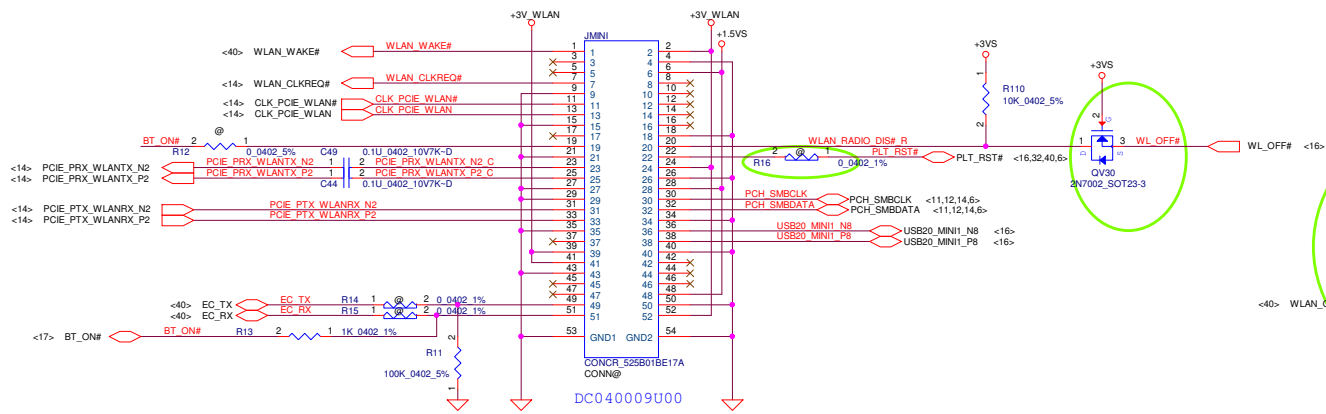


USB conn. 4

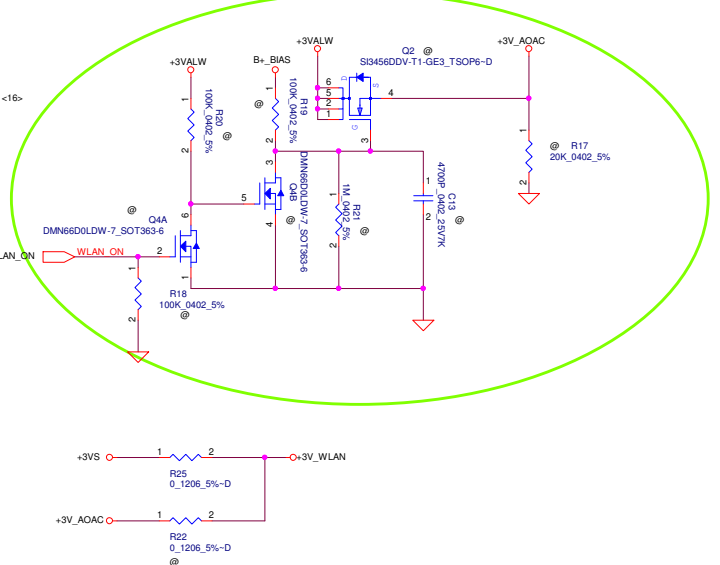


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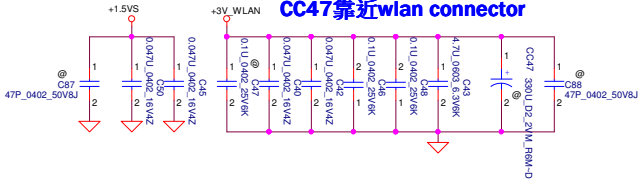
Mini WLAN/WIMAX H=6.7



Power Control for Mini card



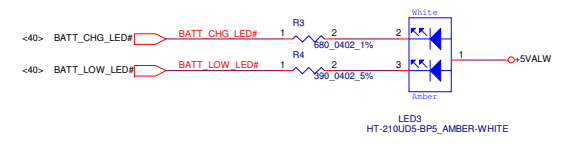
CC47靠近wlan connector



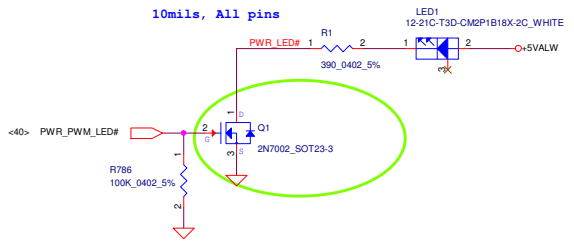
HDD LED



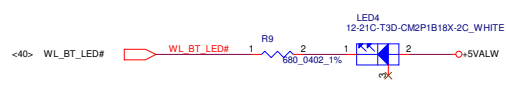
Battery LED



Power LED

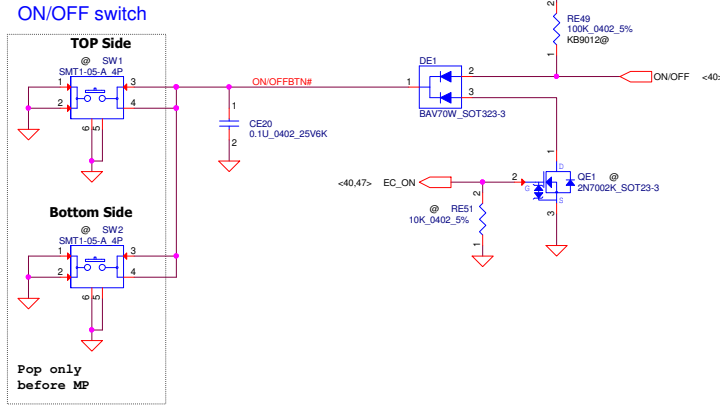


Wireless LED

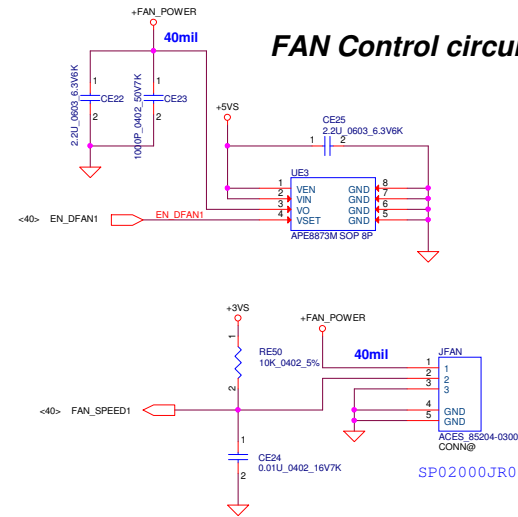


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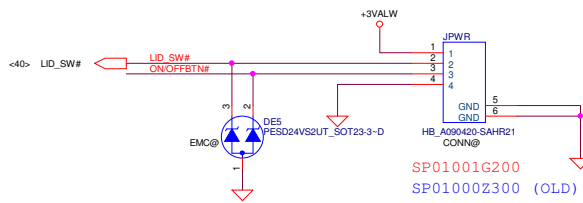
Power ON Circuit



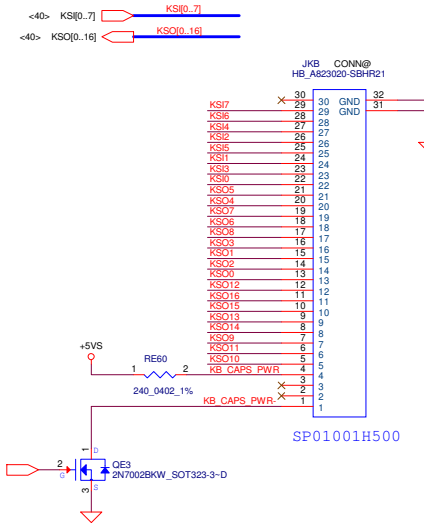
FAN Control circuit



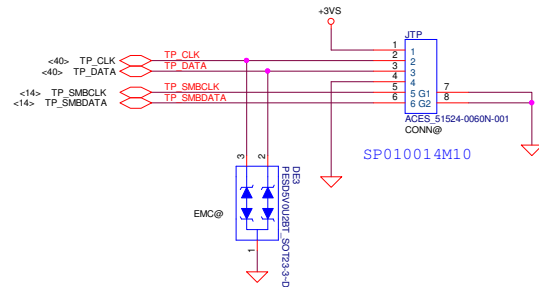
POWER/B



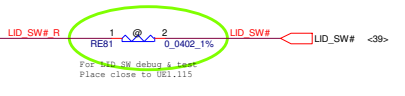
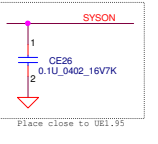
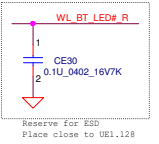
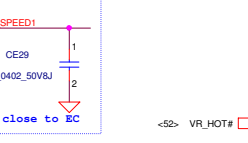
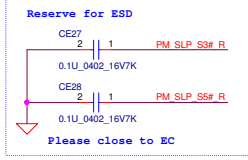
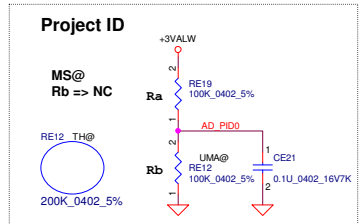
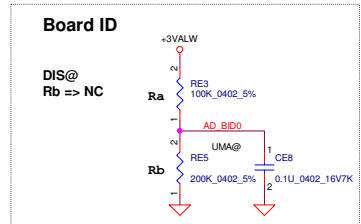
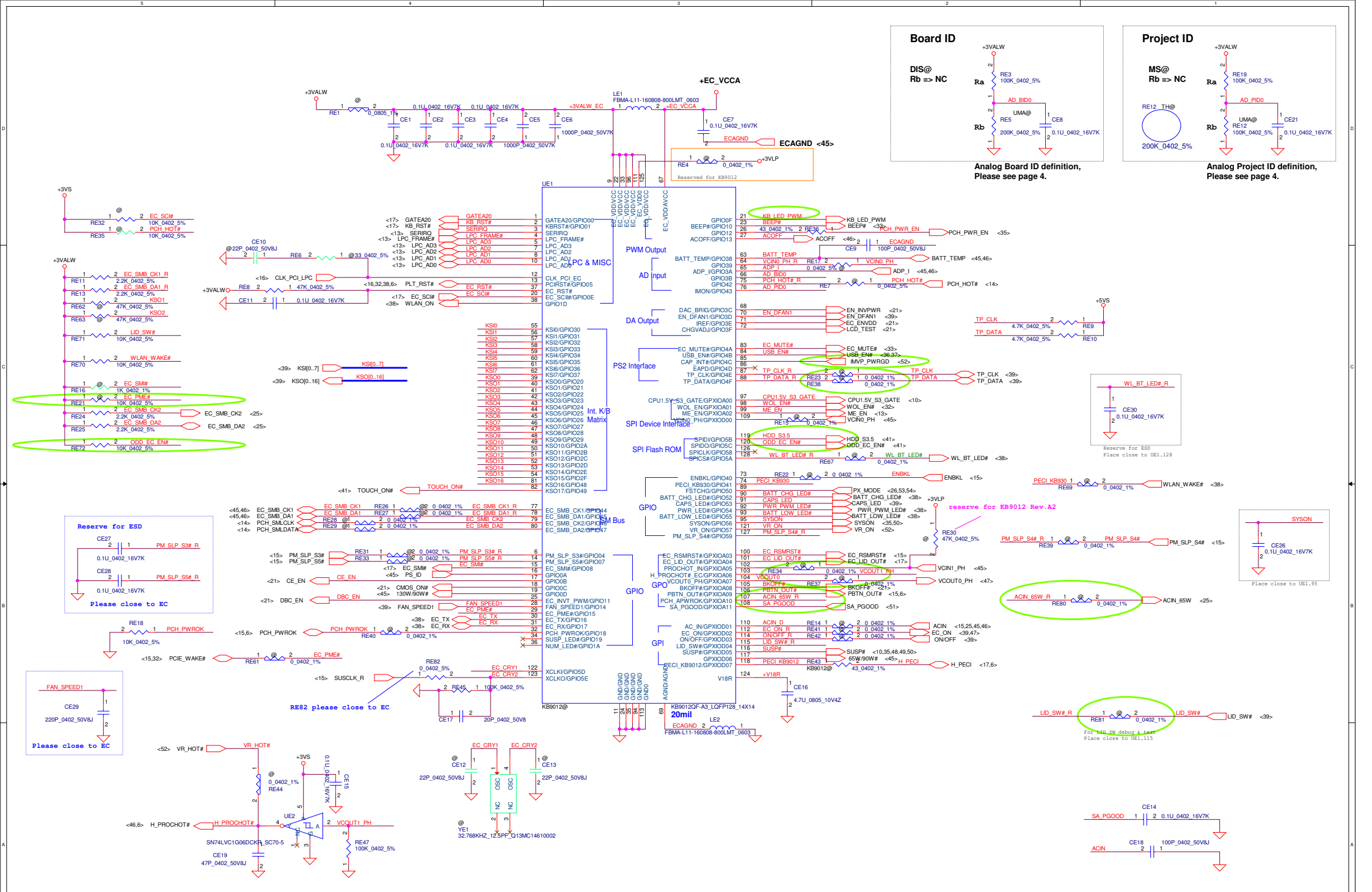
INT_KBD Conn.



Touch pad



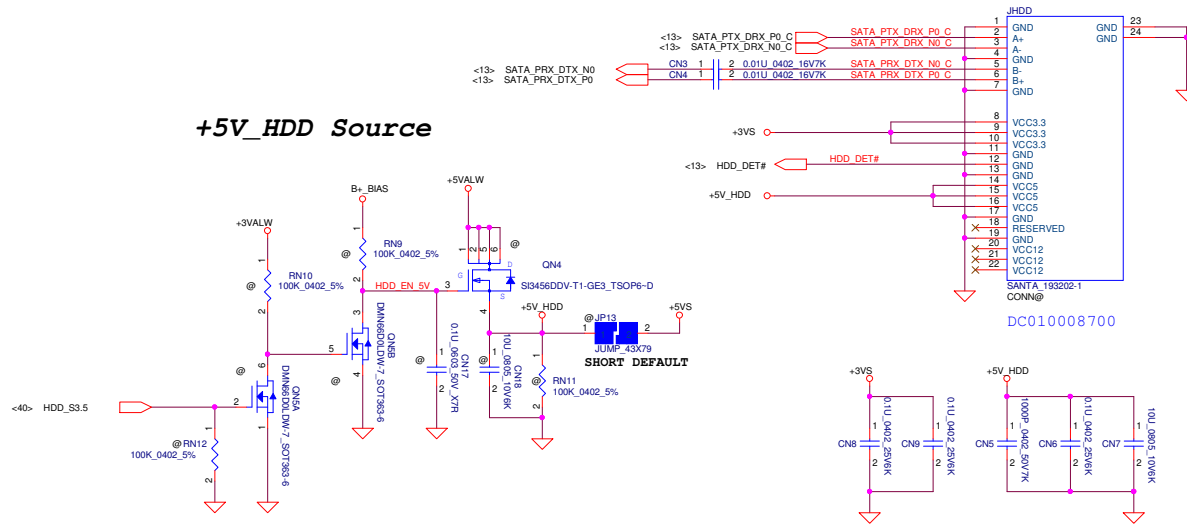
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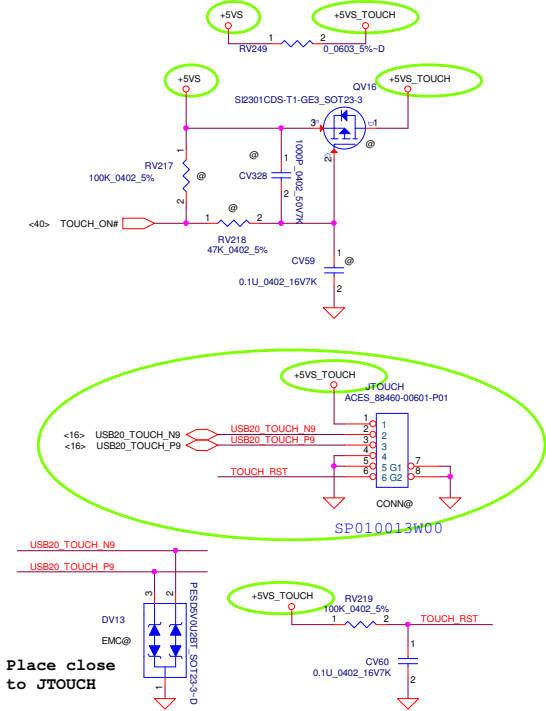
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Issued Date	2012/08/22	Deciphered Date	2013/08/31	EC ENE-KB9012	
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SATA HDD Conn.

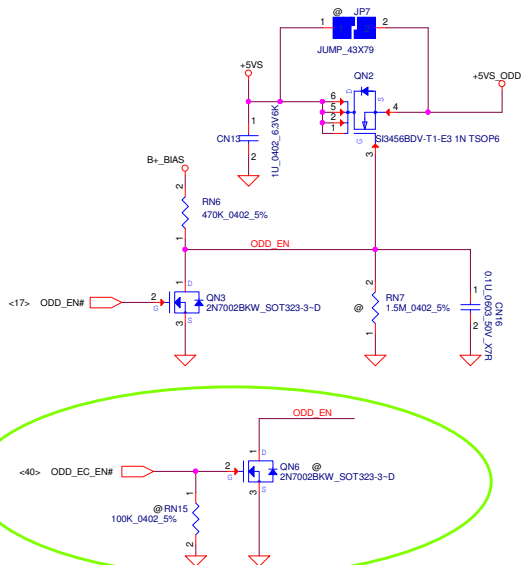
+5V_HDD Source



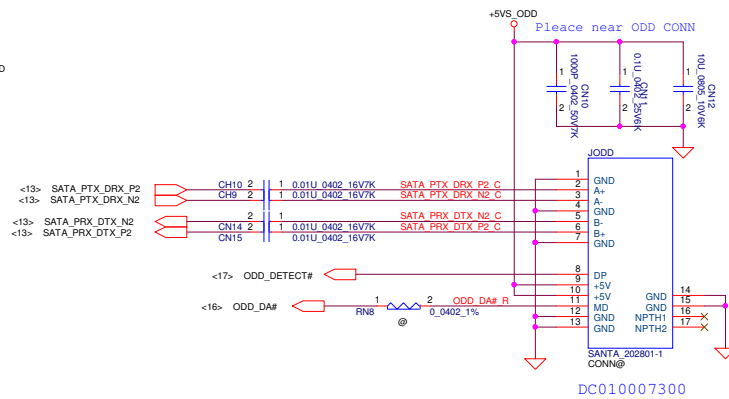
*** Touch Screen Panel**



ODD Power Control

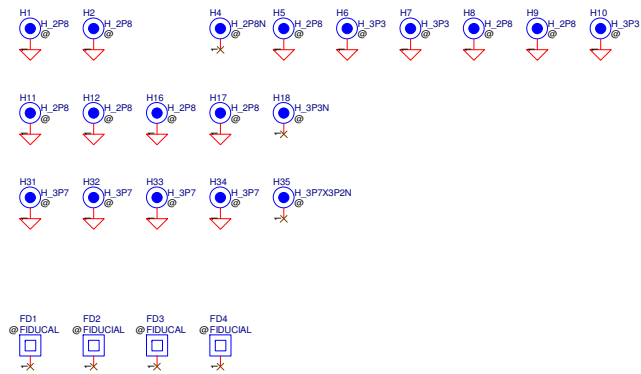


SATA ODD Conn.



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Screw Hole



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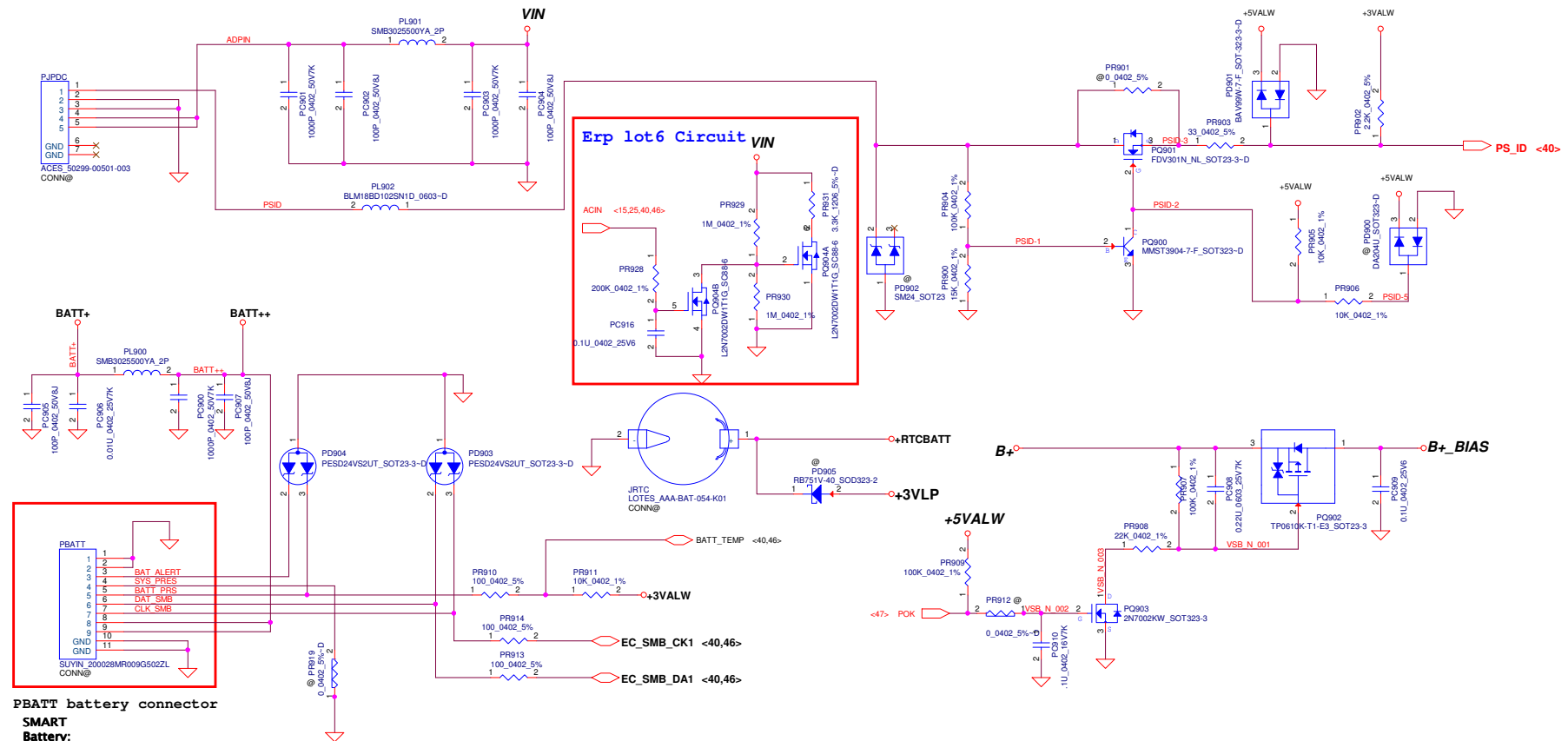
Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	21,39	LVDS	2012/05/17	SED	Add FHD Panel CE_ENABLE, DBC_ENABLE function from SED request	Add CE_EN, DBC_EN control pin to EC	0.2
2	21	LVDS	2012/05/22	SED	Follow SED team request disable CE_EN function	Change RV62 to DE-POP and RV100 to POP for disable CE_EN function	0.2
3	33	Audio codec	2012/05/23	CODEC	Follow CODEC vendor suggestion	Add AUDIO JACK PLUG delay circuit, Separate NET JACK_PLUG to -> JACK_SENSE# & -> JACK_PLUG#	0.2
4	16,21	Touch Screen	2012/05/29	HW	Add touch screen function	Add RV217, RV218, RV219, RV249, CV59, CV60, CV328, DV13, QV16, JTOUCH	0.2
5	39	Board ID	2012/05/30	HW	Board ID change for PT	Change RES from 8.2k_0402(SD028820180) to 33k_0402(SD028330280)	0.2
6	21,39	Touch Screen	2012/05/30	HW	Add touch screen function power control	Add NET "TOUCH_ON#" from JTOUCH to UE1.82(KB9012) for TOUCH SCREEN PANEL power control	0.2
7	33	Audio codec	2012/05/30	HW	Follow RealTek suggestion remove, delete reserve MUTE circuit	Delete D1,QA1,QA2,QA3,RA24,RA26,RA60,RA62,RA68,RA109,CA72,CA73	0.2
8	15,16, 39,41	ESD	2012/05/30	ESD	ESD ask CAP for reserve	Reserve 0.1u/0402 CH104,C223,CH105,CE27,CE29	0.2
9	14	Green CLK	2012/05/30	HW	For Green CLK test	Change RH31,RH41,RV232 0ohm form "GCLK#" to "g" for break the clock signal to device	0.2
10	10,26,41	DC/DC	2012/05/31	HW	Change "+1.5V_CPU_VDDQ", "+1.5VS", "+1.5VGS" derating	Change RC150 330K/0402 to 2M/0402, RC151 100K/0402 to 470K/0402, R218 100K/0402 to 470K/0402, RV115 0/0402 to 2M/0403	0.2
11	41	DC/DC	2012/05/31	HW	For power sequence trunning	Change R215 to DE-POP	0.2
12	06,15,16, 39,41	ESD	2012/05/31	ESD	Follow ESD team request	Change 0.1u/0402 from "g" to POP	0.2
13	32	Green CLK	2012/06/15	HW	Change for Green CLK bom control	Change RL21,RL30 from "g" to "GCLK#"	0.2
14	41	DC/DC	2012/06/15	HW	For WLAN card power sequence issue	Change R24,R213 from 470K/0402 56K/0403	0.2
15	35,41	Schematic page modify	2012/06/18	HW	Schematic page modify for easily maintain.	Swap Page. 35 & Page 41.	0.2
16	41	ODD	2012/06/18	HW	Change component location for easily maintain.	Move CH9,CH10 from Page.13 to Page.41	0.2
17	39	FAN	2012/06/29	HW	Fan speed noise issue	Reserve 220p/0402 CE24	0.2
18	6	CPU	2012/06/29	ESD	System boot-up shot down issue.	Change CC151 from POP to "g"	0.2
19	21,35, 39,40,41	Circuit adjust	2012/07/01	HW	Circuit & page adjust for OAK 15" & OAK 17"	1. Swap P.35 & P.41 and move touch screen circuit from P.21 to P.41. 2. Swap P.39 & P.40 page no	0.2
20	40	LID SW	2012/07/01	HW	LID SW need a trace for debug and switch.	Add RE81 for LID SW.	0.2
21	25	GPU	2012/07/01	HW	Follow AMD request, MarsPro will used MPLs.	Change RV75,RV76,RV81 from "DIS#" to "TH#"	0.2
22	29	GPU	2012/07/01	HW	Follow AMD request, MEM_CALRP2 is not need for Mars ASIC now.	Change RV205 from "MS#" to "g"	0.2
23	38	MINI card	2012/07/03	HW	Power Control for Mini card didn't need	Change R17 to "g"	0.2
24	6	XDP	2012/07/06	HW	S3 return hang issue	Change RC89 from "g" to POP	0.2
25	23	GREEN CLK	2012/07/09	HW	Follow Green CLK FAE suggestion	1. Change UG1.2(+3VLP) & UG1.8(+3VALW) connect to +LAN_IO 2. Add R787 connect from +RTC Batt to C5.2 & UG1.10 3. Change C14 from 0.1u to 5p/0402 4. Change C8 connect from +3V_ALW to +LAN_IO 5. Add R788 0ohm/0402 from +RTC VCC to UG1 for GCLK & DH1 select	0.2
26	35	MOAT	2012/07/09	ESD	For ESD request reserve CAP.	Reserve those CAP for ESD MOAT.	0.2
27	18	LVDS	2012/07/10	HW	Change RES and reserve CAP for LVDS issue	Change RH185 from 0ohm-short to 0ohm/0805, and reserve CH106 1U/0402	0.2
28	13	PCH	2012/07/11	ESD	Follow ESD team request	Add RH44,RH49,RH70 & NET PCH_JTAG_TMS_R, PCH_JTAG_TDI_R, PCH_JTAG_TDO_R for break signal trace	0.2
29	40	PCH	2012/07/11	ESD	Follow ESD team request	1.Change NET NAME "N59110727" to "WL_BT_LED#_R" 2. Reserve 0.1u/0402 on "WL_BT_LED#_R" for ESD	0.2
30	21	LVDS	2012/07/11	HW	Reserve for CE function for LVDS connector	Change CE_EN_R from dummy to JLVDS.18	0.2
31	32	Connector	2012/07/12	ME	For ME request	Change JLAN CPN from "DC234004V00" to "SP011207090"	0.2
32	40	FAN	2012/07/16	HW	For FAN_SPEED1 noise issue	Change CE29 from "g" to POP	0.2
33	14	Touch PAD	2012/07/17	SED	Change Touch PAD SMBUS port for SMBUS issue	Change Touch PAD SMBUS port for SMB0 to SMB	1.0
34	32	GREEN CLK	2012/07/19	HW	Follow Silego FAE request	Change RL21 from 510 ohm to 0 ohm/0402	1.0
35	41	Touch Screen	2012/08/07	SED	Follow SED team request change JTOUCH USB signal conatct.	Change JTOUCH Pin define.	1.0
36	34	Card Reader	2012/08/14	ESD	Follow ESD team request	Reserve CR11 100p/0402 close to JREAD	1.0
37	23	GREEN CLK	2012/08/16	HW	Fixed GCLK output abnormal issue	Change UG1.2(UG1/VDD) from +LAN_IO to+3VALW	1.0
38	33	CODEC	2012/08/16	HW	The issue already fixed by new CODEC.	Remove delay circuit and POP RA4	1.0
39	23	GREEN CLK	2012/08/17	HW	For RTC discharge issue	De-pop R788	1.0
40	32,34	LAN	2012/08/17	HW	For LAN Chip abnormal leakage issue	Pop RL34 and de-pop RE21	1.0
41	34	Card Reader	2012/08/20	ESD	Follow ESD team request	Change CR11 from 100p/0402 to 10p/0402 and POP	1.0

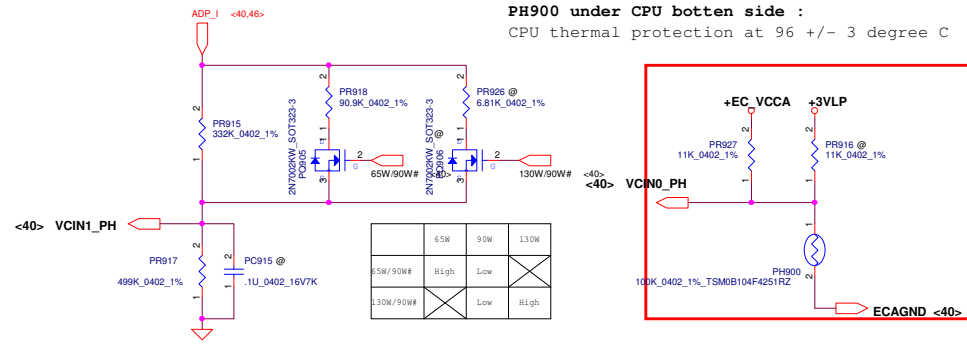
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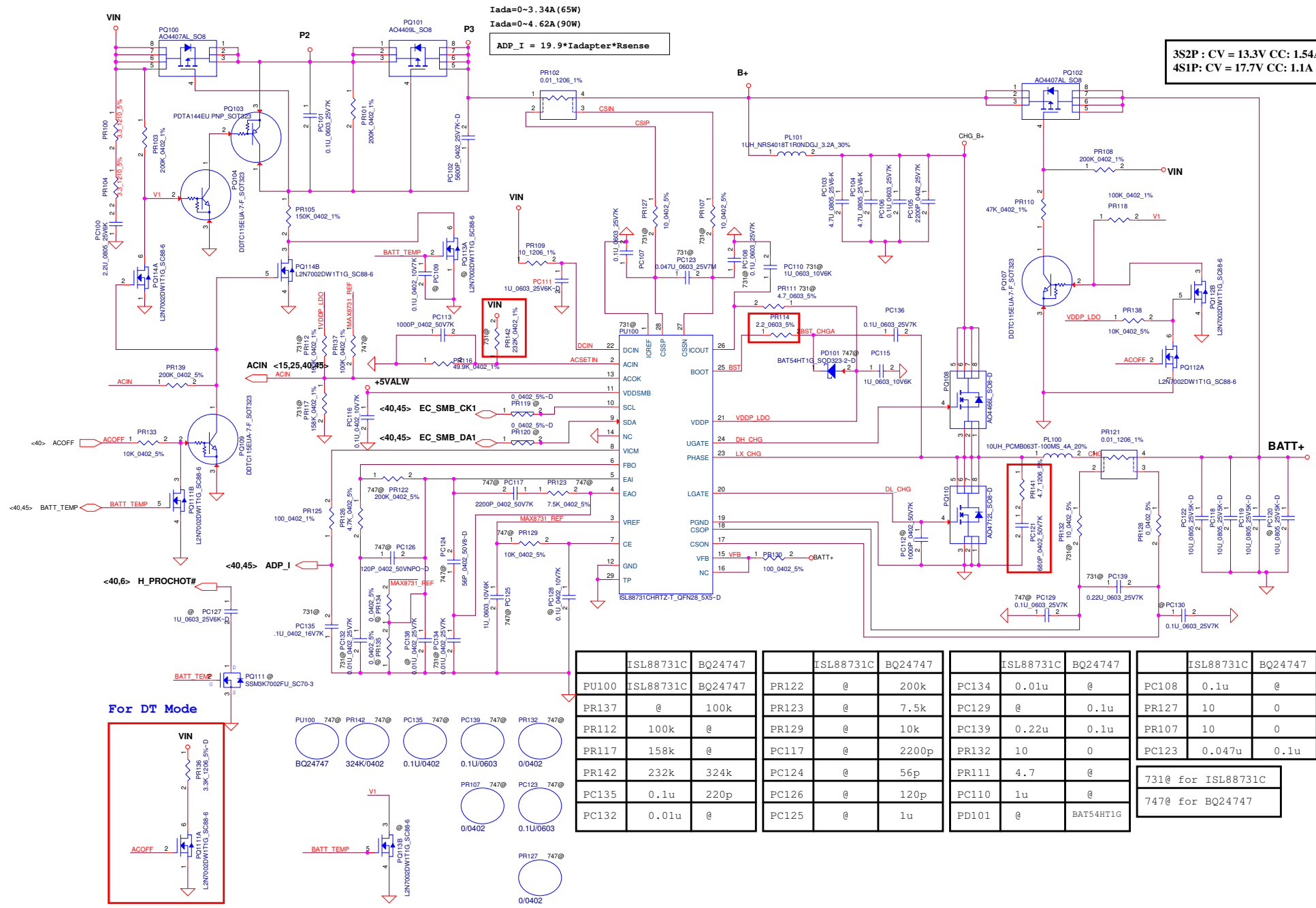
Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
42	41	Touch Screen	2012/08/20	SED	Follow SED team request	Change Touch screen power rail for +3VS to +5VS	1.0
43	38	LED	2012/08/20	HW	Change LED light	Change LED1,LED2,LED4 CPN from SC500006000 to SC50000DC00	1.0
44	38	WLAN	2012/08/20	HW	Remove AGAC function power control	Change R18,R19,R20,R21,C13,Q2,Q4 component BOM structure to "g"	1.0
45	41	Touch Screen	2012/08/20	HW	Add EC control for Touch Screen function	Add RN15 & QN6 and relative circuit connect	1.0
46	40	BATMAN2	2012/08/21	HW	For BATMAN2	Add RE82 0ohm/0402 between trace SUSCLK_R & EC_CRY2	1.0
47	14,17	PCH	2012/08/21	HW	For SYSTEM S3 leakage issue	Change RH79.2 & RH245.2 connect from +3V_PCH to +3VS	1.0

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PH900 under CPU bottom side :
CPU thermal protection at 96 +/- 3 degree C



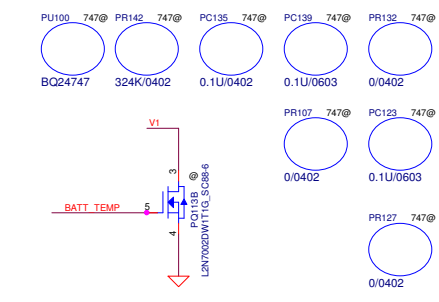
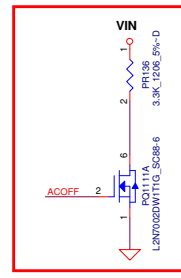


Iada=0~3.34A (65W)
Iada=0~4.62A (90W)

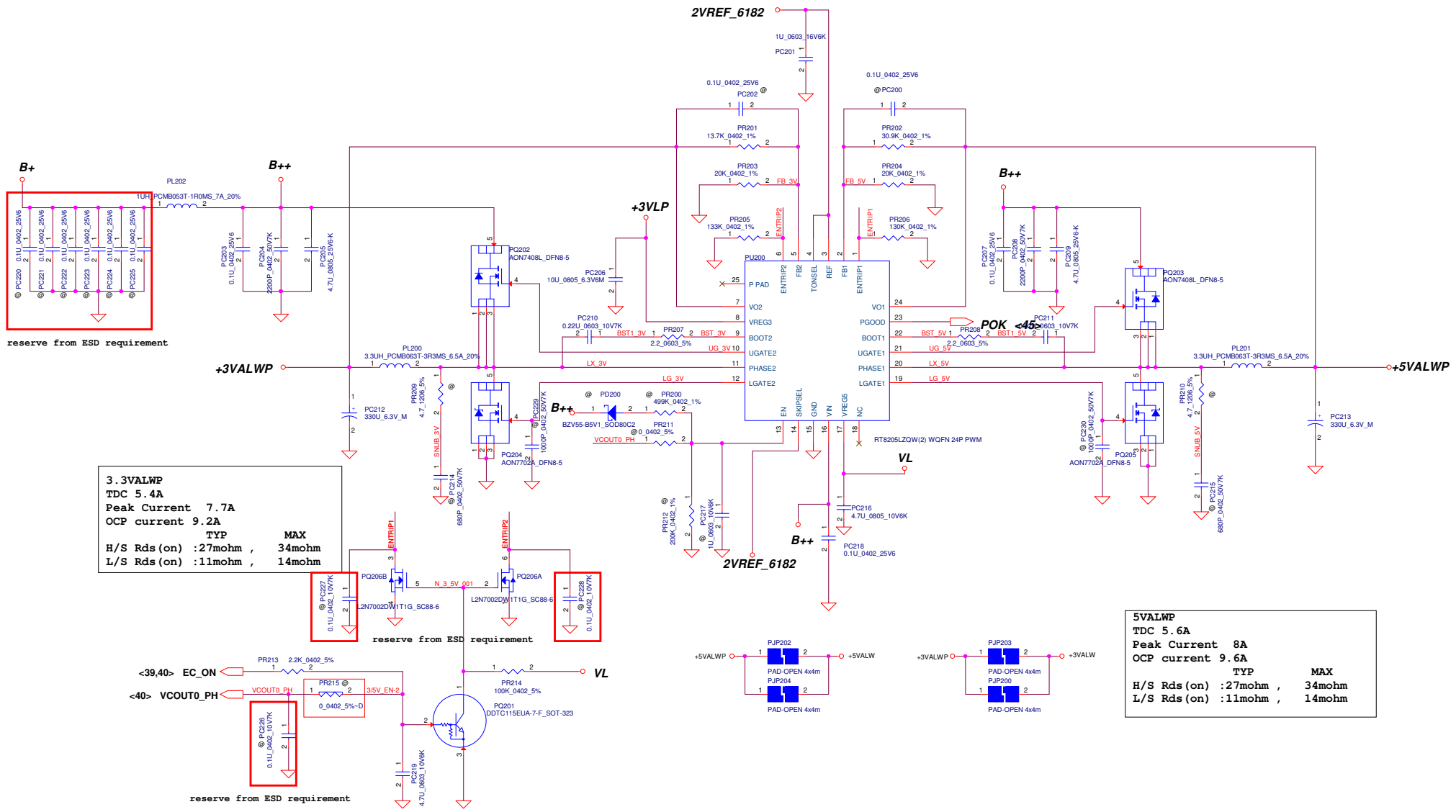
$ADP_I = 19.9 \cdot I_{adapter} \cdot R_{sense}$

3S2P : CV = 13.3V CC = 1.54A
4S1P : CV = 17.7V CC = 1.1A

For DT Mode



	ISL88731C	BQ24747		ISL88731C	BQ24747		ISL88731C	BQ24747		ISL88731C	BQ24747
PU100	ISL88731C	BQ24747	PR122	@	200k	PC134	0.01u	@	PC108	0.1u	@
PR137	@	100k	PR123	@	7.5k	PC129	@	0.1u	PR127	10	0
PR112	100k	@	PR129	@	10k	PC139	0.22u	0.1u	PR107	10	0
PR117	158k	@	PC117	@	2200p	PR132	10	0	PC123	0.047u	0.1u
PR142	232k	324k	PC124	@	56p	PR111	4.7	@	731@ for ISL88731C		
PC135	0.1u	220p	PC126	@	120p	PC110	1u	@	747@ for BQ24747		
PC132	0.01u	@	PC125	@	1u	PD101	@	BAT54HT1G			



B+

reserve from ESD requirement

+3VALWP

3.3VALWP
 TDC 5.4A
 Peak Current 7.7A
 OCP current 9.2A

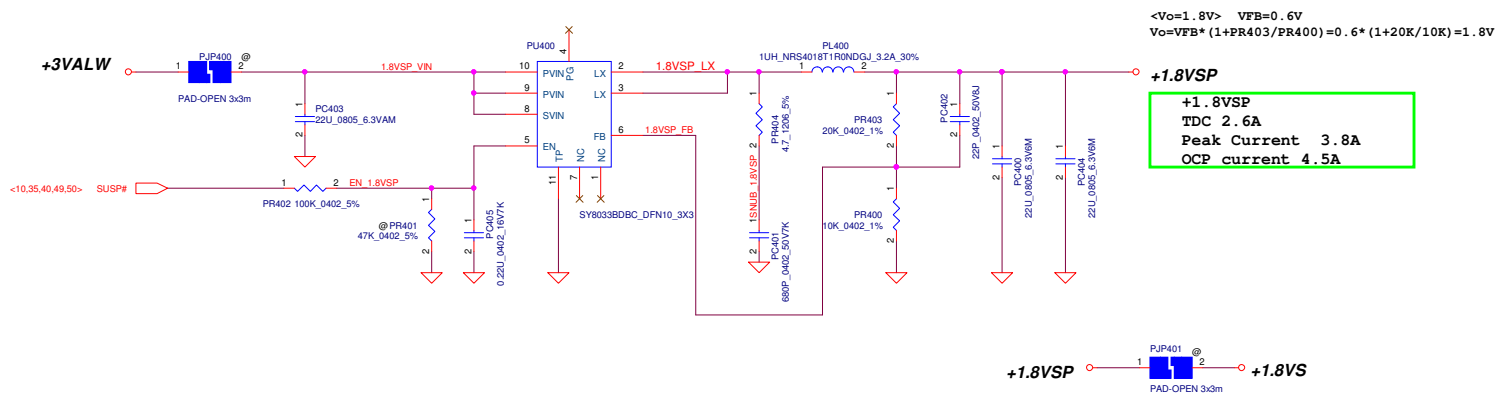
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H/S Rds (on)	: 27mohm	34mohm
L/S Rds (on)	: 11mohm	14mohm

reserve from ESD requirement

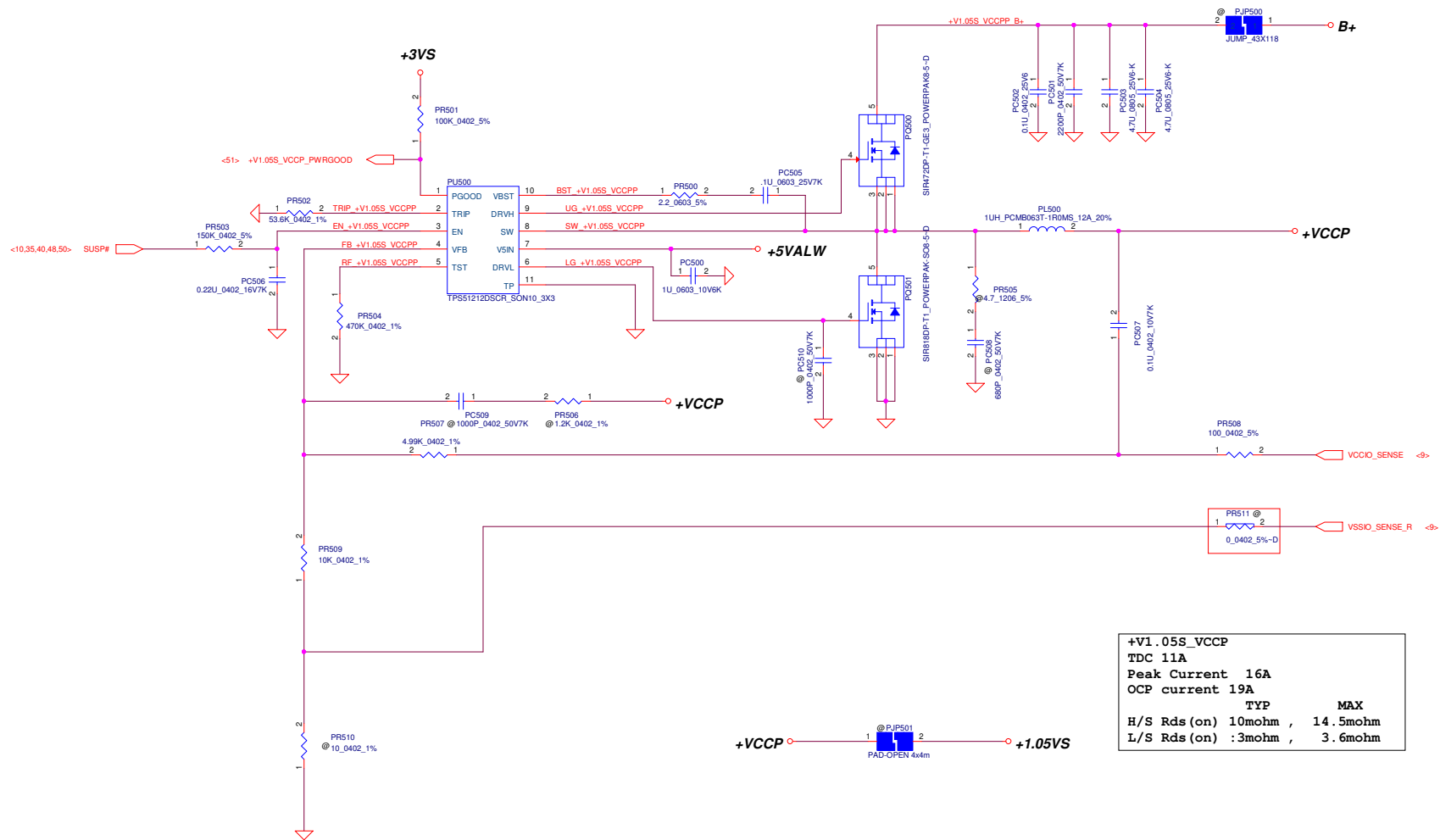
5VALWP
 TDC 5.6A
 Peak Current 8A
 OCP current 9.6A

	TYP	MAX
H/S Rds (on)	: 27mohm	34mohm
L/S Rds (on)	: 11mohm	14mohm

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+V1.05S_VCCPP
TDC 11A
Peak Current 16A
OCF current 19A

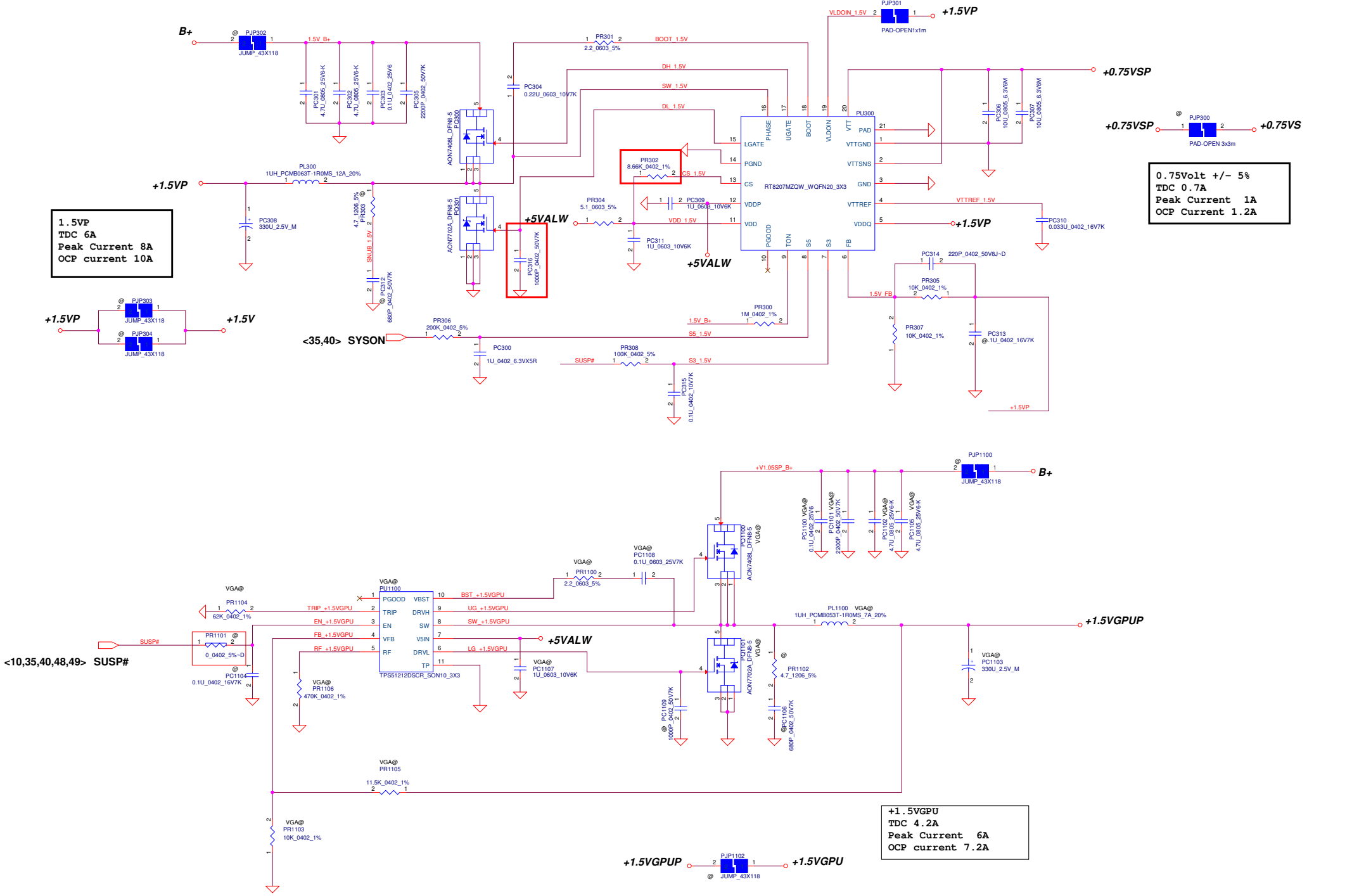
TYP	MAX
H/S Rds (on) 10mohm	14.5mohm
L/S Rds (on) :3mohm	3.6mohm

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1.5VP
TDC 6A
Peak Current 8A
OCP current 10A

0.75Volt +/- 5%
TDC 0.7A
Peak Current 1A
OCP Current 1.2A

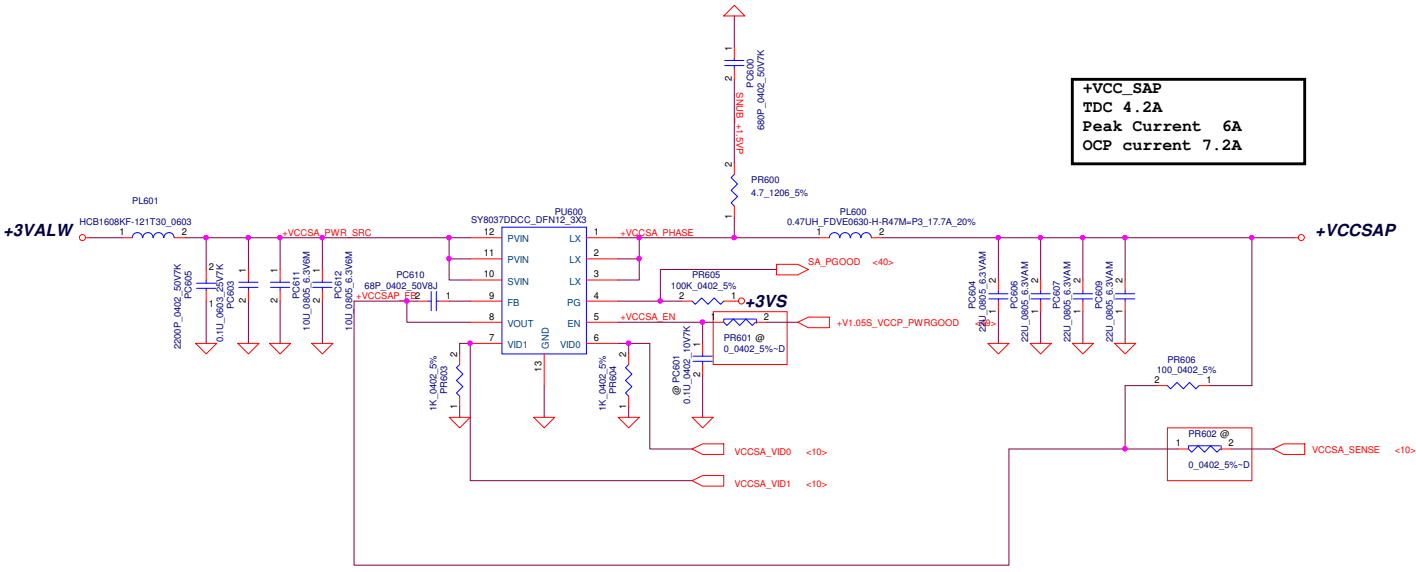
+1.5VGPU
TDC 4.2A
Peak Current 6A
OCP current 7.2A



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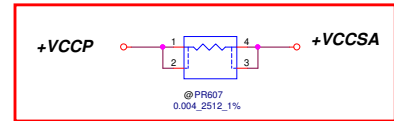
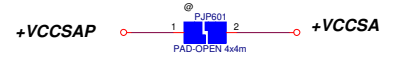
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

output voltage adjustable network

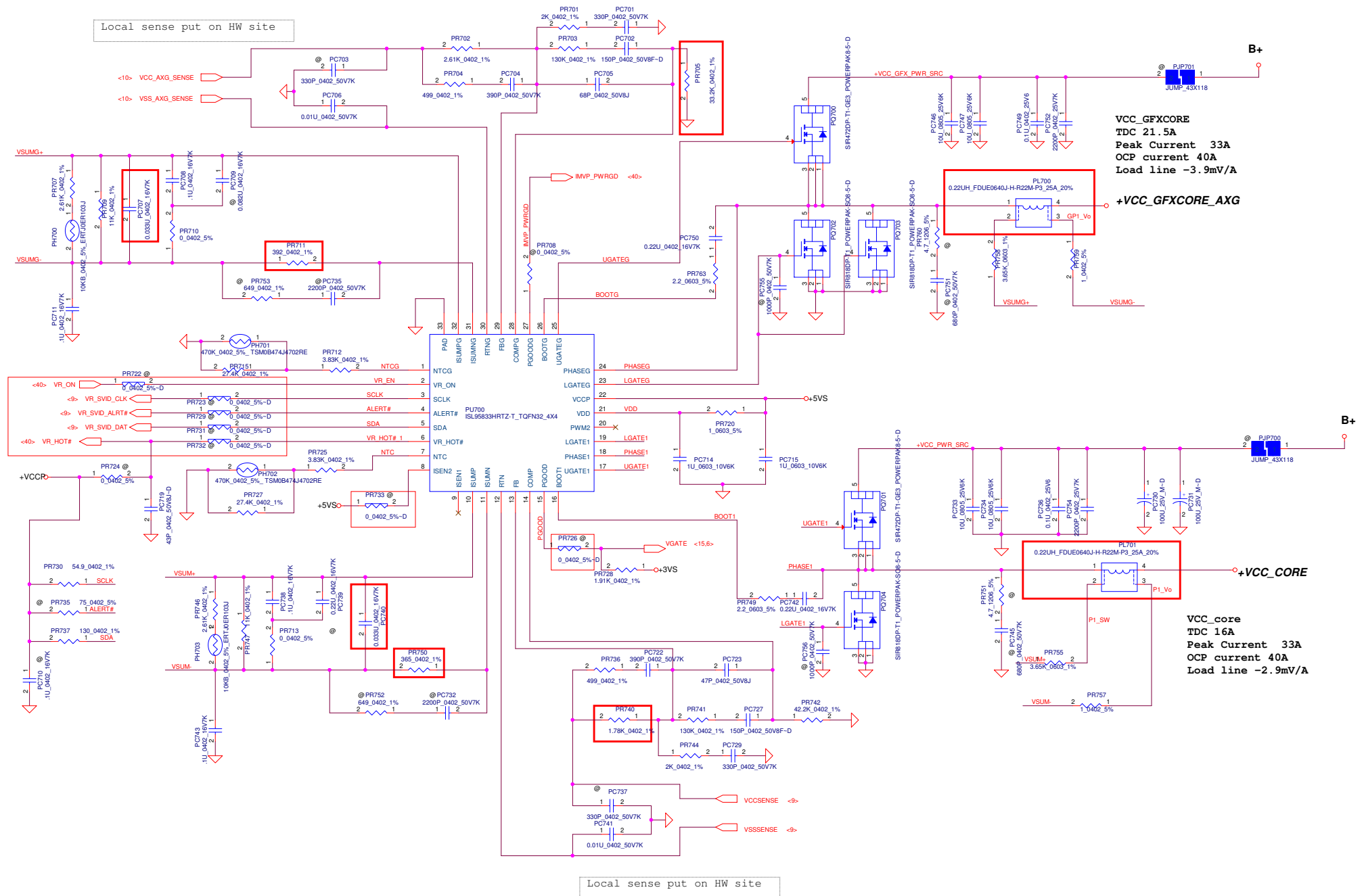


+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

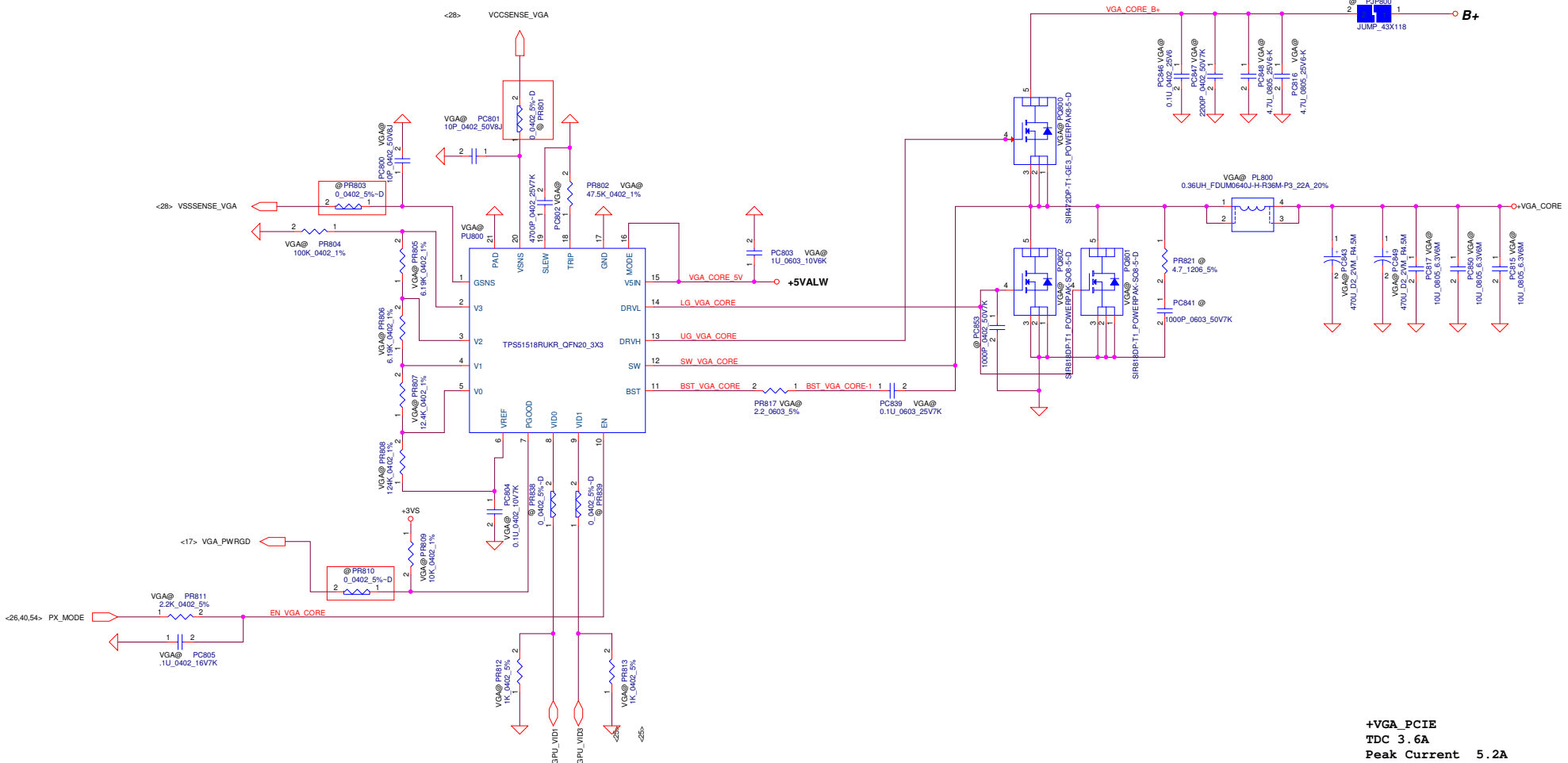


reserve for Pentium and Celeron only



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Issued Date		Deciphered Date		PWR_VCORE	
2012/08/22		2013/08/31		Document Number	
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				Date: Wednesday, August 28, 2012	
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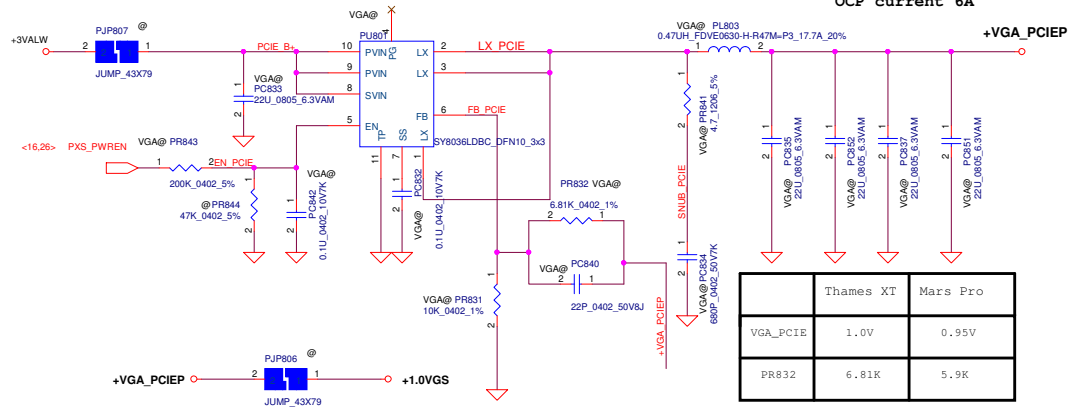


+VGA_PCIE
 TDC 3.6A
 Peak Current 5.2A
 OCP current 6A

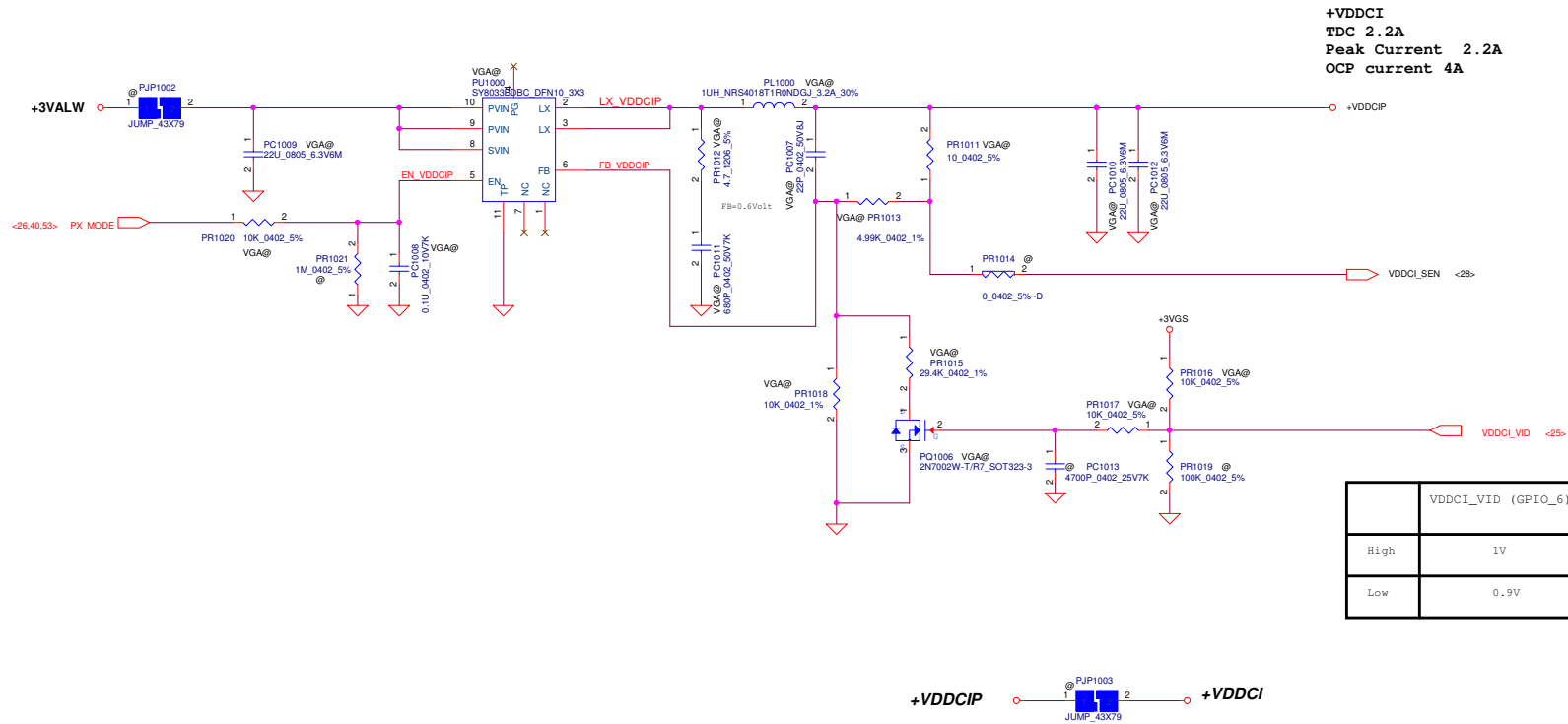
Thames XT

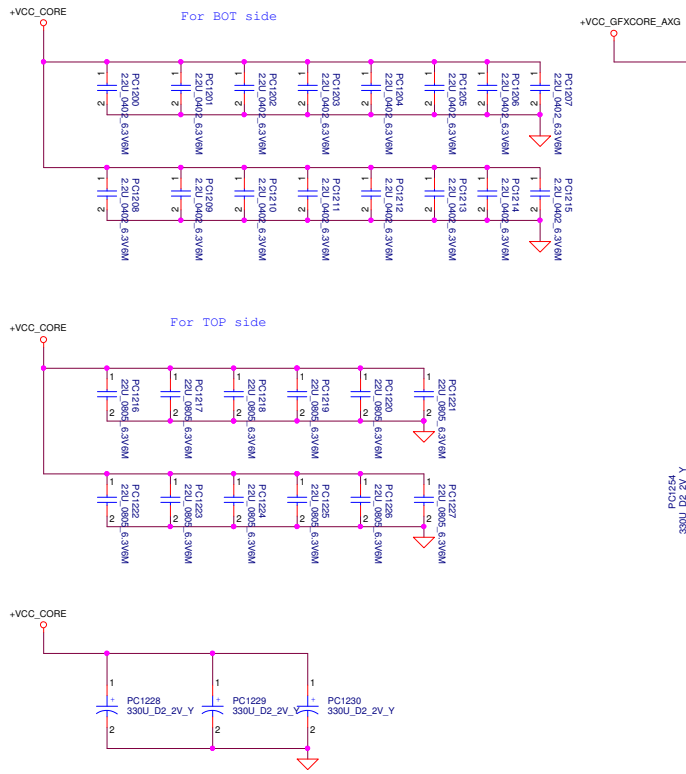
GPU_VID3 (GPIO15)	GPU_VID1 (GPIO20)	Core Voltage Level
1	1	0.8V
1	0	0.85V
0	1	0.9V
0	0	1.0V

+VGA_CORE
 TDC 20A
 Peak Current 30A
 OCP current 36A
 FSW=350kHz
 DCR 1.4mohm +/-5%



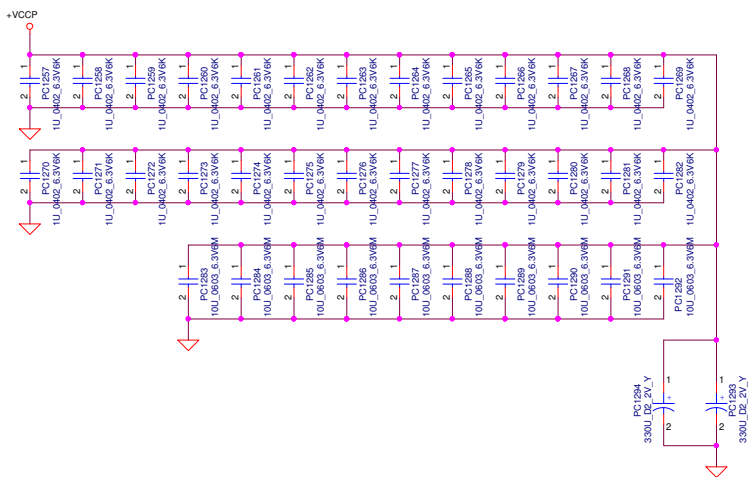
	Thames XT	Mars Pro
VGA_PCIE	1.0V	0.95V
PR832	6.81K	5.9K





Vaxg

- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
- VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed

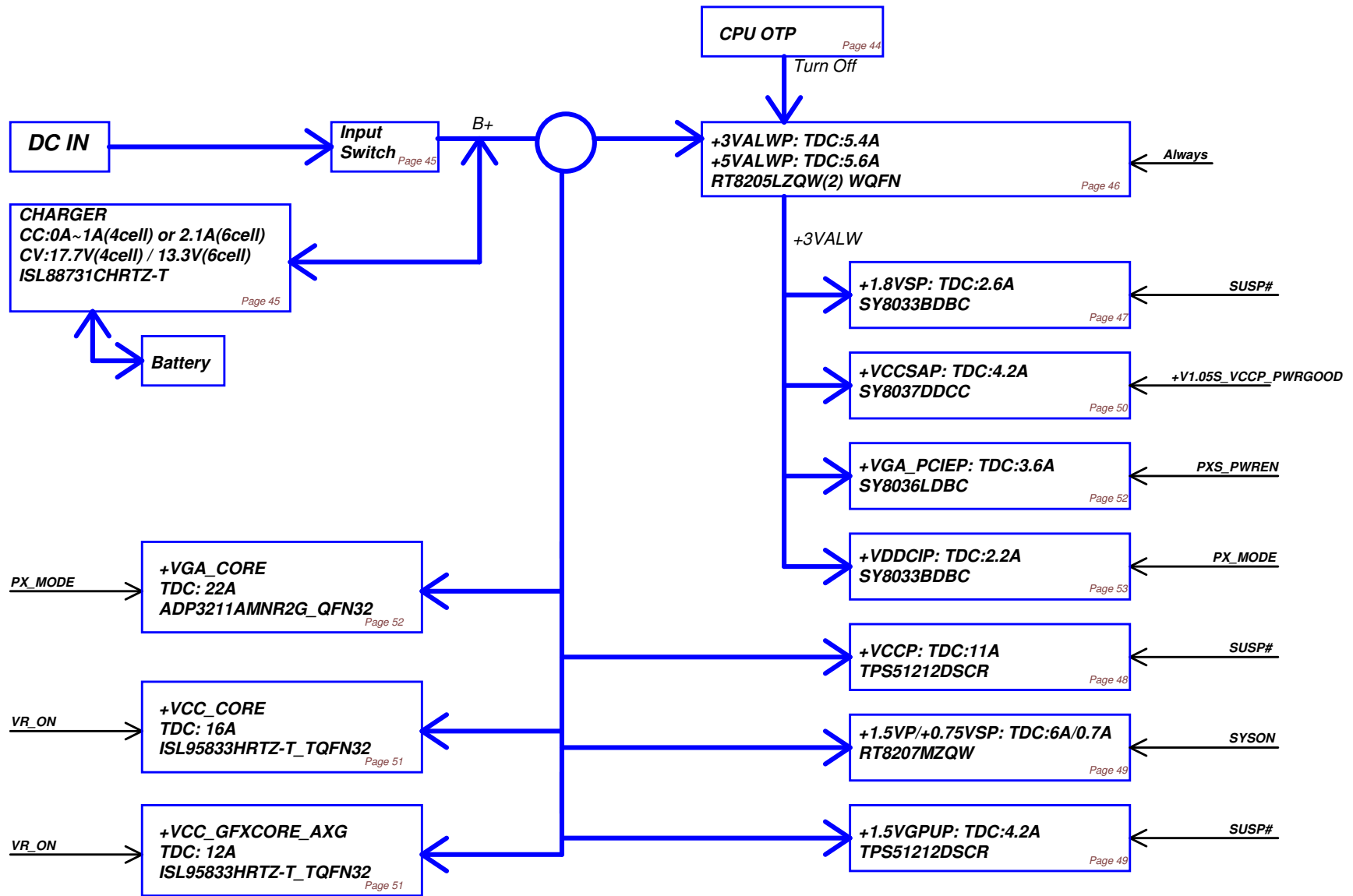


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PWR PROCESSOR DECOUPLING	
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Power block



Version Change List (P. I. R. List)

<i>Item</i>	<i>Page#</i>	<i>Title</i>	<i>Date</i>	<i>Request Owner</i>	<i>Issue Description</i>	<i>Solution Description</i>	<i>Rev.</i>
1	51	VCORE	12/05/11	Morris	adjust VR parameter	change PL700 and PL701 from 0.36u to 0.22u change PC707 and PC740 from 0.047u to 0.033u change PR750 from 649 to 365 change PR711 from 649 to 392 change PR740 from 1.91k to 1.78k change PR705 from 150k to 33.2k	X00
2	44 45 46	DCIN/BATT CONN/OTP CHARGER 3.3VALWP/5VALWP	12/05/11	Morris	follow SSI memo for part shortage issue	change PQ112,PQ114,PQ1111,PQ206,PQ904 from SB00000CQ00 to SB00000PV00	X00
3	49	+1.5VP/1.5VDGPU/0.75VSP	12/05/15	Morris	design change	change PR302 from 12k to 8.66k	X00
4	50	+VCCSAP	12/05/23	Morris	for Pentium and Celeron special BOM	add PR607 and reserve	X00
5	49	+1.5VP/1.5VDGPU/0.75VSP	12/07/06	Morris	design change to reduce low-side mosfet induce	add PC316 1000pf	X01
6	45	CHARGER	12/07/17	Morris	from EMI request	change PR114 from 0 to 2.2 add PR141 and PC121	X01
7	45	CHARGER	12/07/17	Morris	design change to solve Battery LED is still on after unplug AC when SUT in S3S4S5 issue	change PR142 from 210k to 232k for ISL88731C (X76) change PR142 from 309k to 324k for BQ24747 (X76)	X01
8	44	DCIN/BATT CONN/OTP	12/07/17	Morris	revise OTP setting to 96C from thermal request	change PR927 from 12.1k to 11k	X01

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