## Voltage Detector with Separated Sense Pin & Delay Type Capacitor

## GENERAL DESCRIPTION

The XC6108 series is highly precise, low power consumption voltage detector, manufactured using CMOS and laser trimming technologies.

Since the sense pin is separated from power supply, it allows the IC to monitor added power supply.

Using the IC with the sense pin separated from power supply enables output to maintain the state of detection even when voltage of the monitored power supply drops to 0V.

Moreover, with the built-in delay circuit, connecting the delay capacitance pin to the capacitor enables the IC to provide an arbitrary release delay time.

Both CMOS and N-channel open drain output configurations are available.

## APPLICATIONS

Microprocessor reset circuitry

Charge voltage monitors

Memory battery back-up switch circuits

Power failure detection circuits

## FEATURES

**Highly Accurate** : $\pm$2% (Setting Detect Voltage  1.5V)

: $\pm$30mV (Setting Detect Voltage  1.5V)

**Ultra Low Power Consumption**

: 0.8 $\mu$A (TYP.) ($V_{IN}$= 2.0V)

**Detect Voltage Range** : 0.8V ~ 5.0V in 100mV increments

**Operating Voltage Range** : 1.0V ~ 6.0V

**Detect Voltage Temperature Characteristics**

: $\pm$100ppm/  (TYP.)

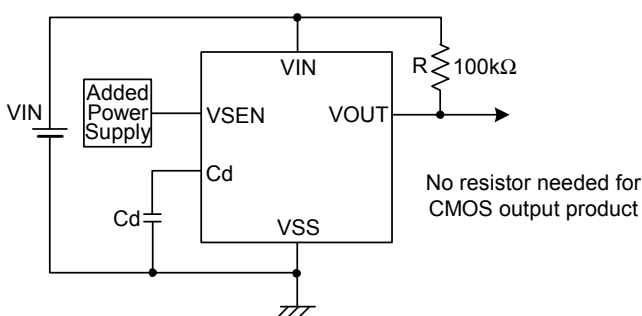**Output Configuration** : CMOS or N-channel open drain

**Operating Temperature Range**

: -40  ~ +85

**Separated Sense Pin**

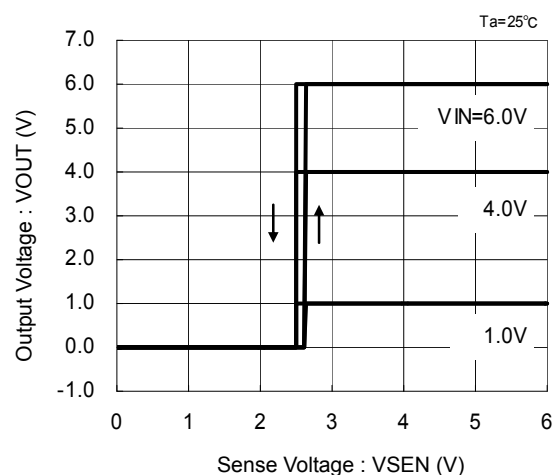**Built-In Delay Circuit, Delay Capacitance Pin Available**

**Ultra Small Package** : USP-4
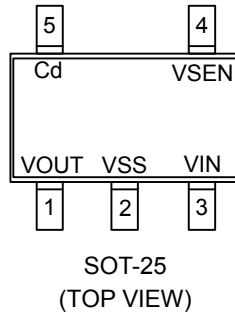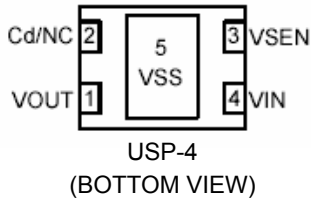
SOT-25

## TYPICAL APPLICATION CIRCUIT



No resistor needed for CMOS output product

## TYPICAL PERFORMANCE CHARACTERISTICS

Output Voltage vs. Sense Voltage

XC6108C25AGR

## PIN CONFIGURATION



USP-4
(BOTTOM VIEW)

SOT-25
(TOP VIEW)

* In the XC6108xxxA/B series, the dissipation pad should not be short-circuited with other pins.
* In the XC6108xxxC/D series, when the dissipation pad is short-circuited with other pins, connect it to the NC pin (pin No.2) before use.

## PIN ASSIGNMENT

| PIN NUMBER | | PIN NAME | FUNCTION |
|---|---|---|---|
| USP- 4 | SOT-25 | | |
| 1 | 1 | V$_{OUT}$ | Output (Detect "L") |
| 2 | 5 | Cd | Delay Capacitance (*1) |
| 2 | - | NC | No Connection |
| 3 | 4 | V$_{SEN}$ | Sense |
| 4 | 3 | V$_{IN}$ | Input |
| 5 | 2 | V$_{SS}$ | Ground (*2) |

NOTE:

*1: With the V$_{SS}$ pin of the USP-4 package, a tab on the backside is used as the pin No.5.

*2: In the case of selecting no built-in delay capacitance pin type, the delay capacitance (Cd) pin will be used as the N.C.

## PRODUCT CLASSIFICATION

Ordering Information

XC6108 _____

| DESIGNATOR | DESCRIPTION | SYMBOL | DESCRIPTION |
|---|---|---|---|
| | Output Configuration | C | : CMOS output |
| | | N | : N-ch open drain output |
| | Detect Voltage | 08 ~ 50 | : e.g. 18   1.8V |
| | Output Delay & Hysteresis (Options) | A | : Built-in delay capacitance pin, hysteresis 5% (TYP.)(Standard*) |
| | | B | : Built-in delay capacitance pin, hysteresis less than 1%(Standard*) |
| | | C | : No built-in delay capacitance pin, hysteresis 5% (TYP.) (Semi-custom) |
| | | D | : No built-in delay capacitance pin, hysteresis less than 1% (Semi-custom) |
| | Package | G | : USP-4 |
| | | M | : SOT-25 |
| | Device Orientation | R | : Embossed tape, standard feed |
| | | L | : Embossed tape, reverse feed |

*When delay function isn't used, open the delay capacitance pin before use.
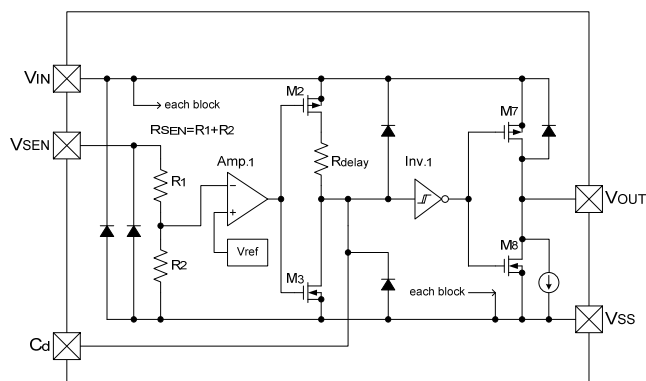
# BLOCK DIAGRAMS

## (1) XC6108CxxA
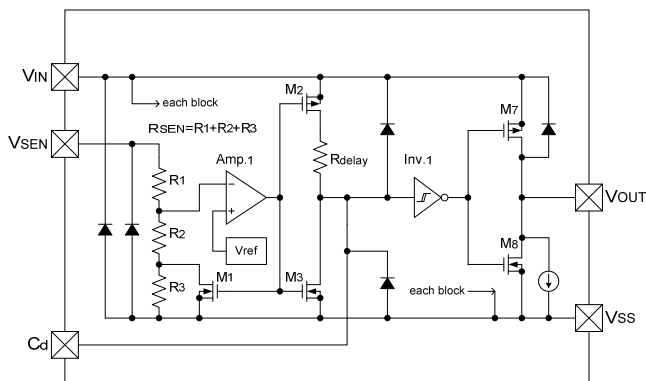


*The delay capacitance pin (Cd) is not connected to the circuit in the block diagram of XC6108CxxC (semi-custom).

## (2) XC6108CxxB



*The delay capacitance pin (Cd) is not connected to the circuit in the block diagram of XC6108CxxD (semi-custom).
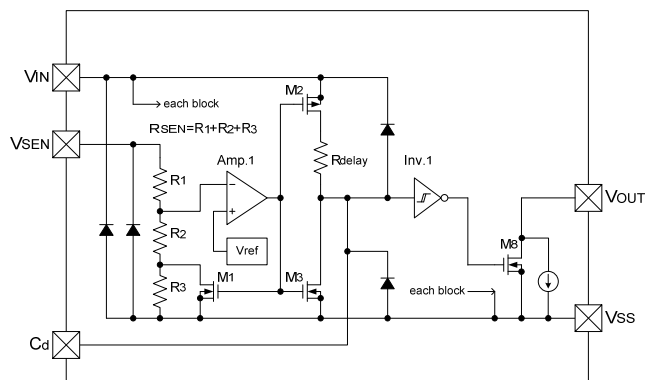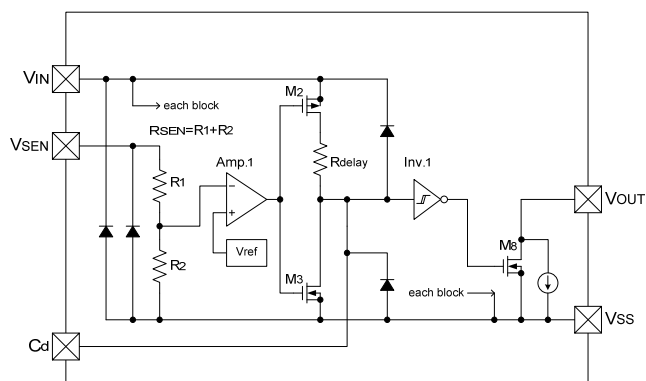
## (3) XC6108NxxA



*The delay capacitance pin (Cd) is not connected to the circuit in the block diagram of XC6108NxxC (semi-custom).

## (4) XC6108NxxB



*The delay capacitance pin (Cd) is not connected to the circuit in the block diagram of XC6108NxxD (semi-custom).

## ABSOLUTE MAXIMUM RATINGS

XC6108xxxA/B

Ta = 25$^O$C

| PARAMETER | | SYMBOL | RATINGS | UNITS |
|---|---|---|---|---|
| Input Voltage | | $V_{IN}$ | $V_{SS}$ 0.3 ~ 7.0 | V |
| Output Current | | $I_{OUT}$ | 10 | mA |
| Output Voltage | XC6108C (*1) | $V_{OUT}$ | $V_{SS}$ 0.3 ~ $V_{IN}$ 0.3 | V |
| | XC6108N (*2) | | $V_{SS}$ 0.3 ~ 7.0 | |
| Sense Pin Voltage | | $V_{SEN}$ | $V_{SS}$ 0.3 ~ 7.0 | V |
| Delay Capacitance Pin Voltage | | $V_{CD}$ | $V_{SS}$ 0.3 ~ $V_{IN}$ 0.3 | V |
| Delay Capacitance Pin Current | | $I_{CD}$ | 5.0 | mA |
| Power Dissipation | USP-4 | Pd | 120 | mW |
| | SOT-25 | | 250 | |
| Operating Temperature Range | | Ta | 40 ~ 85 | |
| Storage Temperature Range | | Tstg | 55 ~ 125 | |

XC6108xxxC/D

Ta = 25$^O$C

| PARAMETER | | SYMBOL | RATINGS | UNITS |
|---|---|---|---|---|
| Input Voltage | | $V_{IN}$ | $V_{SS}$ 0.3 ~ 7.0 | V |
| Output Current | | $I_{OUT}$ | 10 | mA |
| Output Voltage | XC6108C (*1) | $V_{OUT}$ | $V_{SS}$ 0.3 ~ $V_{IN}$ 0.3 | V |
| | XC6108N (*2) | | $V_{SS}$ 0.3 ~ 7.0 | |
| Sense Pin Voltage | | $V_{SEN}$ | $V_{SS}$ 0.3 ~ 7.0 | V |
| Power Dissipation | USP-4 | Pd | 120 | mW |
| | SOT-25 | | 250 | |
| Operating Temperature Range | | Ta | 40 ~ 85 | |
| Storage Temperature Range | | Tstg | 55 ~ 125 | |

NOTE:

*1: CMOS output

*2: N-ch open drain output

## ELECTRICAL CHARACTERISTICS

XC6108xxxA

Ta=25

| PARAMETER | SYMBOL | CONDITIONS | | MIN. | TYP. | MAX. | UNITS | CIRCUITS |
|---|---|---|---|---|---|---|---|---|
| Operating Voltage | $V_{IN}$ | $V_{DF(T)}$ = 0.8 ~ 5.0V (*1) | | 1.0 | - | 6.0 | V | - |
| Detect Voltage | $V_{DF}$ | $V_{IN}$ = 1.0 ~ 6.0V | | | E-1 | | V | 1 |
| Hysteresis Range1 | $V_{HYS1}$ | $V_{IN}$ = 1.0 ~ 6.0V | | | E-2 | | V | 1 |
| Detect Voltage Line Regulation | $\dfrac{\Delta V_{DF}}{\Delta V_{IN} \cdot V_{DF}}$ | $V_{IN}$ = 1.0 ~ 6.0V | | - | ±0.1 | - | %/V | 1 |
| Supply Current 1 (*2) | $I_{SS1}$ | $V_{SEN}$ = $V_{DF}$ x 0.9 | $V_{IN}$ = 1.0V | - | 0.6 | 1.5 | μA | 2 |
| | | | $V_{IN}$ = 6.0V | - | 0.7 | 1.6 | | |
| Supply Current 2 (*2) | $I_{SS2}$ | $V_{SEN}$ = $V_{DF}$ x 1.1 | $V_{IN}$ = 1.0V | - | 0.8 | 1.7 | μA | 2 |
| | | | $V_{IN}$ = 6.0V | - | 0.9 | 1.8 | | |
| Output Current (*3) | $I_{OUT}$ | $V_{SEN}$ =0V $V_{DS}$ = 0.5V (N-ch) | $V_{IN}$ = 1.0V | 0.08 | 0.20 | - | mA | 3 |
| | | | $V_{IN}$ = 6.0V | 1.20 | 2.00 | - | | |
| | | $V_{SEN}$ = 6.0V $V_{DS}$ = 0.5V (P-ch) | $V_{IN}$ = 1.0V | - | -0.30 | -0.08 | mA | 4 |
| | | | $V_{IN}$ = 6.0V | - | -2.00 | -0.70 | | |
| Temperature Characteristics | $\dfrac{\Delta V_{DF}}{\Delta Ta \cdot V_{DF}}$ | -40 Ta 85 | | - | ±100 | - | ppm/ | 1 |
| Sense Resistance (*4) | $R_{SEN}$ | $V_{SEN}$ = 5.0V, $V_{IN}$ = 0V | | | E-4 | | MΩ | 5 |
| Delay Resistance (*5) | Rdelay | $V_{SEN}$ = 6.0V, $V_{IN}$ = 5.0V, Cd = 0V | | 1.6 | 2.0 | 2.4 | MΩ | 6 |
| Delay capacitance pin Sink Current | $I_{CD}$ | $V_{DS}$ = 0.5V, $V_{IN}$ = 1.0V | | - | 200 | - | μA | 6 |
| Delay Capacitance Pin Threshold Voltage | $V_{TCD}$ | $V_{SEN}$ = 6.0V, $V_{IN}$ = 1.0V | | 0.4 | 0.5 | 0.6 | V | 7 |
| | | $V_{SEN}$ = 6.0V, $V_{IN}$ = 6.0V | | 2.9 | 3.0 | 3.1 | | |
| Unspecified Operating Voltage (*6) | $V_{UNS}$ | $V_{IN}$ = $V_{SEN}$ = 0V ~ 0.7V | | - | 0.3 | 0.4 | V | 8 |
| Detect Delay Time (*7) | $T_{DF0}$ | $V_{IN}$ = 6.0V, $V_{SEN}$ = 6.0V 0.0V Cd: Open | | | 30 | 230 | μs | 9 |
| Release Delay Time (*8) | $T_{DR0}$ | $V_{IN}$ = 6.0V, $V_{SEN}$ = 0.0V 6.0V Cd: Open | | | 30 | 200 | μs | 9 |

NOTE:

*1: $V_{DF(T)}$: Setting detect voltage

*2: Current flows the sense resistor is not included.

*3: This numerical value is applied only to the XC6108C series (CMOS output).

*4: Calculated from the voltage value and the current value of the $V_{SEN}$.

*5: Calculated from the voltage value of the $V_{IN}$ and the current value of the Cd.

*6: The maximum voltage of the $V_{OUT}$ in the range of the $V_{IN}$ 0V to 0.7V when the $V_{IN}$ and the $V_{SEN}$ are short-circuited

This numerical value is applied only to the XC6108C series (CMOS output).

*7: Time which ranges from the state of $V_{SEN}$=$V_{DF}$ to the $V_{OUT}$ reaching 0.6V when the $V_{SEN}$ falls without connecting to the Cd pin.

*8: Time which ranges from the state of $V_{IN}$= $V_{DF}$ +$V_{HYS}$ to the $V_{OUT}$ reaching 5.4V when the $V_{SEN}$ rises without connecting to the Cd pin.

## ELECTRICAL CHARACTERISTICS (Continued)

XC6108xxxB                                                                                                    Ta=25

| PARAMETER | SYMBOL | CONDITIONS | | MIN. | TYP. | MAX. | UNITS | CIRCUITS |
|---|---|---|---|---|---|---|---|---|
| Operating Voltage | $V_{IN}$ | $V_{DF(T)}$ = 0.8 ~ 5.0V (*1) | | 1.0 | - | 6.0 | V | - |
| Detect Voltage | $V_{DF}$ | $V_{IN}$ = 1.0 ~ 6.0V | | | E-1 | | V | 1 |
| Hysteresis Range1 | $V_{HYS1}$ | $V_{IN}$ = 1.0 ~ 6.0V | | | E-3 | | V | 1 |
| Detect Voltage Line Regulation | $\frac{V_{DF}}{V_{IN} \cdot V_{DF}}$ | $V_{IN}$ = 1.0 ~ 6.0V | | - | ±0.1 | - | %/V | 1 |
| Supply Current 1 (*2) | $I_{SS1}$ | $V_{SEN}$ = $V_{DF}$ x 0.9 | $V_{IN}$ = 1.0V | - | 0.6 | 1.5 | µA | 2 |
| | | | $V_{IN}$ = 6.0V | - | 0.7 | 1.6 | | |
| Supply Current 2 (*2) | $I_{SS2}$ | $V_{SEN}$ = $V_{DF}$ x 1.1 | $V_{IN}$ = 1.0V | - | 0.8 | 1.7 | µA | 2 |
| | | | $V_{IN}$ = 6.0V | - | 0.9 | 1.8 | | |
| Output Current (*3) | $I_{OUT}$ | $V_{SEN}$ =0V $V_{DS}$ = 0.5V (N-ch) | $V_{IN}$ = 1.0V | 0.08 | 0.20 | - | mA | 3 |
| | | | $V_{IN}$ = 6.0V | 1.20 | 2.00 | - | | |
| | | $V_{SEN}$ = 6.0V $V_{DS}$ = 0.5V (P-ch) | $V_{IN}$ = 1.0V | - | -0.30 | -0.08 | mA | 4 |
| | | | $V_{IN}$ = 6.0V | - | -2.00 | -0.70 | | |
| Temperature Characteristics | $\frac{V_{DF}}{Ta \cdot V_{DF}}$ | -40    Ta    85 | | - | ±100 | - | ppm/ | 1 |
| Sense Resistance (*4) | $R_{SEN}$ | $V_{SEN}$ = 5.0V, $V_{IN}$ = 0V | | | E-4 | | MΩ | 5 |
| Delay Resistance (*5) | Rdelay | $V_{SEN}$ = 6.0V, $V_{IN}$ = 5.0V, Cd = 0V | | 1.6 | 2.0 | 2.4 | MΩ | 6 |
| Delay capacitance pin Sink Current | $I_{CD}$ | $V_{DS}$ = 0.5V, $V_{IN}$ = 1.0V | | - | 200 | - | µA | 6 |
| Delay Capacitance Pin Threshold Voltage | $V_{TCD}$ | $V_{SEN}$ = 6.0V, $V_{IN}$ = 1.0V | | 0.4 | 0.5 | 0.6 | V | 7 |
| | | $V_{SEN}$ = 6.0V, $V_{IN}$ = 6.0V | | 2.9 | 3.0 | 3.1 | | |
| Unspecified Operating Voltage (*6) | $V_{UNS}$ | $V_{IN}$ = $V_{SEN}$ = 0V ~ 0.7V | | - | 0.3 | 0.4 | V | 8 |
| Detect Delay Time (*7) | $T_{DF0}$ | $V_{IN}$ = 6.0V, $V_{SEN}$ = 6.0V  0.0V  Cd: Open | | | 30 | 230 | µs | 9 |
| Release Delay Time (*8) | $T_{DR0}$ | $V_{IN}$ = 6.0V, $V_{SEN}$ = 0.0V  6.0V  Cd: Open | | | 30 | 200 | µs | 9 |

NOTE:

*1: $V_{DF(T)}$: Setting detect voltage

*2: Current flows the sense resistor is not included.

*3: This numerical value is applied only to the XC6108C series (CMOS output).

*4: Calculated from the voltage value and the current value of the $V_{SEN}$.

*5: Calculated from the voltage value of the $V_{IN}$ and the current value of the Cd.

*6: The maximum voltage of the $V_{OUT}$ in the range of the $V_{IN}$ 0V to 0.7V when the $V_{IN}$ and the $V_{SEN}$ are short-circuited

   This numerical value is applied only to the XC6108C series (CMOS output).

*7: Time which ranges from the state of $V_{SEN}$=$V_{DF}$ to the $V_{OUT}$ reaching 0.6V when the $V_{SEN}$ falls without connecting to the Cd pin.

*8: Time which ranges from the state of $V_{IN}$= $V_{DF}$ +$V_{HYS}$ to the $V_{OUT}$ reaching 5.4V when the $V_{SEN}$ rises without connecting to the Cd pin.

# ELECTRICAL CHARACTERISTICS (Continued)

XC6108xxxC

Ta=25

| PARAMETER | SYMBOL | CONDITIONS | | | MIN. | TYP. | MAX. | UNITS | CIRCUITS |
|---|---|---|---|---|---|---|---|---|---|
| Operating Voltage | $V_{IN}$ | $V_{DF(T)}$ = 0.8 ~ 5.0V (*1) | | | 1.0 | - | 6.0 | V | - |
| Detect Voltage | $V_{DF}$ | $V_{IN}$ = 1.0 ~ 6.0V | | | | E-1 | | V | 1 |
| Hysteresis Range1 | $V_{HYS1}$ | $V_{IN}$ = 1.0 ~ 6.0V | | | | E-2 | | V | 1 |
| Detect Voltage Line Regulation | $\frac{V_{DF}}{V_{IN} \cdot V_{DF}}$ | $V_{IN}$ = 1.0 ~ 6.0V | | | - | ±0.1 | - | %/V | 1 |
| Supply Current 1 (*2) | $I_{SS1}$ | $V_{SEN}$ = $V_{DF}$ x 0.9 | $V_{IN}$ = 1.0V | | - | 0.6 | 1.5 | μA | 2 |
| | | | $V_{IN}$ = 6.0V | | - | 0.7 | 1.6 | | |
| Supply Current 2 (*2) | $I_{SS2}$ | $V_{SEN}$ = $V_{DF}$ x 1.1 | $V_{IN}$ = 1.0V | | - | 0.8 | 1.7 | μA | 2 |
| | | | $V_{IN}$ = 6.0V | | - | 0.9 | 1.8 | | |
| Output Current (*3) | $I_{OUT}$ | $V_{SEN}$ =0V $V_{DS}$ = 0.5V (N-ch) | $V_{IN}$ = 1.0V | | 0.08 | 0.20 | - | mA | 3 |
| | | | $V_{IN}$ = 6.0V | | 1.20 | 2.00 | - | | |
| | | $V_{SEN}$ = 6.0V $V_{DS}$ = 0.5V (P-ch) | $V_{IN}$ = 1.0V | | - | -0.30 | -0.08 | mA | 4 |
| | | | $V_{IN}$ = 6.0V | | - | -2.00 | -0.70 | | |
| Temperature Characteristics | $\frac{V_{DF}}{Ta \cdot V_{DF}}$ | -40 Ta 85 | | | - | ±100 | - | ppm/ | 1 |
| Sense Resistance (*4) | $R_{SEN}$ | $V_{SEN}$ = 5.0V, $V_{IN}$ = 0V | | | | E-4 | | MΩ | 5 |
| Unspecified Operating Voltage (*5) | $V_{UNS}$ | $V_{IN}$ = $V_{SEN}$ = 0V ~ 0.7V | | | - | 0.3 | 0.4 | V | 7 |
| Detect Delay Time (*6) | $T_{DF0}$ | $V_{IN}$ = 6.0V, $V_{SEN}$ = 6.0V 0.0V | | | | 30 | 230 | μs | 9 |
| Release Delay Time (*7) | $T_{DR0}$ | $V_{IN}$ = 6.0V, $V_{SEN}$ = 0.0V 6.0V | | | | 30 | 200 | μs | 9 |

NOTE:

*1: $V_{DF(T)}$: Setting detect voltage

*2: Current flows the sense resistor is not included.

*3: This numerical value is applied only to the XC6108C series (CMOS output).

*4: Calculated from the voltage value and the current value of the $V_{SEN}$.

*5: The maximum voltage of the $V_{OUT}$ in the range of the $V_{IN}$ 0V to 0.7V when the $V_{IN}$ and the $V_{SEN}$ are short-circuited

　　This numerical value is applied only to the XC6108C series (CMOS output).

*6: Time which ranges from the state of $V_{SEN}$=$V_{DF}$ to the $V_{OUT}$ reaching 0.6V when the $V_{SEN}$ falls.

*7: Time which ranges from the state of $V_{IN}$= $V_{DF}$ +$V_{HYS}$ to the $V_{OUT}$ reaching 5.4V when the $V_{SEN}$ rises.

## ELECTRICAL CHARACTERISTICS (Continued)

XC6108xxxD
Ta=25

| PARAMETER | SYMBOL | CONDITIONS | | | MIN. | TYP. | MAX. | UNITS | CIRCUITS |
|---|---|---|---|---|---|---|---|---|---|
| Operating Voltage | $V_{IN}$ | $V_{DF(T)} = 0.8 \sim 5.0V$ (*1) | | | 1.0 | - | 6.0 | V | - |
| Detect Voltage | $V_{DF}$ | $V_{IN} = 1.0 \sim 6.0V$ | | | | E-1 | | V | 1 |
| Hysteresis Range1 | $V_{HYS1}$ | $V_{IN} = 1.0 \sim 6.0V$ | | | | E-3 | | V | 1 |
| Detect Voltage Line Regulation | $\dfrac{V_{DF}}{V_{IN} \cdot V_{DF}}$ | $V_{IN} = 1.0 \sim 6.0V$ | | | - | ±0.1 | - | %/V | 1 |
| Supply Current 1 (*2) | $I_{SS1}$ | $V_{SEN} =$ $V_{DF}$ x 0.9 | $V_{IN} = 1.0V$ | | - | 0.6 | 1.5 | μA | 2 |
| | | | $V_{IN} = 6.0V$ | | - | 0.7 | 1.6 | | |
| Supply Current 2 (*2) | $I_{SS2}$ | $V_{SEN} =$ $V_{DF}$ x 1.1 | $V_{IN} = 1.0V$ | | - | 0.8 | 1.7 | μA | 2 |
| | | | $V_{IN} = 6.0V$ | | - | 0.9 | 1.8 | | |
| Output Current (*3) | $I_{OUT}$ | $V_{SEN} = 0V$ $V_{DS} = 0.5V$ (N-ch) | $V_{IN} = 1.0V$ | | 0.08 | 0.20 | - | mA | 3 |
| | | | $V_{IN} = 6.0V$ | | 1.20 | 2.00 | - | | |
| | | $V_{SEN} = 6.0V$ $V_{DS} = 0.5V$ (P-ch) | $V_{IN} = 1.0V$ | | - | -0.30 | -0.08 | mA | 4 |
| | | | $V_{IN} = 6.0V$ | | - | -2.00 | -0.70 | | |
| Temperature Characteristics | $\dfrac{V_{DF}}{Ta \cdot V_{DF}}$ | $-40 \le Ta \le 85$ | | | - | ±100 | - | ppm/ | 1 |
| Sense Resistance (*4) | $R_{SEN}$ | $V_{SEN} = 5.0V$, $V_{IN} = 0V$ | | | | E-4 | | MΩ | 5 |
| Unspecified Operating Voltage (*5) | $V_{UNS}$ | $V_{IN} = V_{SEN} = 0V \sim 0.7V$ | | | - | 0.3 | 0.4 | V | 7 |
| Detect Delay Time (*6) | $T_{DF0}$ | $V_{IN} = 6.0V, V_{SEN} = 6.0V \to 0.0V$ | | | | 30 | 230 | μs | 9 |
| Release Delay Time (*7) | $T_{DR0}$ | $V_{IN} = 6.0V, V_{SEN} = 0.0V \to 6.0V$ | | | | 30 | 200 | μs | 9 |

NOTE:

*1: $V_{DF(T)}$: Setting detect voltage

*2: Current flows the sense resistor is not included.

*3: This numerical value is applied only to the XC6108C series (CMOS output).

*4: Calculated from the voltage value and the current value of the $V_{SEN}$.

*5: The maximum voltage of the $V_{OUT}$ in the range of the $V_{IN}$ 0V to 0.7V when the $V_{IN}$ and the $V_{SEN}$ are short-circuited
   This numerical value is applied only to the XC6108C series (CMOS output).

*6: Time which ranges from the state of $V_{SEN} = V_{DF}$ to the $V_{OUT}$ reaching 0.6V when the $V_{SEN}$ falls.

*7: Time which ranges from the state of $V_{IN} = V_{DF} + V_{HYS}$ to the $V_{OUT}$ reaching 5.4V when the $V_{SEN}$ rises.

## VOLTAGE CHART

| SYMBOL | E-1 | | E-2 | | E-3 | | E-4 | |
|---|---|---|---|---|---|---|---|---|
| SETTING OUTPUT VOLTAGE | DETECT VOLTAGE (*1) (V) | | HYSTERESIS RANGE (V) | | HYSTERESIS RANGE (V) | | SENSE RESISTANCE (MΩ) | |
| VDF(T) (V) | VDF | | VHYS | | VHYS | | RSEN | |
| | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | TYP. |
| 0.8 | 0.770 | 0.830 | 0.015 | 0.066 | | 0.008 | 10 | 20 |
| 0.9 | 0.870 | 0.930 | 0.017 | 0.074 | | 0.009 | | |
| 1.0 | 0.970 | 1.030 | 0.019 | 0.082 | | 0.010 | | |
| 1.1 | 1.070 | 1.130 | 0.021 | 0.090 | | 0.011 | | |
| 1.2 | 1.170 | 1.230 | 0.023 | 0.098 | | 0.012 | | |
| 1.3 | 1.270 | 1.330 | 0.025 | 0.106 | | 0.013 | | |
| 1.4 | 1.370 | 1.430 | 0.027 | 0.114 | | 0.014 | | |
| 1.5 | 1.470 | 1.530 | 0.029 | 0.122 | | 0.015 | | |
| 1.6 | 1.568 | 1.632 | 0.031 | 0.131 | | 0.016 | | |
| 1.7 | 1.666 | 1.734 | 0.033 | 0.085 | | 0.017 | | |
| 1.8 | 1.764 | 1.836 | 0.035 | 0.147 | | 0.018 | | |
| 1.9 | 1.862 | 1.938 | 0.037 | 0.155 | | 0.019 | | |
| 2.0 | 1.960 | 2.040 | 0.039 | 0.163 | | 0.020 | 13 | 24 |
| 2.1 | 2.058 | 2.142 | 0.041 | 0.171 | | 0.021 | | |
| 2.2 | 2.156 | 2.244 | 0.043 | 0.180 | | 0.022 | | |
| 2.3 | 2.254 | 2.346 | 0.045 | 0.188 | | 0.023 | | |
| 2.4 | 2.352 | 2.448 | 0.047 | 0.196 | | 0.024 | | |
| 2.5 | 2.450 | 2.550 | 0.049 | 0.204 | | 0.026 | | |
| 2.6 | 2.548 | 2.652 | 0.051 | 0.212 | | 0.027 | | |
| 2.7 | 2.646 | 2.754 | 0.053 | 0.220 | | 0.028 | | |
| 2.8 | 2.744 | 2.856 | 0.055 | 0.228 | | 0.029 | | |
| 2.9 | 2.842 | 2.958 | 0.057 | 0.237 | 0 | 0.030 | | |
| 3.0 | 2.940 | 3.060 | 0.059 | 0.245 | | 0.031 | | |
| 3.1 | 3.038 | 3.162 | 0.061 | 0.253 | | 0.032 | | |
| 3.2 | 3.136 | 3.264 | 0.063 | 0.261 | | 0.033 | | |
| 3.3 | 3.234 | 3.366 | 0.065 | 0.269 | | 0.034 | | |
| 3.4 | 3.332 | 3.468 | 0.067 | 0.277 | | 0.035 | | |
| 3.5 | 3.430 | 3.570 | 0.069 | 0.286 | | 0.036 | | |
| 3.6 | 3.528 | 3.672 | 0.071 | 0.294 | | 0.037 | | |
| 3.7 | 3.626 | 3.774 | 0.073 | 0.302 | | 0.038 | | |
| 3.8 | 3.724 | 3.876 | 0.074 | 0.310 | | 0.039 | | |
| 3.9 | 3.822 | 3.978 | 0.076 | 0.318 | | 0.040 | | |
| 4.0 | 3.920 | 4.080 | 0.078 | 0.326 | | 0.041 | 15 | 28 |
| 4.1 | 4.018 | 4.182 | 0.080 | 0.335 | | 0.042 | | |
| 4.2 | 4.116 | 4.284 | 0.082 | 0.343 | | 0.043 | | |
| 4.3 | 4.214 | 4.386 | 0.084 | 0.351 | | 0.044 | | |
| 4.4 | 4.312 | 4.488 | 0.086 | 0.359 | | 0.045 | | |
| 4.5 | 4.410 | 4.590 | 0.088 | 0.367 | | 0.046 | | |
| 4.6 | 4.508 | 4.692 | 0.090 | 0.375 | | 0.047 | | |
| 4.7 | 4.606 | 4.794 | 0.092 | 0.384 | | 0.048 | | |
| 4.8 | 4.704 | 4.896 | 0.094 | 0.392 | | 0.049 | | |
| 4.9 | 4.802 | 4.998 | 0.096 | 0.400 | | 0.050 | | |
| 5.0 | 4.900 | 5.100 | 0.098 | 0.408 | | 0.051 | | |

NOTE:

*1: When VDF(T) 1.4V, the detection accuracy is ± 30mV.

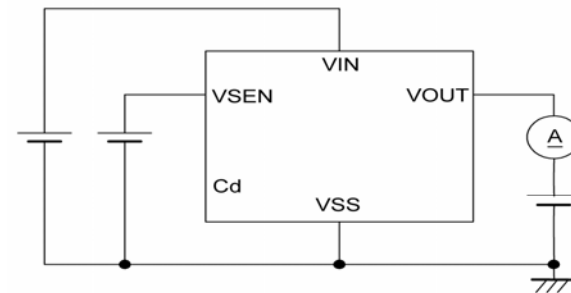When VDF(T) 1.5V, the detection accuracy is ± 2%.

## TEST CIRCUITS

Circuit 1



R=100kΩ
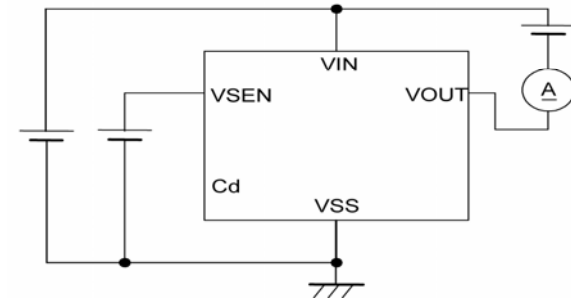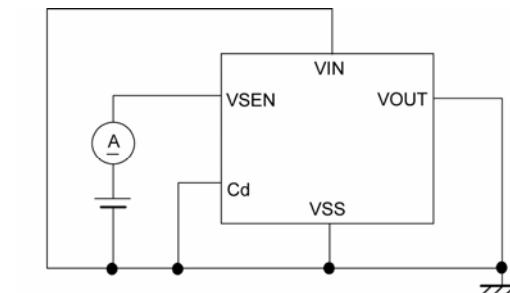(No resistor needed for CMOS output products)
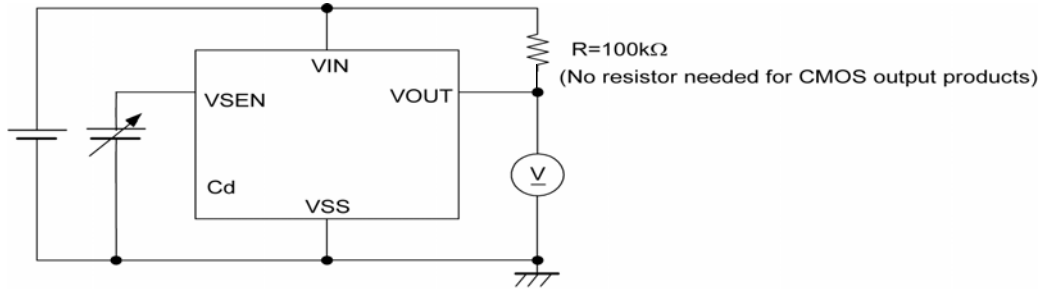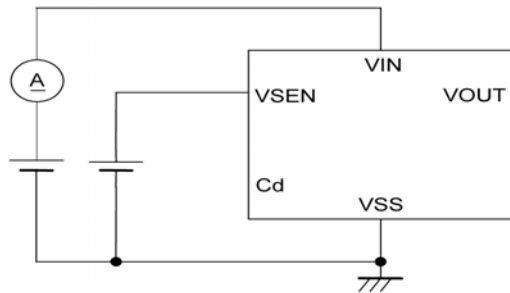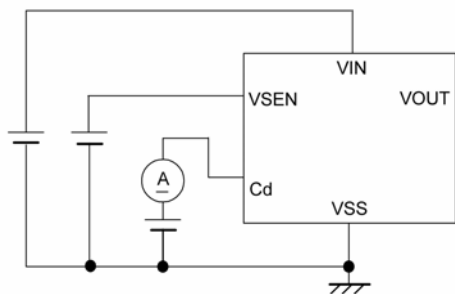
Circuit 2



Circuit 3



Circuit 4



Circuit 5

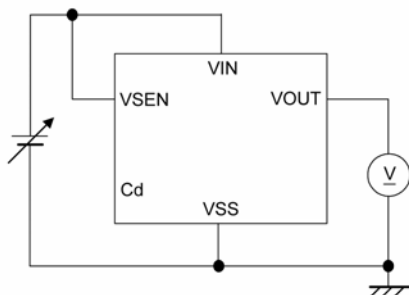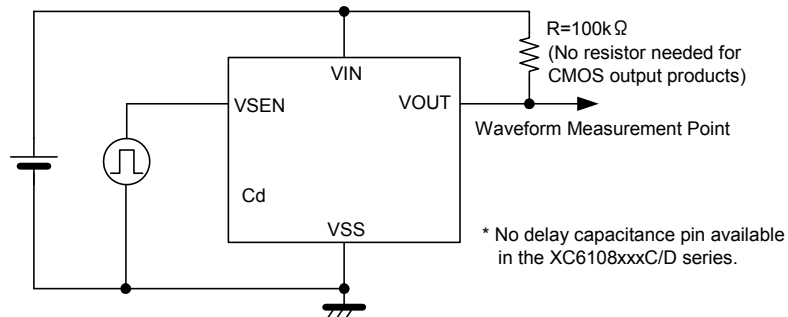# TEST CIRCUITS (Continued)

Circuit 6



Circuit 7



R=100kΩ
(No resistor needed for CMOS output products)

Circuit 8



Circuit 9



R=100kΩ
(No resistor needed for
CMOS output products)

Waveform Measurement Point

* No delay capacitance pin available
  in the XC6108xxxC/D series.
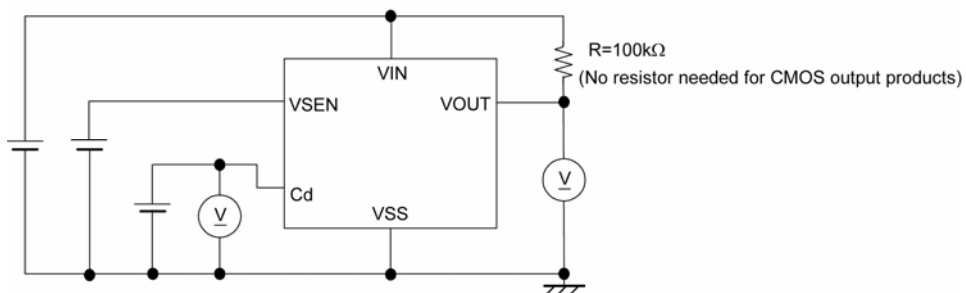
## OPERATIONAL EXPLANATION

A typical circuit example is shown in Figure 1, and the timing chart of Figure 1 is shown in Figure 2 on page 14.

As an early state, the sense pin is applied sufficiently high voltage (6.0V MAX.) and the delay capacitance (Cd) is charged to the power supply input voltage, ($V_{IN}$: 1.0V MIN., 6.0V MAX.). While the sense pin voltage ($V_{SEN}$) starts dropping to reach the detect voltage ($V_{DF}$) ($V_{SEN}$>$V_{DF}$), the output voltage ($V_{OUT}$) keeps the "High" level (=$V_{IN}$).
* If a pull-up resistor of the XC6108N series (N-ch open drain) is connected to added power supply different from the input voltage pin, the "High" level will be a voltage value where the pull-up resistor is connected.

When the sense pin voltage keeps dropping and becomes equal to the detect voltage ($V_{SEN}$ =$V_{DF}$), an N-ch transistor (M3) for the delay capacitance (Cd) discharge is turned ON, and starts to discharge the delay capacitance (Cd). An inverter (Inv.1) operates as a comparator of the reference voltage $V_{IN}$, and the output voltage changes into the "Low" level (=$V_{SS}$). The detect delay time [$T_{DF}$] is defined as time which ranges from $V_{SEN}$=$V_{DF}$ to the $V_{OUT}$ of "Low" level (especially, when the Cd pin is not connected: $T_{DF0}$).

While the sense pin voltage keeps below the detect voltage, the delay capacitance (Cd) is discharged to the ground voltage (=$V_{SS}$) level. Then, the output voltage maintains the "Low" level while the sense pin voltage increases again to reach the release voltage ($V_{SEN}$< $V_{DF}$ +$V_{HYS}$).

When the sense pin voltage continues to increase up to the release voltage level ($V_{DF}$+$V_{HYS}$), the N-ch transistor (M3) for the delay capacitance (Cd) discharge will be turned OFF, and the delay capacitance (Cd) will start discharging via a delay resistor (Rdelay). The inverter (Inv.1) will operate as a comparator (Rise Logic Threshold: $V_{TLH}$=$V_{TCD}$, Fall Logic Threshold: $V_{THL}$=$V_{SS}$) while the sense pin voltage keeps higher than the detect voltage ($V_{SEN}$ > $V_{DF}$).

While the delay capacitance pin voltage ($V_{CD}$) rises to reach the delay capacitance pin threshold voltage ($V_{TCD}$) with the sense pin voltage equal to the release voltage or higher, the sense pin will be charged by the time constant of the RC series circuit. Assuming the time to the release delay time ($T_{DR}$), it can be given by the formula (1).

$$T_{DR} = Rdelay \times Cd \times In (1  V_{TCD} / V_{IN}) \dots (1)$$
* In = a natural logarithm

The release delay time can also be briefly calculated with the formula (2) because the delay resistance is 2.0M (TYP.) and the delay capacitance pin voltage is $V_{IN}$ /2 (TYP.)

$$T_{DR} = 2.0e6 \times Cd \times 0.69 \dots (2)$$

As an example, presuming that the delay capacitance is 0.68μ F, $T_{DR}$ is :

$$2.0e6 \times 0.68e  6 \times 0.69 = 938 (ms)$$

* Note that the release delay time may remarkably be short when the delay capacitance (Cd) is not discharged to the ground (=$V_{SS}$) level because time described in    is short.

When the delay capacitance pin voltage reaches to the delay capacitance pin threshold voltage ($V_{CD}$=$V_{TCD}$), the inverter (Inv.1) will be inverted. As a result, the output voltage changes into the "High" (=$V_{IN}$) level. $T_{DR0}$ is defined as time which ranges from $V_{SEN}$=$V_{DF}$+$V_{HYS}$ to the $V_{OUT}$ of "High" level without connecting to the Cd.

While the sense voltage is higher than the detect voltage ($V_{SEN}$ > $V_{DF}$), the delay capacitance pin is charged until the delay capacitance pin voltage becomes the input voltage level. Therefore, the output voltage maintains the "High"(=$V_{IN}$) level.

## OPERATIONAL EXPLANATION (Continued)

Function Chart

| V~SEN~ | Cd | TRANSITION OF V~OUT~ CONDITION* | | |
|---|---|---|---|---|
| | | | | |
| L | L | L | | L |
| | H | | | |
| | L | H | | |
| | H | | | |
| H | L | L | | L |
| | H | | | |
| | L | H | | H |
| | H | | | |

*V~OUT~ transits from condition    to    because of the combination of V~SEN~ and Cd.

  Example

ex. 1) V~OUT~ ranges from 'L' to 'H' in case of VSEN = 'H' (VDR   VSEN), Cd='H' (VTCD   Cd) while VOUT is 'L'.

ex. 2) V~OUT~ maintains 'H' when Cd ranges from 'H' to 'L', VSEN='H' and Cd='L' when V~OUT~ becomes 'H' in ex.1.


Release Delay Time Chart

| DELAY CAPACITANCE [Cd] (μF) | RELEASE DELAY TIME [T~DR~] (TYP.) (ms) | RELEASE DELAY TIME [T~DR~] (MIN. ~ MAX.) (ms) |
|---|---|---|
| 0.010 | 13.8 | 11.0 ~ 16.6 |
| 0.022 | 30.4 | 24.3 ~ 36.4 |
| 0.047 | 64.9 | 51.9 ~ 77.8 |
| 0.100 | 138 | 110 ~ 166 |
| 0.220 | 304 | 243~ 364 |
| 0.470 | 649 | 519 ~ 778 |
| 1.000 | 1380 | 1100 ~ 1660 |

## OPERATIONAL EXPLANATION (Continued)

Figure 1: Typical application circuit example
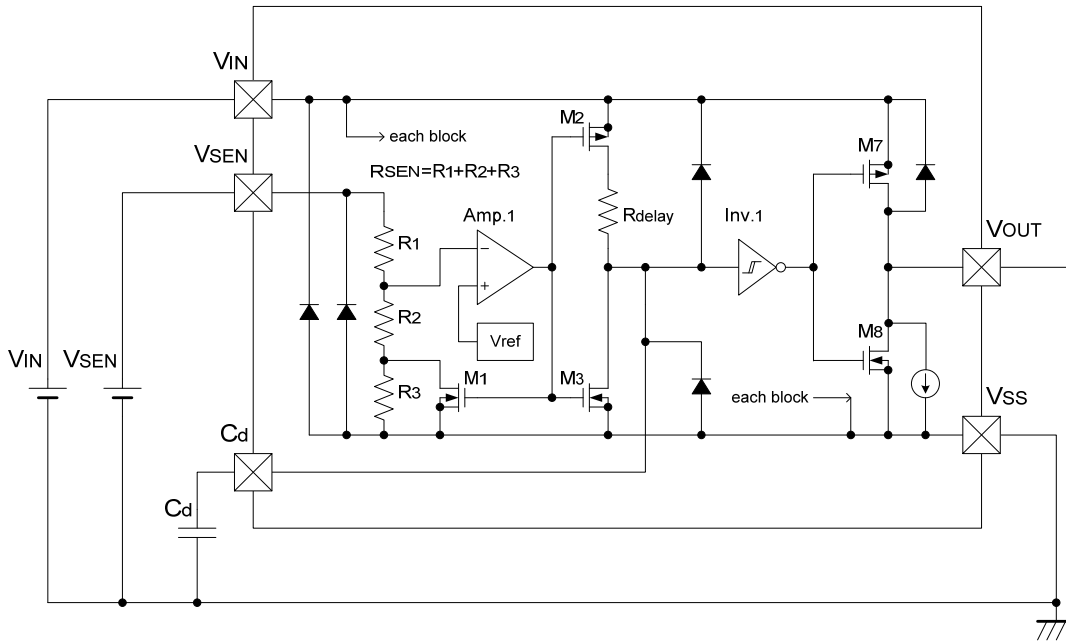
*The XC6108N series (N-ch open drain output) requires a pull-up resistor for pulling up output.

Figure 2: The timing chart of Figure 1
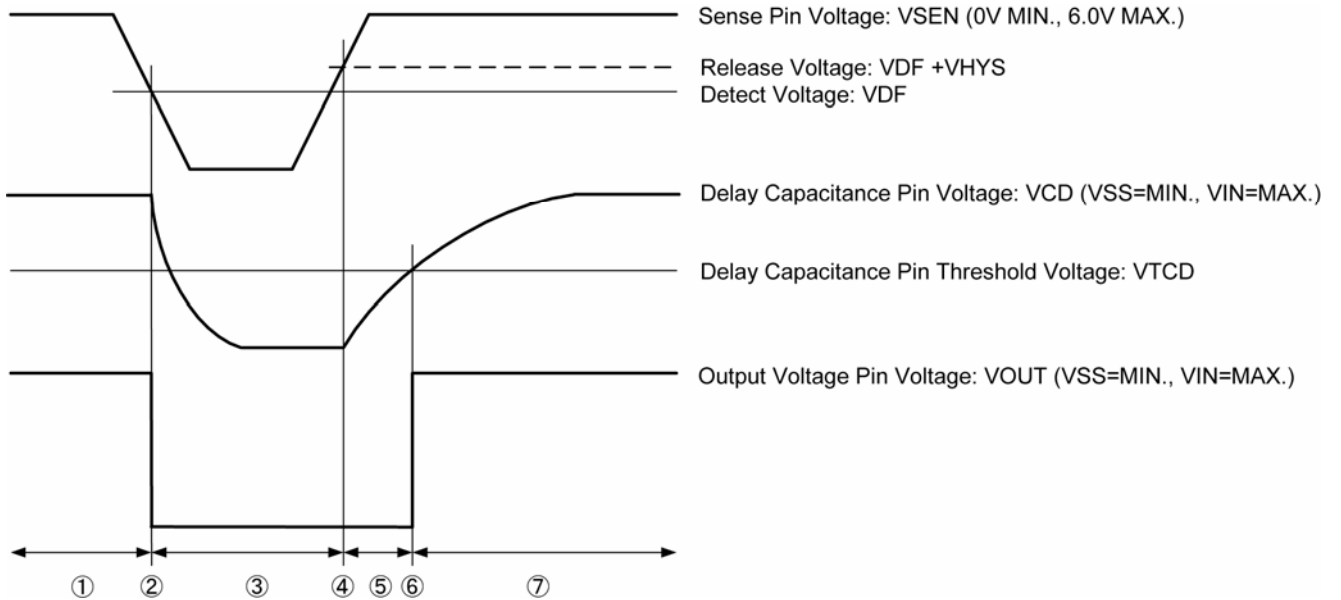
## NOTES ON USE

1. Use this IC within the stated maximum ratings.  Operation beyond these limits may cause degrading or permanent damage to the device.

2. The power supply input pin voltage drops by the resistance between power supply and the V$_{IN}$ pin, and by through current at operation of the IC.  At this time, the operation may be wrong if the power supply input pin voltage falls below the minimum operating voltage range.  In CMOS output, for output current, drops in the power supply input pin voltage similarly occur.  Moreover, in CMOS output, when the V$_{IN}$ pin and the sense pin are short-circuited and used, oscillation of the circuit may occur if the drops in voltage, which caused by through current at operation of the IC, exceed the hysteresis voltage.  Note it especially when you use the IC with the V$_{IN}$ pin connected to a resistor.

3. When the setting voltage is less than 1.0V, be sure to separate the V$_{IN}$ pin and the sense pin, and to apply the voltage over 1.0V to the V$_{IN}$ pin.

4. Note that a rapid and high fluctuation of the power supply input pin voltage may cause a wrong operation.

5. When there is a possibility of which the power supply input pin voltage falls rapidly (e.g.: 6.0V to 0V) at release operation with the delay capacitance pin (Cd) connected to a capacitor, use a schottky barrier diode connected between the V$_{IN}$ pin and the Cd pin as the Figure 3 shown below.

6. In N-ch open drain output, a pull-up resistor connected to the output voltage pin should be 100k-200k .

Figure 3: Circuit example with the delay capacitance pin (Cd) connected to a schottky barrier diode
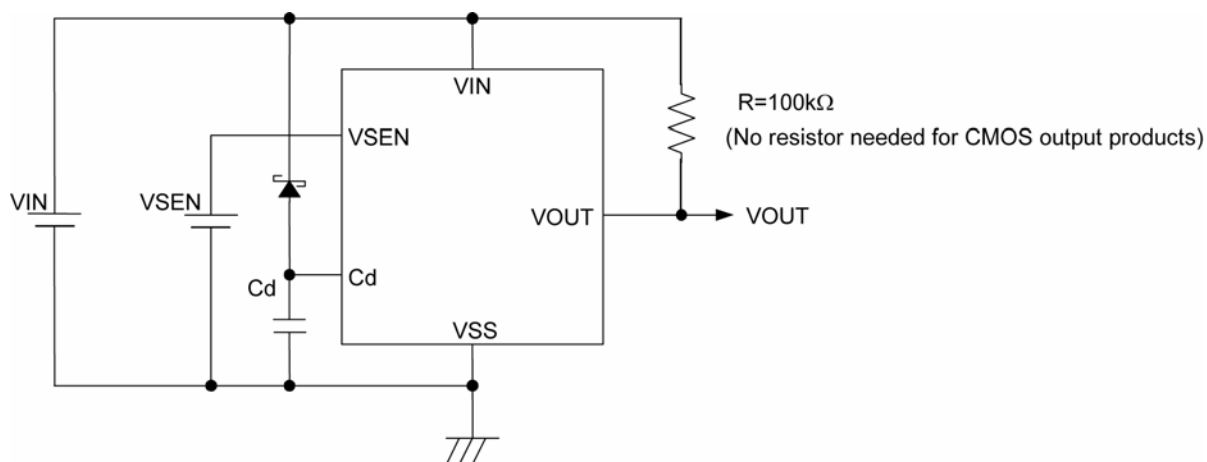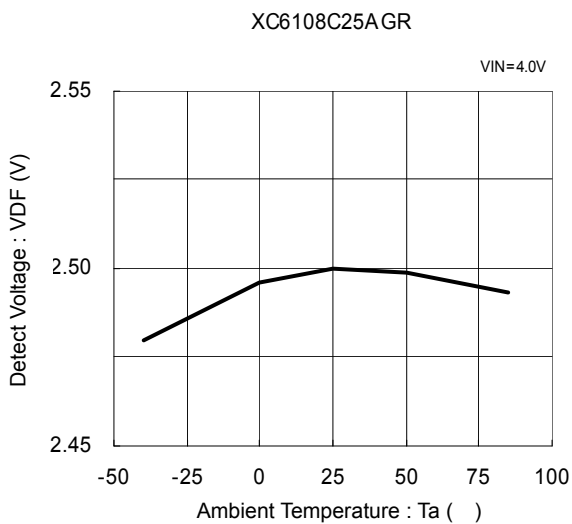
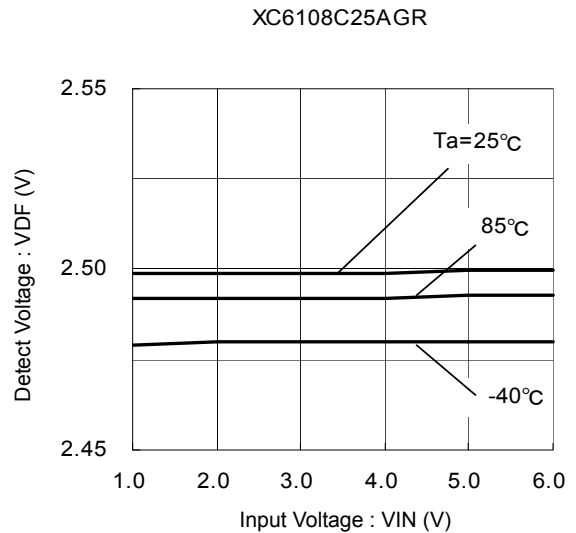## TYPICAL PERFORMANCE CHARACTERISTICS

(1) Supply Current vs. Sense Voltage

XC6108C25AGR
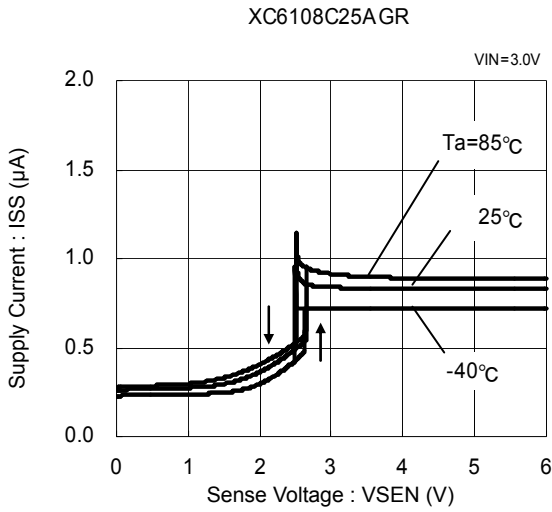


(2) Supply Current vs. Input Voltage

XC6108C25AGR



XC6108C25AGR
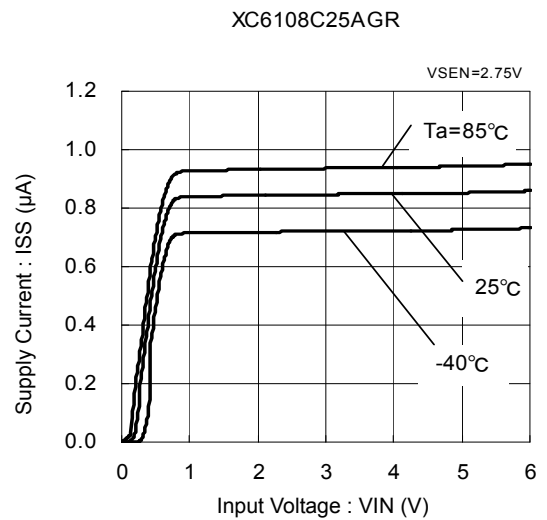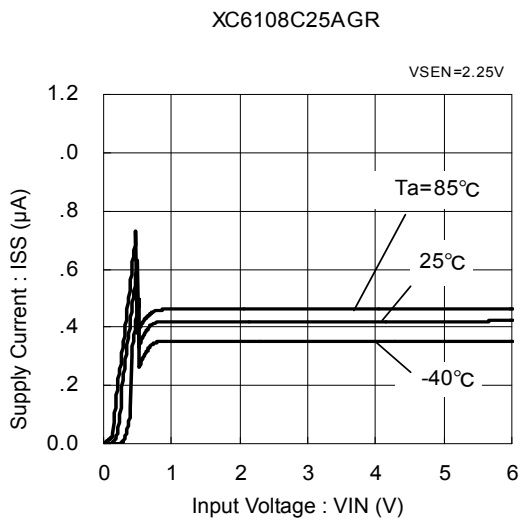


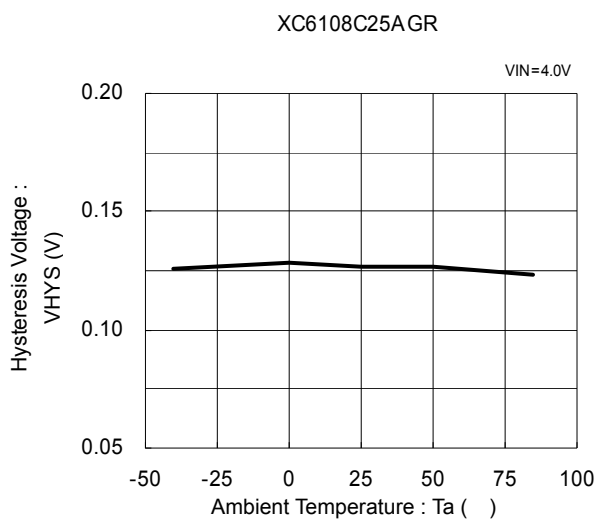(3) Detect Voltage vs. Ambient Temperature

XC6108C25AGR



(4) Detect Voltage vs. Input Voltage

XC6108C25AGR

# TYPICAL PERFORMANCE CHARACTERISTICS (Continued)
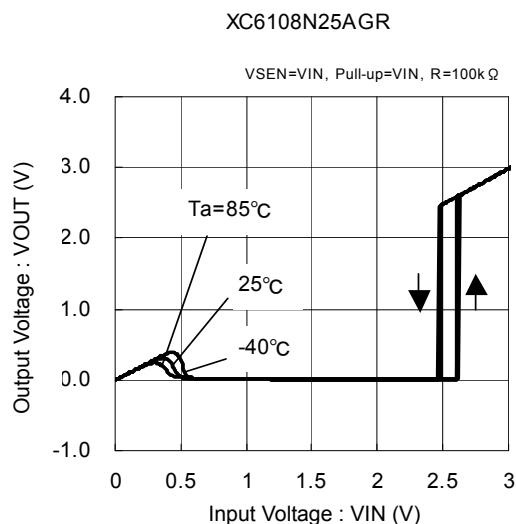
(5) Hysteresis Voltage vs. Ambient Temperature

XC6108C25AGR
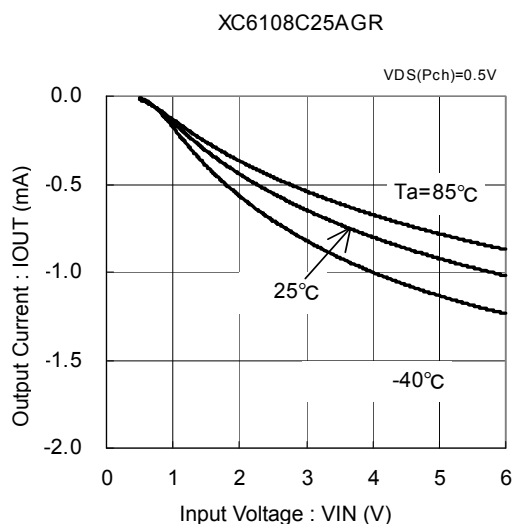
VIN=4.0V

(6) CD Pin Sink Current vs. Input Voltage

XC6108C25AGR

VSEN=0V, VDS=0.5V
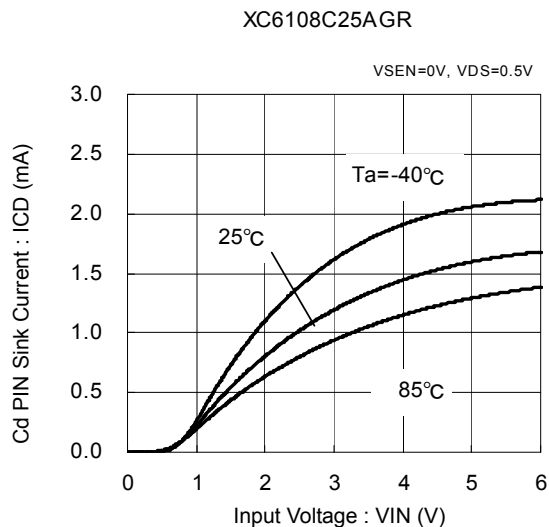
(7) Output Voltage vs. Sense Voltage

XC6108C25AGR

Ta=25℃
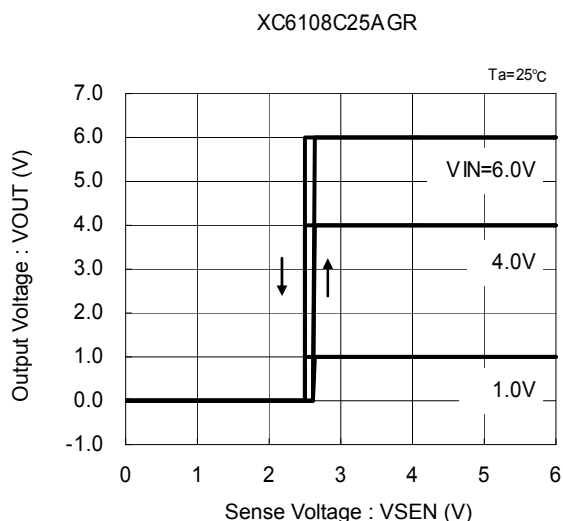
(8) Output Voltage vs. Input Voltage

XC6108N25AGR

VSEN=VIN, Pull-up=VIN, R=100kΩ

(9) Output Current vs. Input Voltage

XC6108C25AGR

VDS(Nch)=0.5V

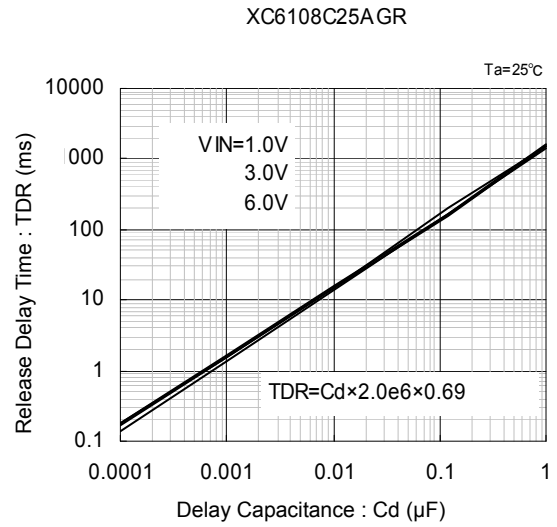XC6108C25AGR

VDS(Pch)=0.5V
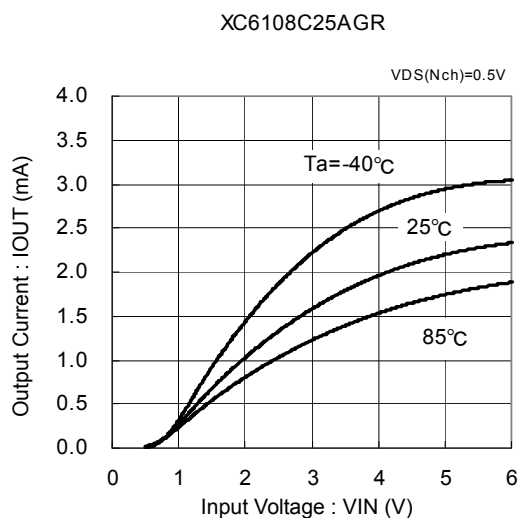
## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(10) Delay Resistance vs. Ambient Temperature
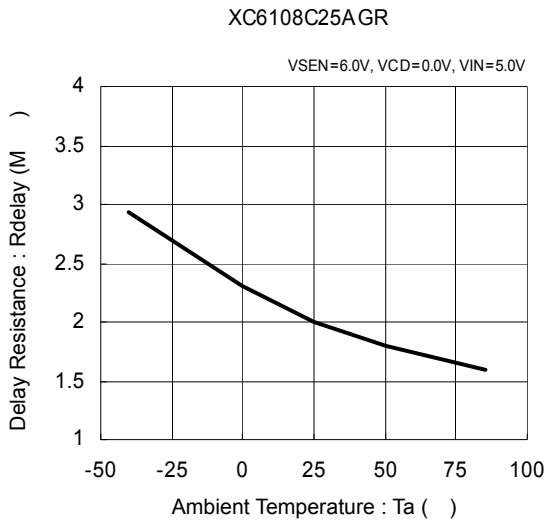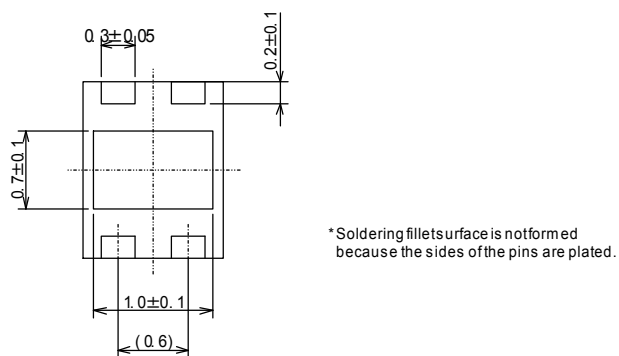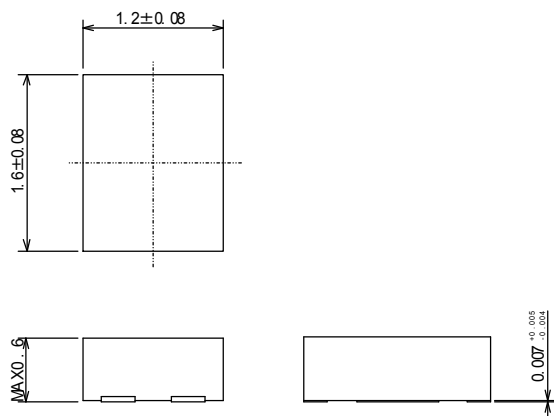
(11) Release Delay Time vs. Delay Capacitance

XC6108C25AGR

XC6108C25AGR





(12) Detect Delay Time vs. Delay Capacitance

XC6108C25AGR

# PACKAGING INFORMATION

USP-4

1.2±0.08

1.6±0.08

MAX0.6

0.007 +0.005 -0.004

0.3±0.05

0.2±0.1

0.7±0.1

1.0±0.1

(0.6)

* Soldering fillet surface is not formed
because the sides of the pins are plated.

SOT-25

2.9±0.2

1.9±0.2

0.4 +0.1 -0.06

0.4 +0.1 -0.06

0~15°

MIN0.2

2.8±0.2

1.6 +0.1 -0.1

0~0.1

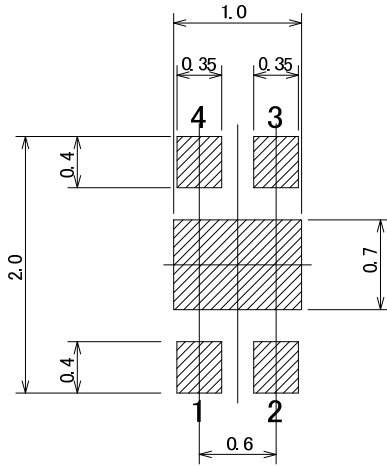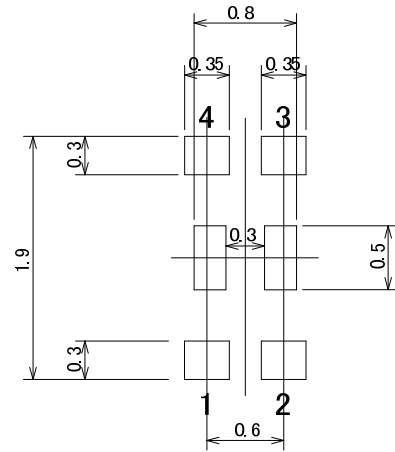0.4 +0.1 -0.06

0.15 +0.1 -0.06

MIN0.2

(0.95)(0.95)

1.0~1.3

1.1±0.1

0.1
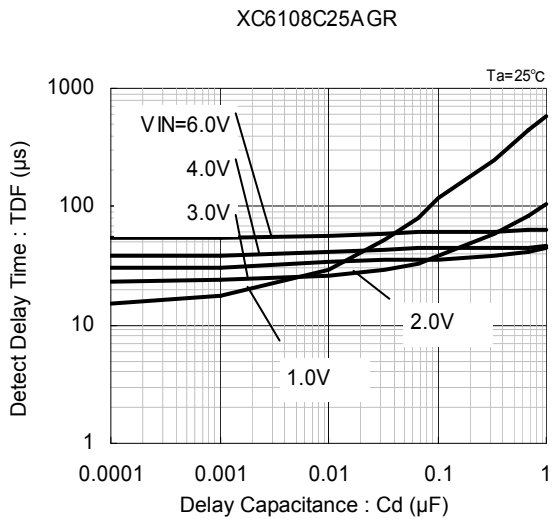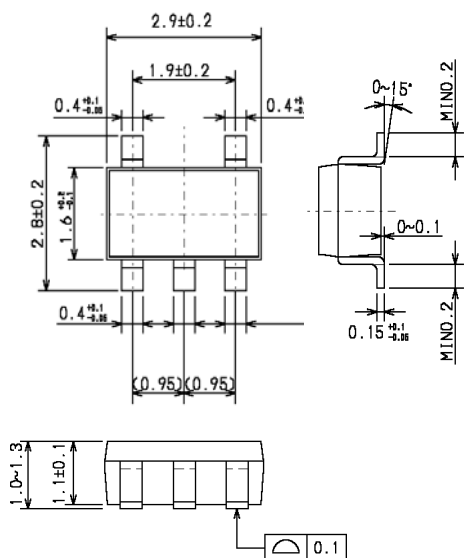
## PACKAGING INFORMATION (Continued)
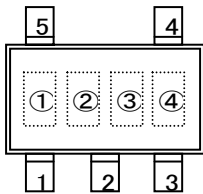
USP-4 Recommended Pattern Layout

USP- Recommended Metal Mask Design

## MARKING RULE

SOT-25

SOT-25
(TOP VIEW)

Represents output configuration and integer number of detect voltage

CMOS Output (XC6108C Series)

| MARK | VOLTAGE (V) |
|------|-------------|
| A | 0.x |
| B | 1.x |
| C | 2.x |
| D | 3.x |
| E | 4.x |
| F | 5.x |

N-ch Open Drain Output (XC6108N Series)

| MARK | VOLTAGE (V) |
|------|-------------|
| K | 0.x |
| L | 1.x |
| M | 2.x |
| N | 3.x |
| P | 4.x |
| R | 5.x |

Represents decimal number of detect voltage

(ex.)

| MARK | VOLTAGE (V) | PRODUCT SERIES |
|------|-------------|----------------|
| 3 | x.3 | XC6108xx3xxx |
| 0 | x.0 | XC6108xx0xxx |

Represents options

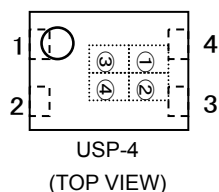| MARK | OPTIONS | PRODUCT SERIES |
|------|---------|----------------|
| A | Built-in delay capacitance pin with hysteresis 5% (TYP.) (Standard) | XC6108xxxAxx |
| B | Built-in delay capacitance pin with hysteresis less than 1% (Standard) | XC6108xxxBxx |
| C | No built-in delay capacitance pin with hysteresis 5% (TYP.) (Semi-custom) | XC6108xxxCxx |
| D | No built-in delay capacitance pin with hysteresis less than 1% (Semi-custom) | XC6108xxxDxx |

Represents production lot number

0 to 9, A to Z or inverted characters of 0 to 9, A to Z repeated.

(G, I, J, O, Q, W excepted.)

# MARKING RULE (Continued)

USP-4



USP-4
(TOP VIEW)

Represents output configuration and integer number of detect voltage

CMOS Output (XC6108C Series)

| MARK | VOLTAGE (V) |
|------|-------------|
| A | 0.x |
| B | 1.x |
| C | 2.x |
| D | 3.x |
| E | 4.x |
| F | 5.x |

N-ch Open Drain Output (XC6108N Series)

| MARK | VOLTAGE (V) |
|------|-------------|
| K | 0.x |
| L | 1.x |
| M | 2.x |
| N | 3.x |
| P | 4.x |
| R | 5.x |

Represents decimal number of detect voltage

(ex.)

| MARK | VOLTAGE (V) | PRODUCT SERIES |
|------|-------------|----------------|
| 3 | x.3 | XC6108xx3xxx |
| 0 | x.0 | XC6108xx0xxx |

Represents options

| MARK | OPTIONS | PRODUCT SERIES |
|------|---------|----------------|
| A | Built-in delay capacitance pin with hysteresis 5% (TYP.) (Standard) | XC6108xxxAxx |
| B | Built-in delay capacitance pin with hysteresis less than 1% (Standard) | XC6108xxxBxx |
| C | No built-in delay capacitance pin with hysteresis 5% (TYP.) (Semi-custom) | XC6108xxxCxx |
| D | No built-in delay capacitance pin with hysteresis less than 1% (Semi-custom) | XC6108xxxDxx |

Represents production lot number

0 to 9, A to Z repeated. (G, I, J, O, Q, W excepted.)

*No character inversion used.

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