1.5MHz, 600mA, High Efficiency PWM Step-Down DC/DC Converter

General Description

The RT8016L is a high-efficiency Pulse-Width-Modulated (PWM) step-down DC/DC converter capable of delivering up to 600mA output current over a wide input voltage range from 2.5V to 5.5V. The RT8016L is ideally suited for portable electronic devices that are powered from 1-cell Li-ion battery or from other power sources, such as cellular phones, PDAs and hand-held devices.

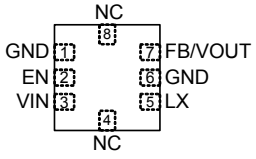
Two operating modes are available including : PWM/low dropout autoswitch mode and shut-down mode. The internal synchronous rectifier with low $R_{DS(ON)}$ dramatically reduces conduction loss at PWM mode. No external Schottky diode is required in practical application.

The RT8016L enters low dropout mode when normal PWM can not provide regulated output voltage by continuously turning on the upper P-MOSFET. The RT8016L enters Shut-down mode and consumes less than 0.1μA when the EN pin is pulled low. The RT8016L also offers a fixed output voltage with a range from 1V to 3.3V with 0.1V per step or an adjustable output voltage via two external resistors.

The switching ripple is easily smoothed out by small package filtering elements due to a fixed operating frequency of 1.5MHz. Other features include soft-start, lower internal reference voltage with 2% accuracy, over temperature protection, and over current protection. The IC is available in a WQFN-8L 1.6x1.6 (COL) package which allows small PCB area application.

Pin Configurations

(TOP VIEW)



WQFN-8L 1.6x1.6 (COL)

Features

- **Input Range : 2.5V to 5.5V**
- **Adjustable Output Voltage Range : 0.6V to V_{IN}**
- **600mA Output Current**
- **Efficiency up to 95%**
- **No Schottky Diode Required**
- **1.5MHz Fixed-Frequency PWM Operation**
- **RoHS Compliant and Halogen Free**

Applications

- Mobile Phones
- Personal Information Appliances
- Wireless and DSL Modems
- MP3 Players
- Portable Instruments

Ordering Information

RT8016L-□□□

Package Type
QW : WQFN-8L 1.6x1.6 (COL) (W-Type)

Lead Plating System
G : Green (Halogen Free and Pb Free)

Output Voltage
Default : Adjustable
10 : 1.0V
11 : 1.1V
:
32 : 3.2V
33 : 3.3V

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

BS : Product Code

W : Date Code

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Typical Application Circuit

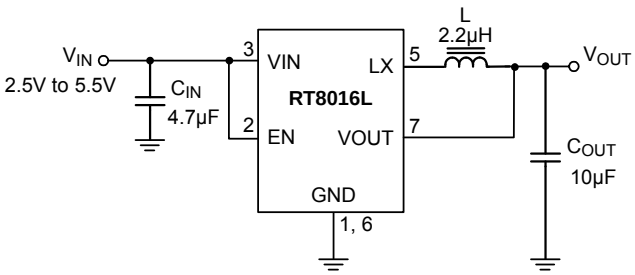
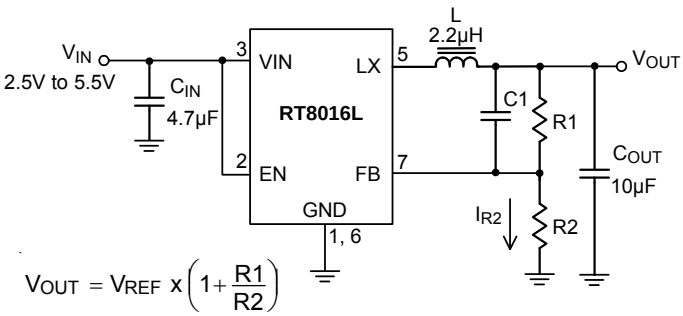


Figure 1. Fixed Voltage Regulator



$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

with R2 = 300kΩ to 60kΩ so I_{R2} = 2µA to 10µA,

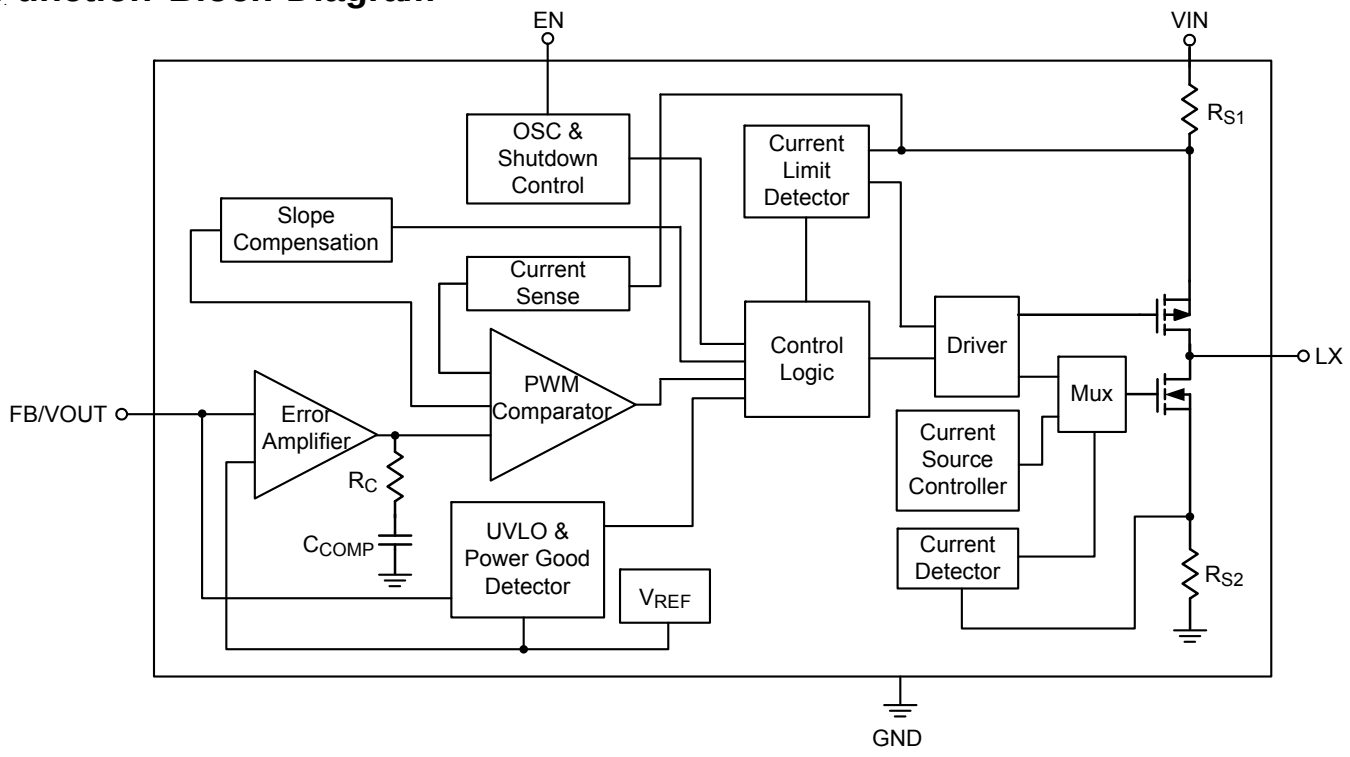
and (R1 x C1) should be in the range between $3x10^{-6}$ and $6x10^{-6}$ for component selection.

Figure 2. Adjustable Voltage Regulator

Functional Pin Description

Pin No.	Pin Name	Pin Function
1, 6	GND	Ground Pin.
2	EN	Chip Enable (Active High).
3	VIN	Power Input Pin
4, 8	NC	No Internal Connection.
5	LX	Switching Pin for Step-down Converter
7	FB/VOUT	Feedback/Output Voltage Pin.

Function Block Diagram



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Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, V_{IN} ---------- 6.5V
- EN, FB Pin Voltage ---------- –0.3V to V_{IN}
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-8L 1.6x1.6 (COL) ---------- 0.833W
- Package Thermal Resistance (Note 2)
  WQFN-8L 1.6x1.6 (COL), θ_{JA} ---------- 120°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- Junction Temperature ---------- 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, V_{IN} ---------- 2.5V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 3.6V, V_{OUT} = 2.5V, V_{REF} = 0.6V, L = 2.2µH, C_{IN} = 4.7µF, C_{OUT} = 10µF, T_A = 25°C, I_{MAX} = 600mA unless otherwise specified)

Parameter		Symbol	Test Conditions		Min	Typ	Max	Unit
Quiescent Current		I_Q	I_{OUT} = 0mA, V_{FB} = V_{REF} + 5%		--	50	70	µA
Shutdown Current		I_{SHDN}	EN = GND		--	0.1	1	µA
Reference Voltage		V_{REF}	For Adjustable Output Voltage		0.588	0.6	0.612	V
Adjustable Output Range		V_{OUT}	(Note 6)		V_{REF}	--	V_{IN} – 0.2V	V
Output Voltage Accuracy	Fixed	ΔV_{OUT}	V_{IN} = (V_{OUT} + ΔV) to 5.5V or V_{IN} > 2.5V whichever is larger. (Note 5)		–3	--	3	%
	Adjustable	ΔV_{OUT}	V_{IN} = V_{OUT} + ΔV to 5.5V (Note 5) 0A < I_{OUT} < 600mA		–3	--	3	%
FB Input Current		I_{FB}	V_{FB} = V_{IN}		–50	--	50	nA
P-MOSFET R_{ON}		$R_{DS(ON)\_P}$	I_{OUT} = 200mA	V_{IN} = 3.6V	--	0.28	--	Ω
				V_{IN} = 2.5V	--	0.38	--	
N-MOSFET R_{ON}		$R_{DS(ON)\_N}$	I_{OUT} = 200mA	V_{IN} = 3.6V	--	0.25	--	Ω
				V_{IN} = 2.5V	--	0.35	--	
P-Channel Current Limit		I_{LIM_P}	V_{IN} = 2.5V to 5.5 V		0.9	1.5	2.1	A
EN Input Voltage	Logic High	V_{EN_H}			1.5	--	V_{IN}	V
	Logic Low	V_{EN_L}			--	--	0.4	V
UVLO Threshold		V_{UVLO}			--	1.8	--	V
UVLO Hysteresis		ΔV_{UVLO}			--	0.1	--	V

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Oscillator Frequency	f_{OSC}	V_{IN} = 3.6V, I_{OUT} = 100mA	1.2	1.5	1.8	MHz
Thermal Shutdown Temperature	T_{SD}		--	160	--	°C
Maximum Duty Cycle	D_{MAX}		100	--	--	%
LX Current Source		V_{IN} = 3.6V, V_{LX} = 0V or V_{LX} = 3.6V	1	--	100	μA

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective thermal conductivity four-layer test board of JEDEC 51-7 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. $\Delta V = I_{OUT} \times P_{RDS(ON)}$

Note 6. Guarantee by design.

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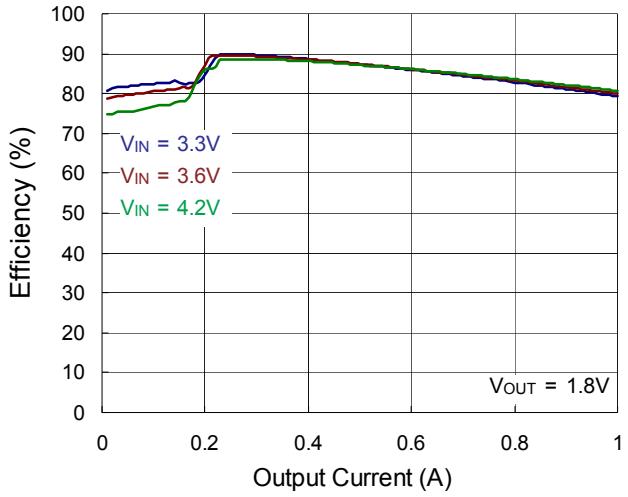
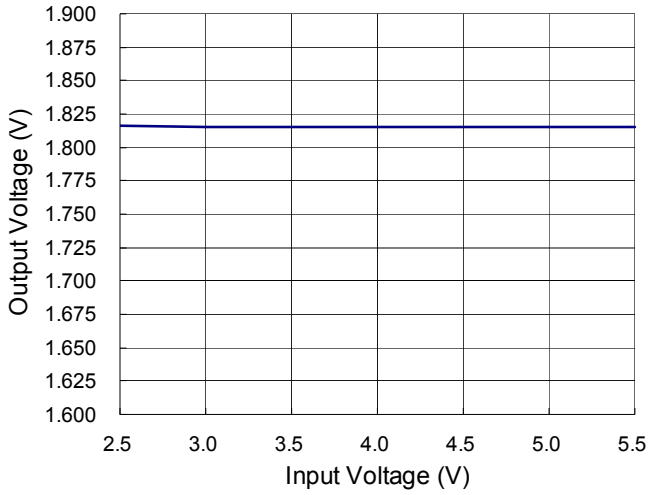
Typical Operating Characteristics

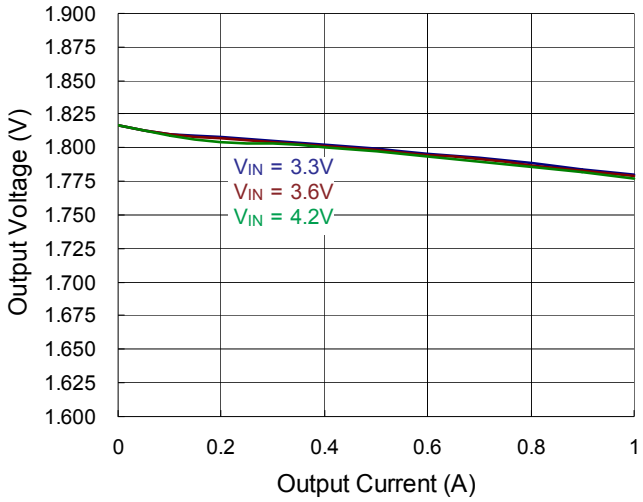
Efficiency vs. Output Current



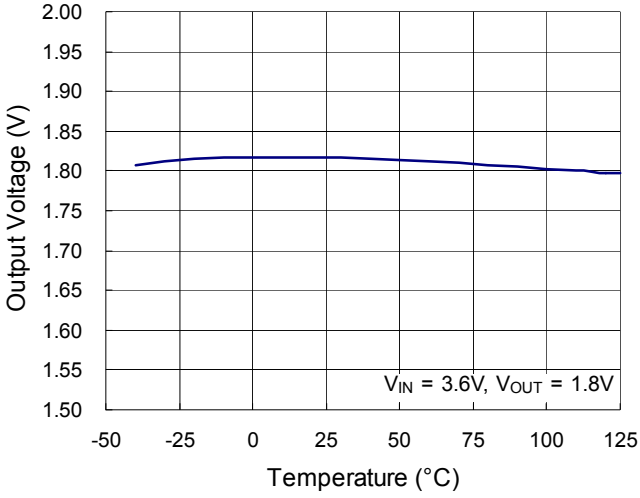
Output Voltage vs. Input Voltage



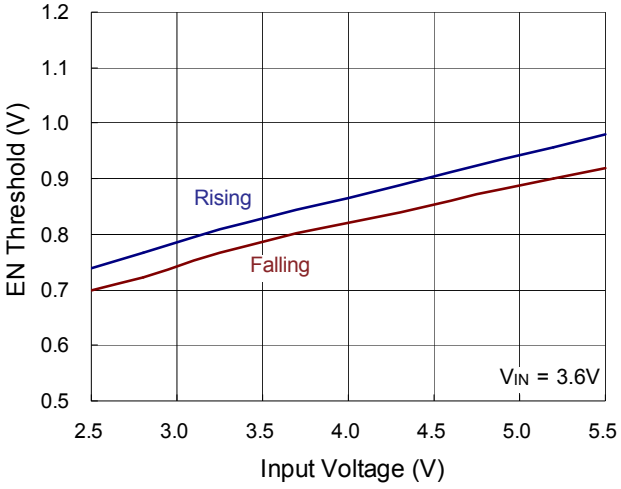
Output Voltage vs. Output Current



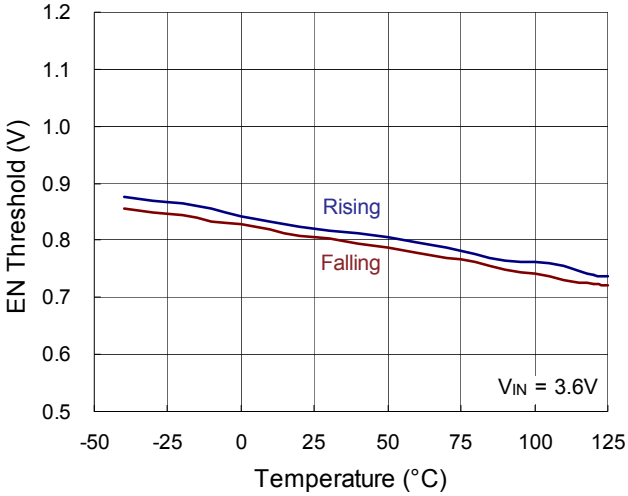
Output Voltage vs. Temperature



EN Threshold vs. Input Voltage



EN Threshold vs. Temperature



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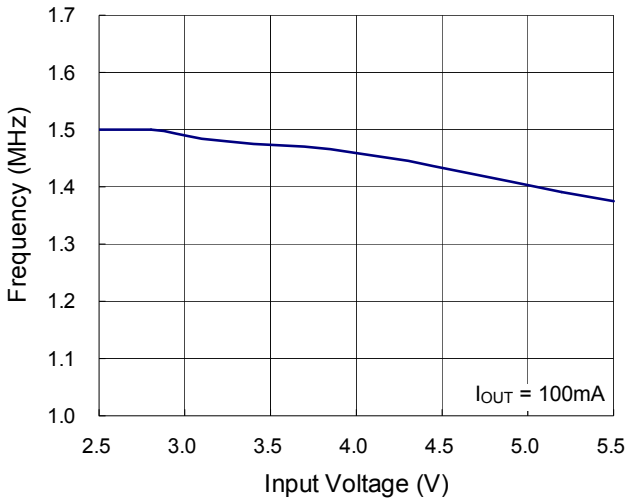
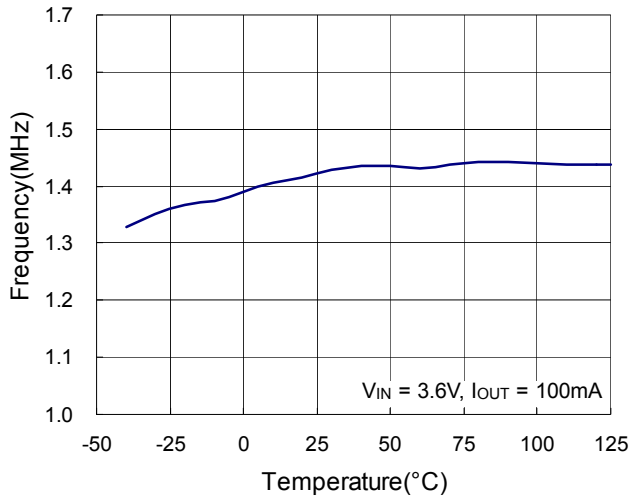
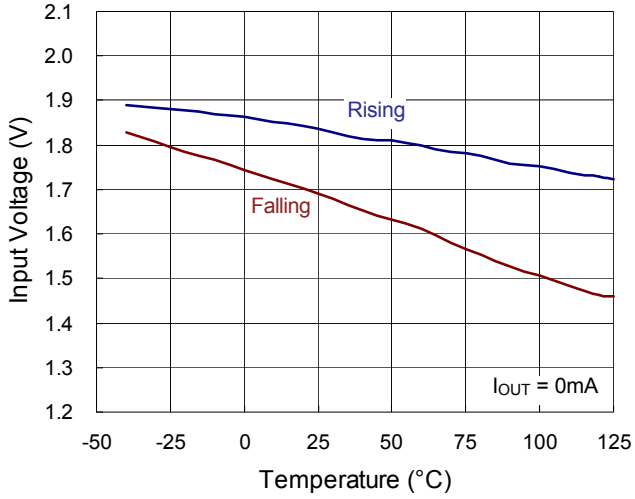
Frequency vs. Input Voltage



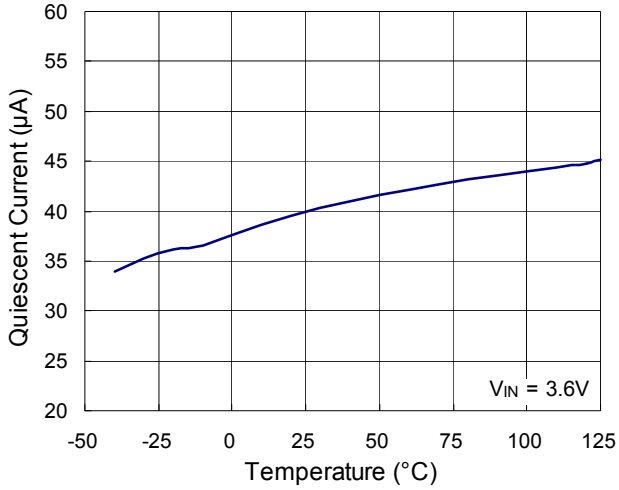
Frequency vs. Temperature



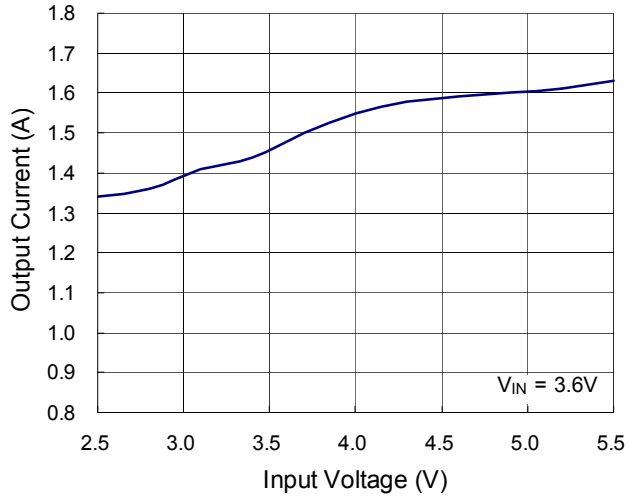
Input Voltage threshold vs. Temperature



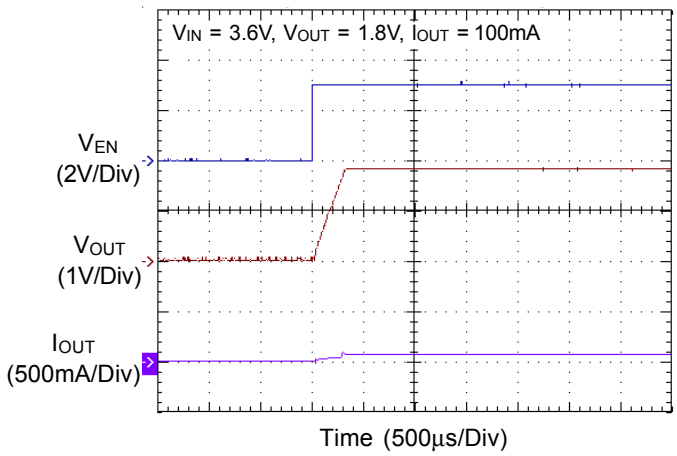
Quiescent Current vs. Temperature



Current Limit vs. Input Voltage



Power On from EN



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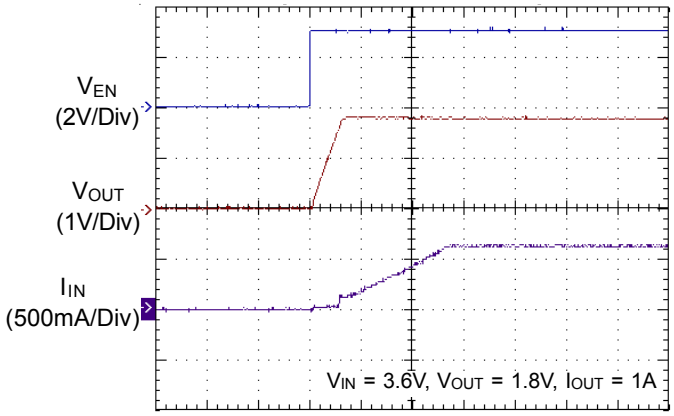
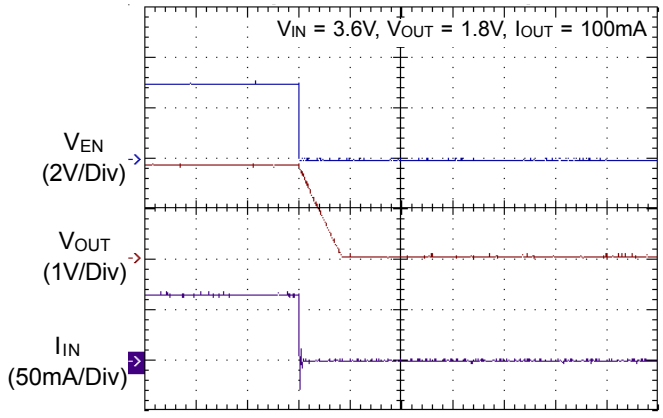
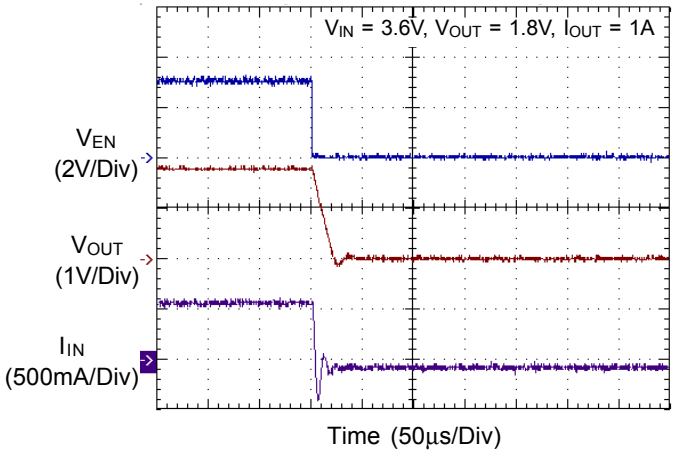
Power On from EN



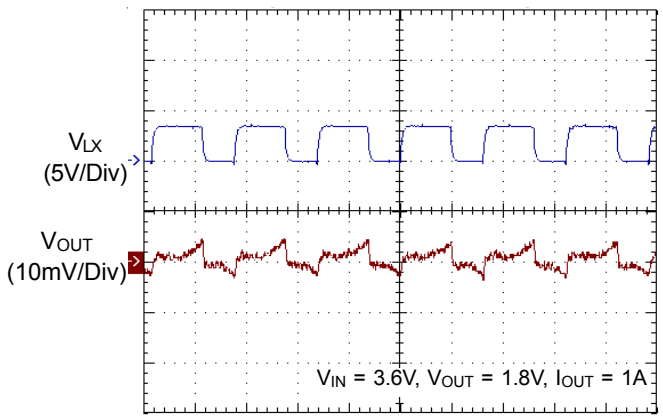
Power Off from EN



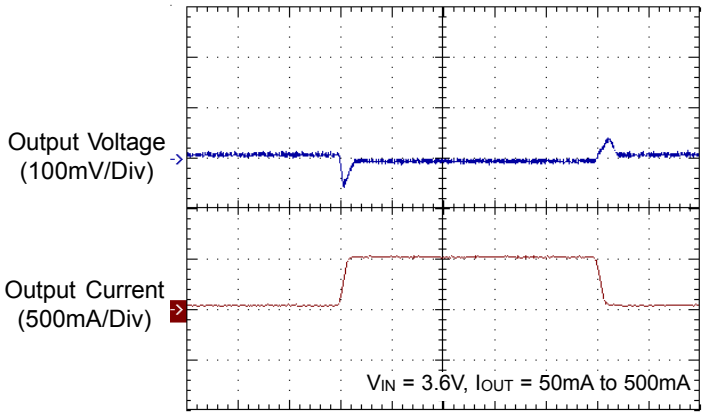
Power Off from EN



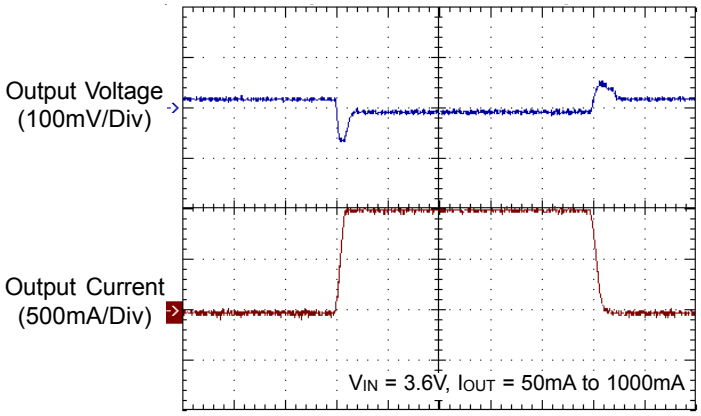
Output Ripple Voltage



Load Transient Response



Load Transient Response



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Application Information

The basic RT8016L application circuit is shown in Typical Application Circuit. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency followed by C_{IN} and C_{OUT}.

Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the ripple current. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance:

$$\Delta I_L = \left[\frac{V_{OUT}}{F \times L}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

Having a lower ripple current reduces the ESR losses in the output capacitors and the output voltage ripple. Highest efficiency operation is achieved at low frequency with small ripple current. This, however, requires a large inductor. A reasonable starting point for selecting the ripple current is $\Delta I_L = 0.4(I_{MAX})$. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

Inductor Core Selection

Once the value for L is known, the type of inductor can be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite or mollypermalloy cores. Actual core loss is independent of core size for a fixed inductor value but it is very dependent on the inductance selected. As the inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase. Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard", which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Different core materials and shapes will change the size/ current and price/current relationship of an inductor.

Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate energy but generally cost more than powdered iron core inductors with similar

characteristics. The choice of which style inductor to use mainly depends on the price vs. size requirements and any radiated field/EMI requirements.

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low ESR input capacitor sized for the maximum RMS current should be used. RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where IRMS = $I_{OUT}/2$. This simple worst case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

The selection of C_{OUT} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients, as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section.

The output ripple, ΔV_{OUT}, is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8fC_{OUT}}\right]$$

The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are

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all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR but can be used in cost sensitive applications provided that consideration is given to ripple current ratings and long term reliability. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

Output Voltage Programming

The resistive voltage divider allows the FB pin to sense a fraction of the output voltage as shown in Figure 3.

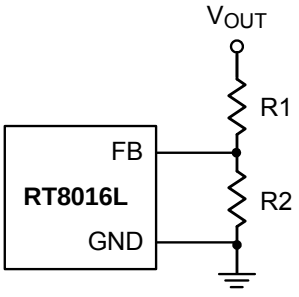

Figure 3. Setting the Output Voltage

For adjustable voltage mode, the output voltage is set by an external resistive voltage divider according to the following equation :

$$V_{OUT} = V_{REF}(1+\frac{R1}{R2})$$

where VREF is the internal reference voltage (0.6V typ.)

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as :

Efficiency = 100% – (L1+ L2+ L3+ ...)

where L1, L2, etc. are the individual losses as a percentage of input power. Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses : V_{IN} quiescent current and I^2R losses.

The V_{IN} quiescent current loss dominates the efficiency loss at very low load currents whereas the I^2R loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of no consequence.

1. The VIN quiescent current appears due to two factors including : the DC bias current as given in the electrical characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge ΔQ moves from VIN to ground. The resulting $\Delta Q/\Delta t$ is the current out of VIN that is typically larger than the DC bias current. In continuous mode,

$I_{GATECHG} = f(Q_T+Q_B)$

where Q_T and Q_B are the gate charges of the internal top and bottom switches. Both the DC bias and gate charge losses are proportional to V_{IN} and thus their effects will be more pronounced at higher supply voltages.

2. I^2R losses are calculated from the resistances of the internal switches, R_{SW} and external inductor R_L. In continuous mode, the average output current flowing through inductor L is "chopped" between the main switch and the synchronous switch. Thus, the series resistance

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looking into the LX pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows :

$R_{SW} = R_{DS(ON)TOP \times DC} + R_{DS(ON)BOT} \times (1-DC)$

The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Operating Characteristics curves. Thus, to obtain I^2R losses, simply add R_{SW} to R_L and multiply the result by the square of the average output current.

Other losses including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses generally account for less than 2% of the total loss.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to ΔI_{LOAD} (ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing which would indicate a stability problem.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications of the RT8016L, the maximum junction temperature is 125°C and T_A is the ambient temperature. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WQFN-8L 1.6x1.6 (COL) packages, the thermal resistance, θ_{JA}, is 120°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula:

$P_{D(MAX)}$ = (125°C – 25°C) / (120°C/W) = 0.833W for WQFN-8L 1.6x1.6 (COL) package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. For the RT8016L package, the derating curve in Figure 4 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

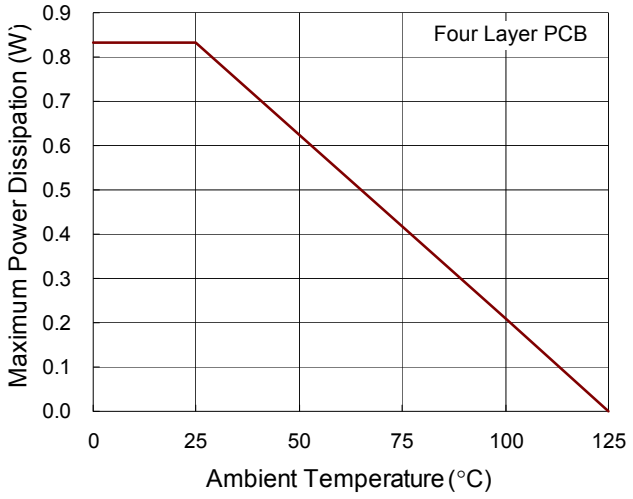

Figure 4

Layout Considerations

Follow the PCB layout guidelines for optimal performance of the RT8016L.

- For the main current paths, keep their traces short and wide.
- Put the input capacitor as close as possible to the device pins (VIN and GND).
- LX node is with high frequency voltage swing and should be kept in a small area. Keep analog components away from LX node to prevent stray capacitive noise pick-up.
- Connect feedback network behind the output capacitors. Keep the loop area small. Place the feedback components near the RT8016L.
- Connect all analog grounds to a common node and then connect the common node to the power ground behind the output capacitors.

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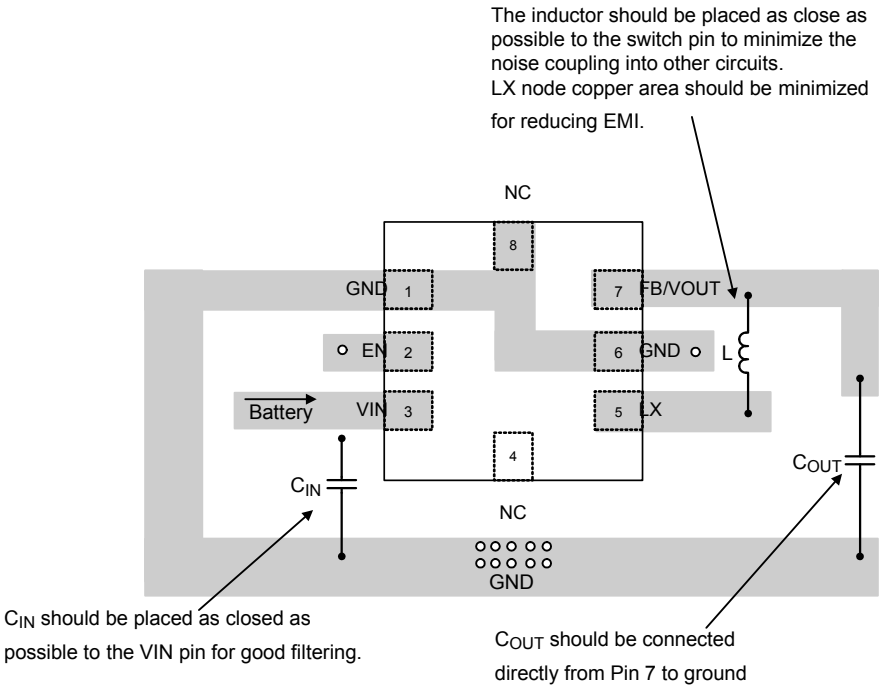

Figure 5. Fixed Voltage Regulator layout guide

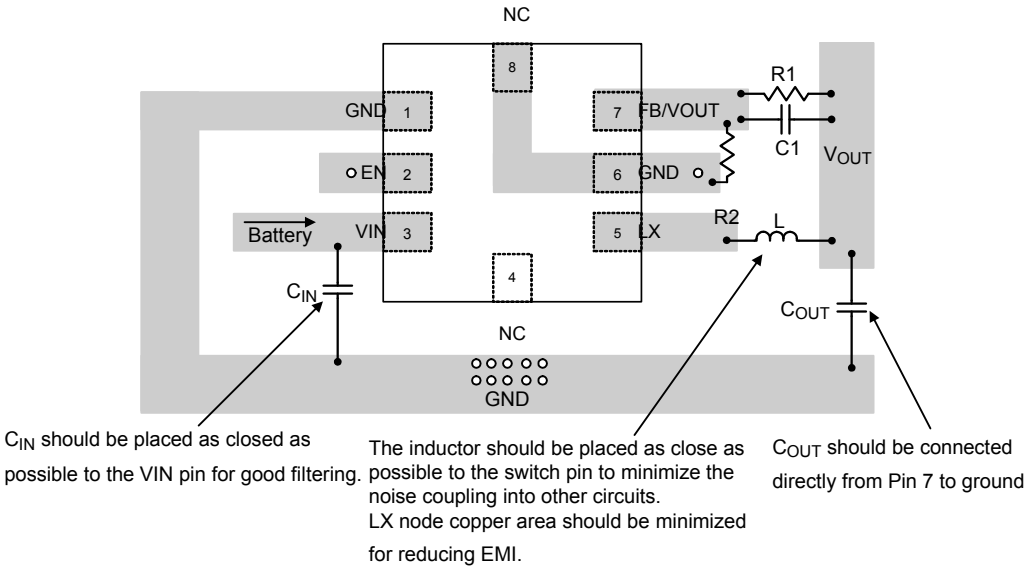

Figure 6. Adjustable Voltage Regulator layout guide

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Table 1. Recommended Inductors

Supplier	Inductance (μH)	Current Rating (mA)	DCR (mΩ)	Dimensions(mm)	Series
TAIYO YUDEN	2.2	1480	60	3.00 x 3.00 x 1.50	NR3015
GOTREND	2.2	1500	58	3.85 x 3.85 x 1.80	GTSD32
Sumida	2.2	1500	75	4.50 x 3.20 x 1.55	CDRH2D14
Sumida	4.7	1000	135	4.50 x 3.20 x 1.55	CDRH2D14
TAIYO YUDEN	4.7	1020	120	3.00 x 3.00 x 1.50	NR3015
GOTREND	4.7	1100	146	3.85 x 3.85 x 1.80	GTSD32

Table 2. Recommened Capacitors for C_{IN} and C_{OUT}

Supplier	Capacitance (μF)	Package	Part Number
TDK	4.7	0603	C1608JB0J475M
MURATA	4.7	0603	GRM188R60J475KE19
TAIYO YUDEN	4.7	0603	JMK107BJ475RA
TAIYO YUDEN	10	0603	JMK107BJ106MA
TDK	10	0805	C2012JB0J106M
MURATA	10	0805	GRM219R60J106ME19
MURATA	10	0805	GRM219R60J106KE19
TAIYO YUDEN	10	0805	JMK212BJ106RD

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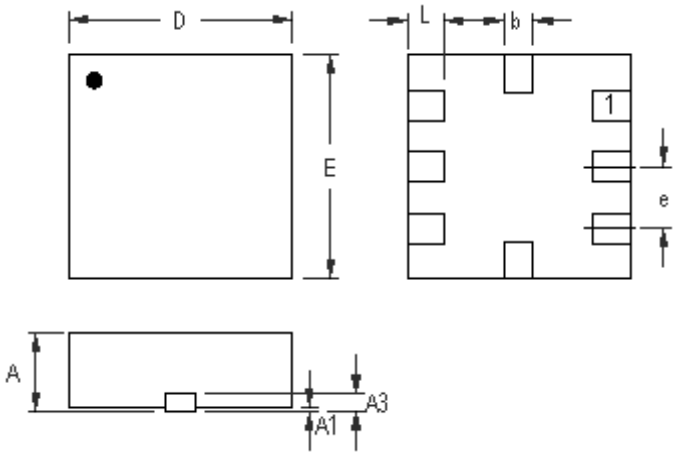
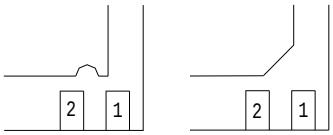
Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	1.550	1.650	0.061	0.065
E	1.550	1.650	0.061	0.065
e	0.400		0.016	
L	0.350	0.450	0.014	0.018

W-Type 8L QFN 1.6x1.6 (COL) Package

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