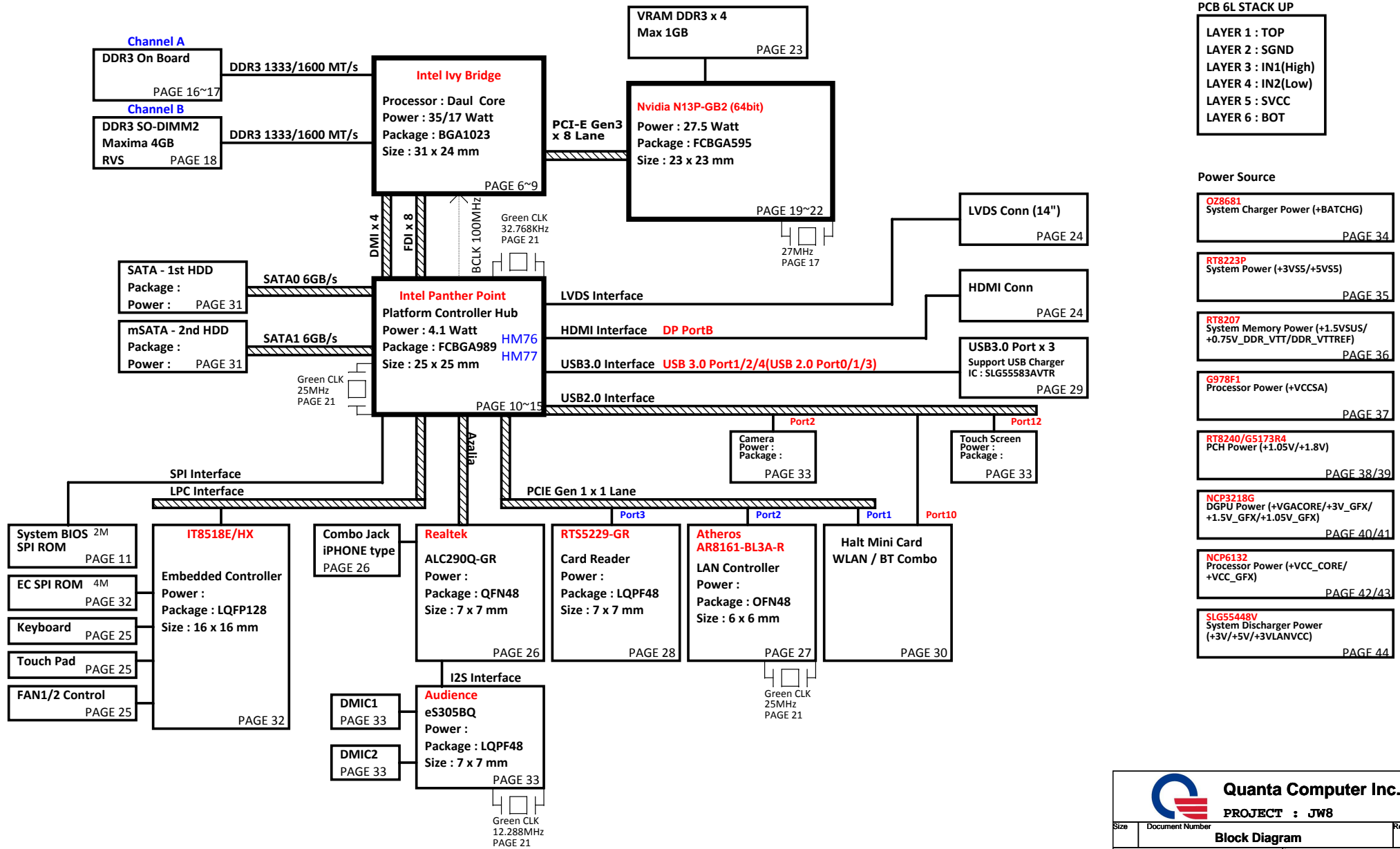
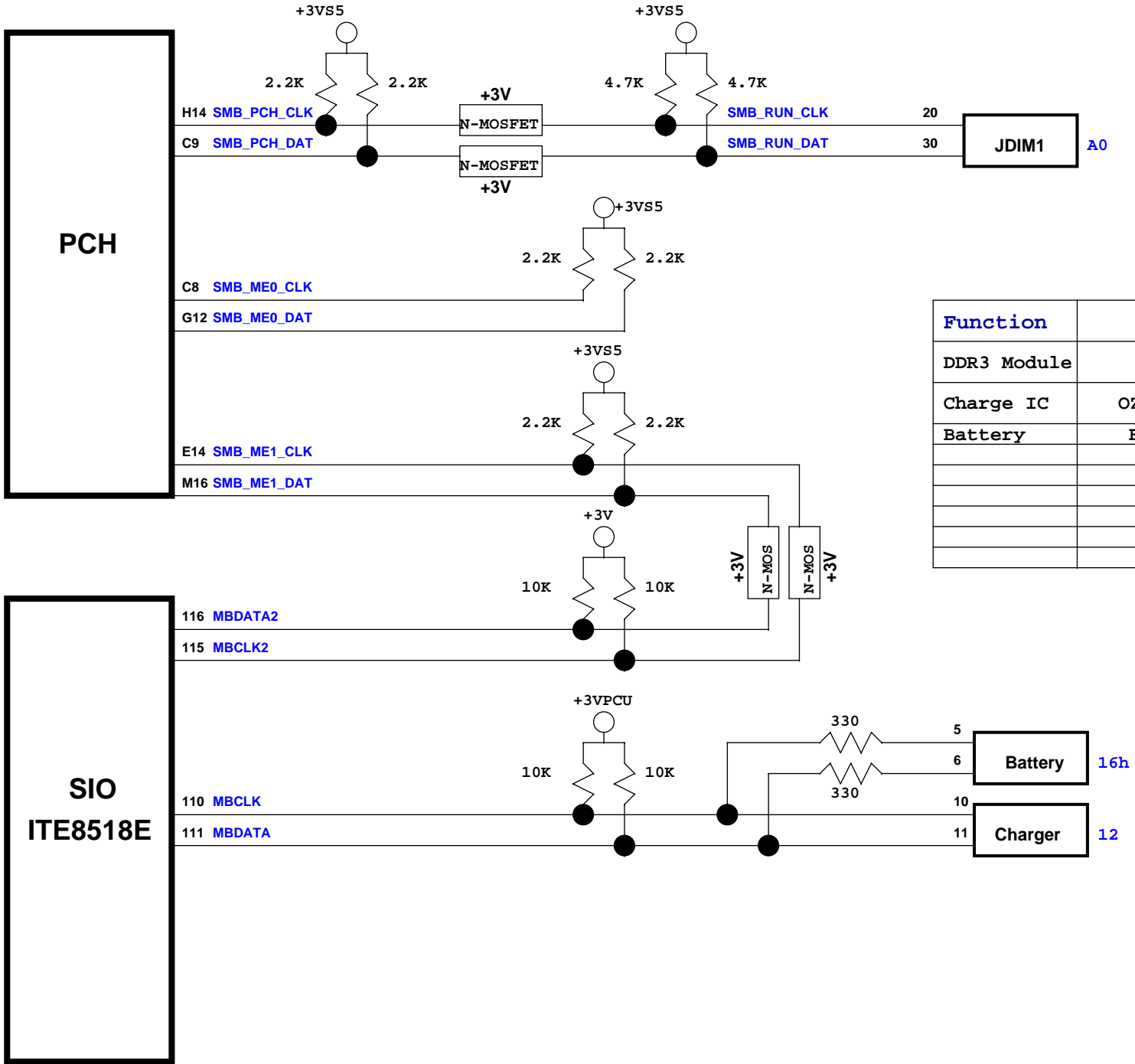


JW8 DIS (14") Super Ultra Intel Chief River Platform Block Diagram





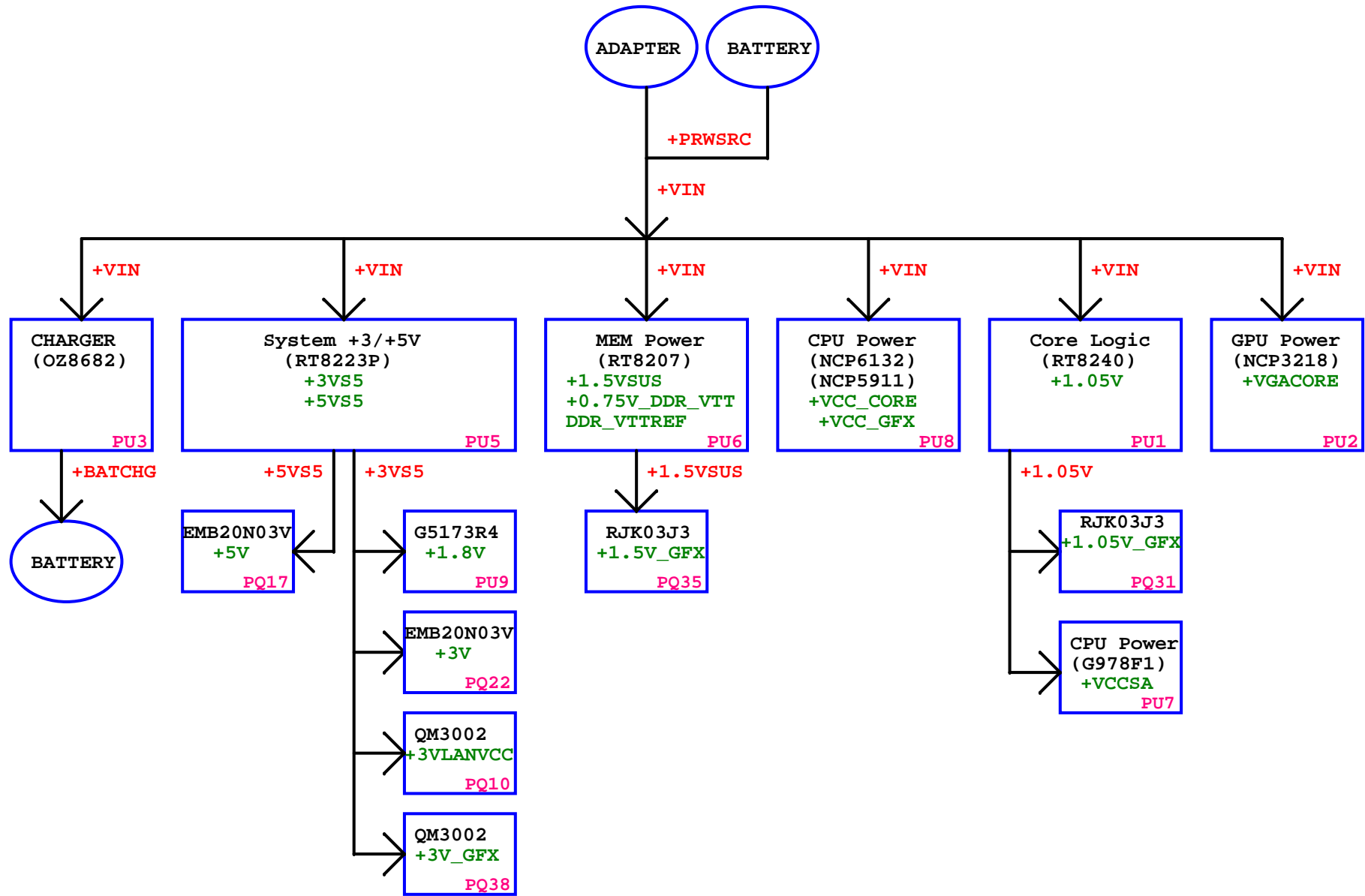
Function	IC	SMBus Address
DDR3 Module	JDIM1	A0h
Charge IC	OZ8681NL	0b0001001x (0x12h)
Battery	Battery	16h

USB Master	Port Assignment
USB0	External port#1 (USB3.0)
USB1	External port#2 (USB3.0)
USB2	Camera
USB3	External port#3 (USB3.0)
USB4	NC
USB5	NC
USB6	NC
USB7	NC
USB8	NC
USB9	Debug
USB10	WLAN
USB11	NC
USB12	Touch Screen
USB13	NC

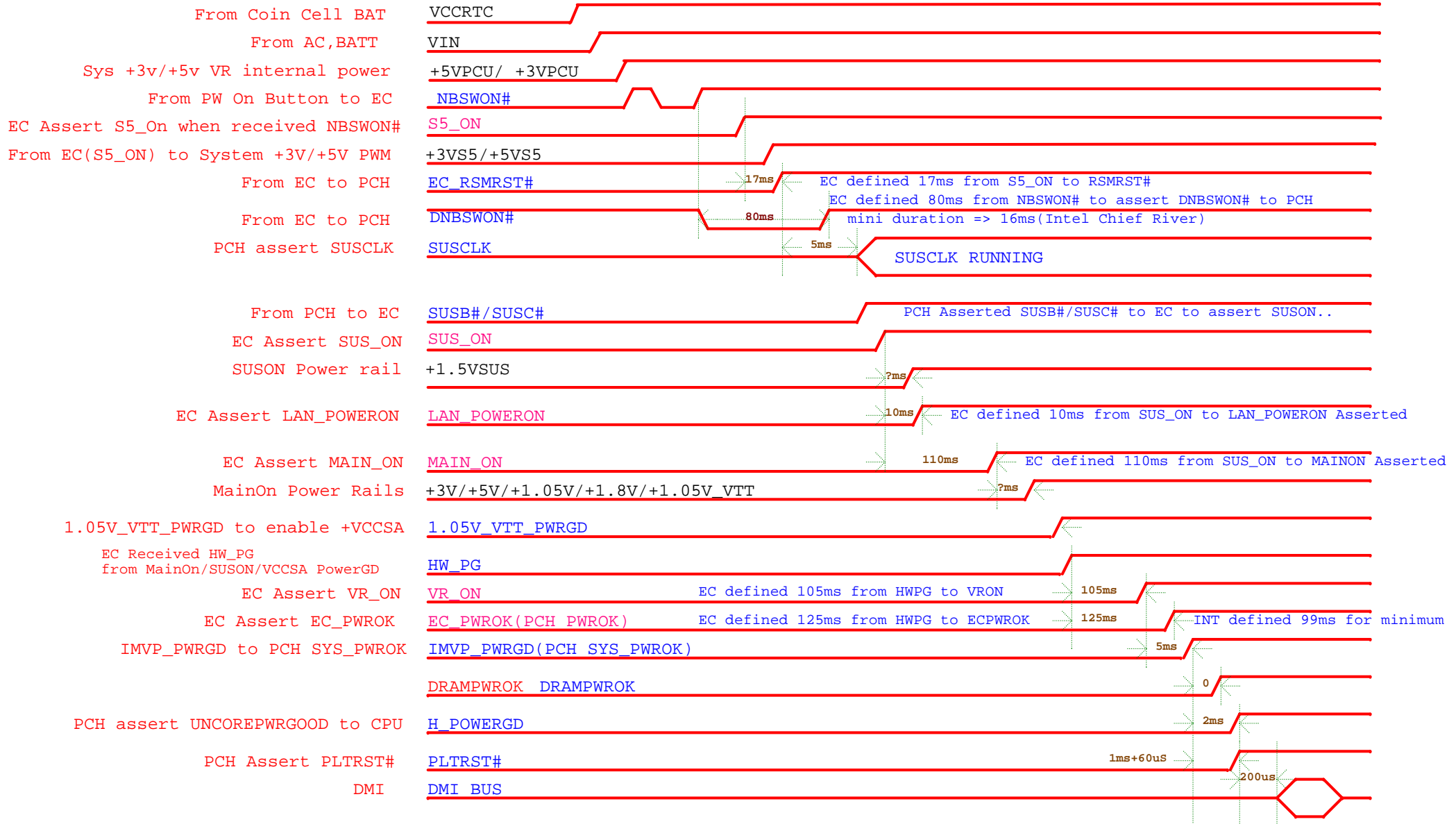
SATA Master	Port Assignment
SATA0	HDD
SATA1	mSATA
SATA2	NC
SATA3	NC
SATA4	NC
SATA5	NC

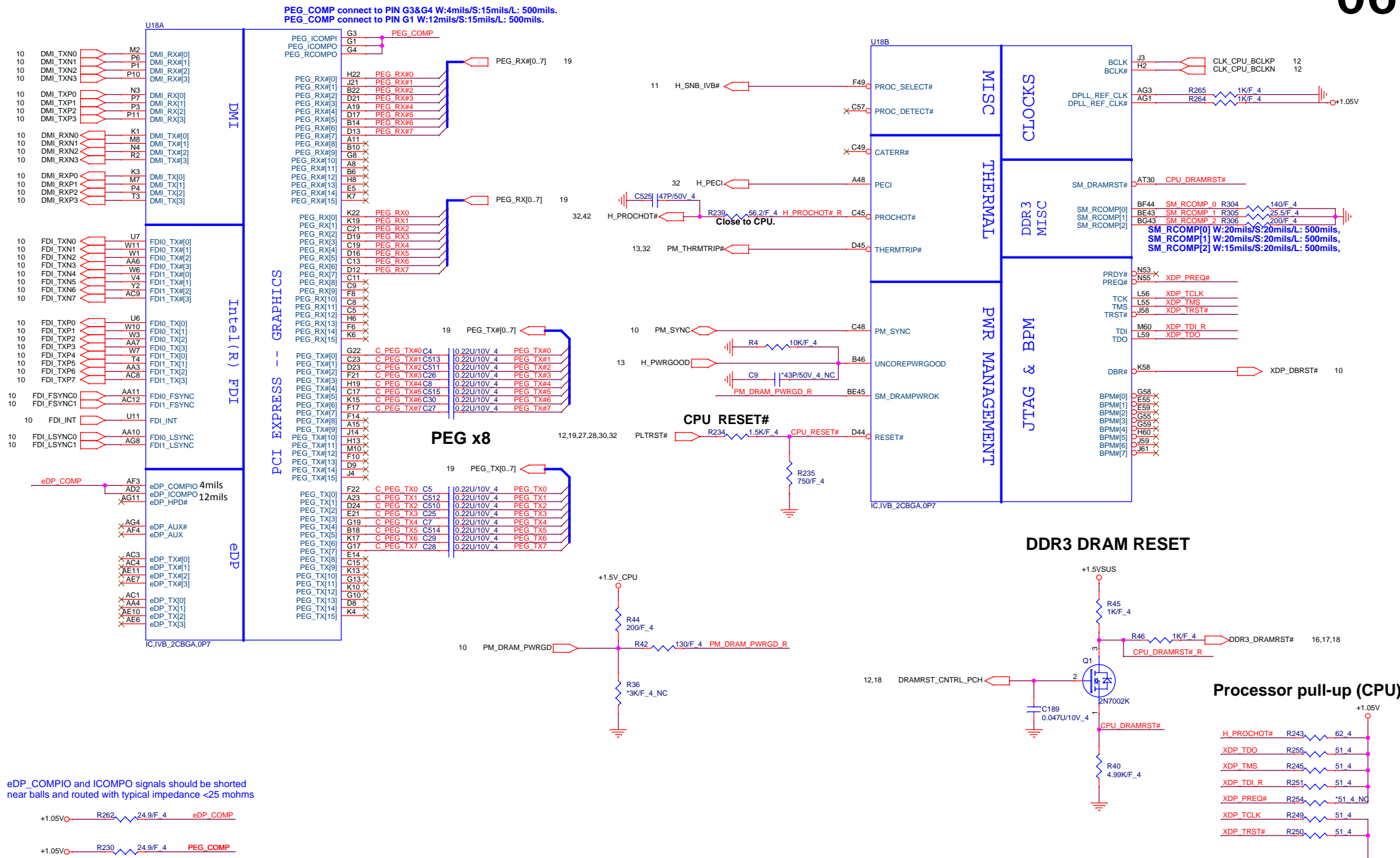
PCIE Master	Port Assignment
PCIE 1	WLAN
PCIE 2	LAN
PCIE 3	Card reader
PCIE 4	NC
PCIE 5	NC
PCIE 6	NC
PCIE 7	NC
PCIE 8	NC

Main Power tree

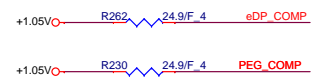


Chief River mainly Power On Sequence(G3 to S0)





eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

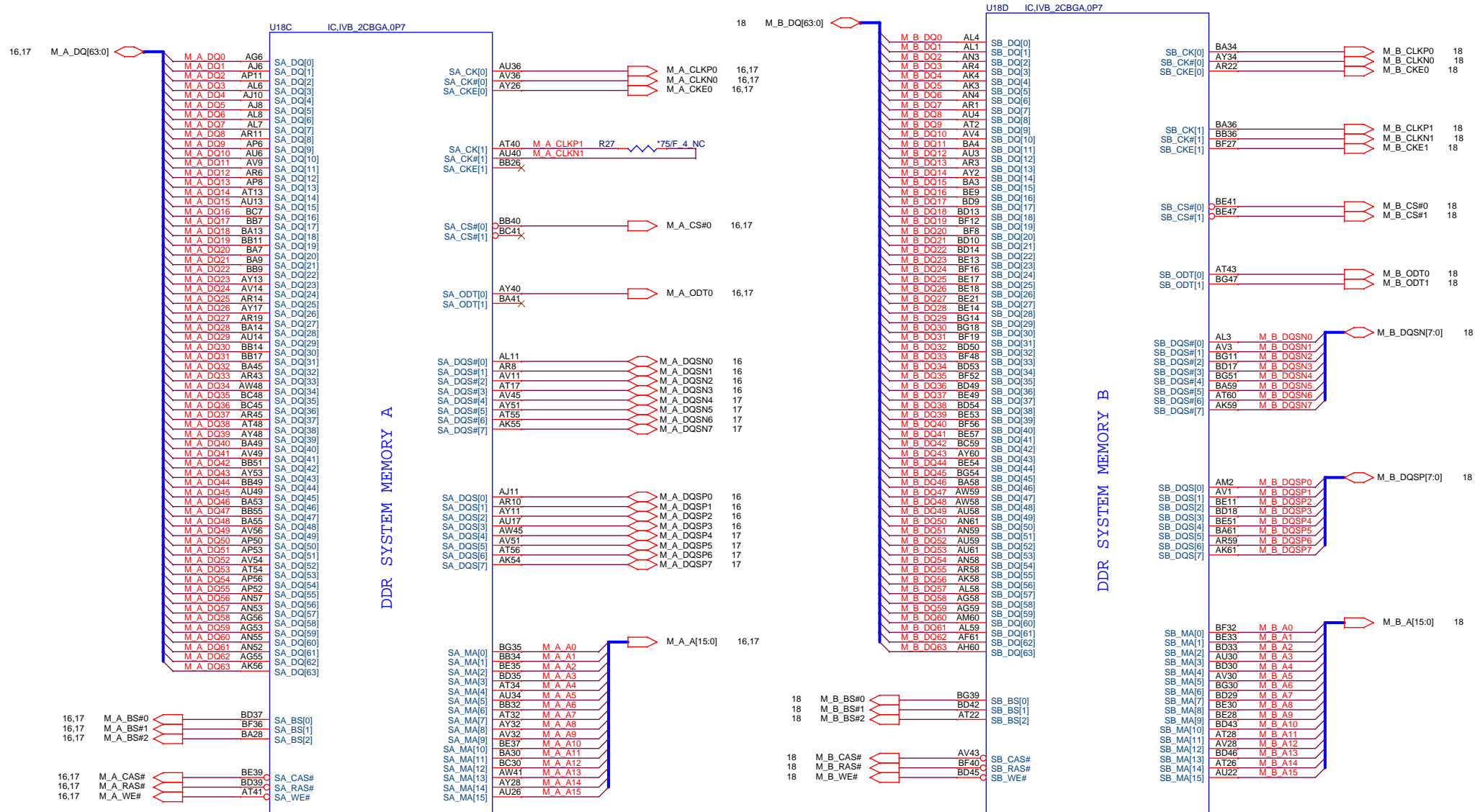


Quanta Computer Inc.
PROJECT : JW8

Size	Document Number	Rev
	Processor 1/4 (Host/GPU)	3A
Date:	Friday, November 02, 2012	Sheet 06 of 46

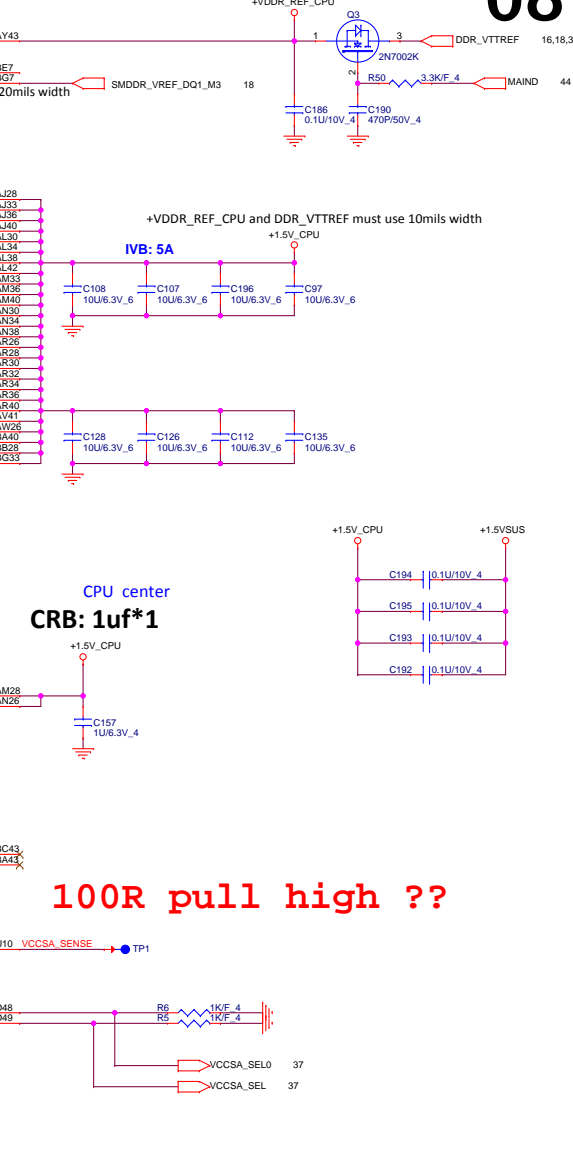
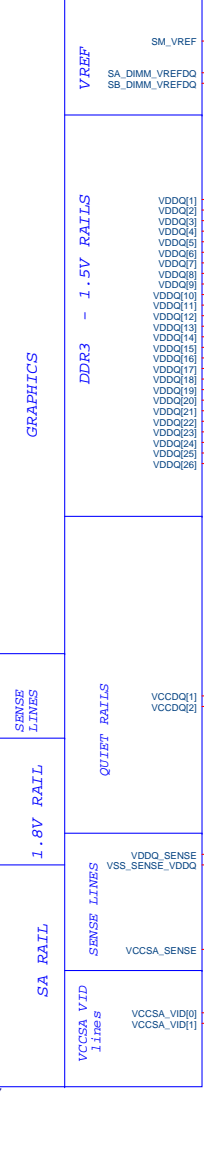
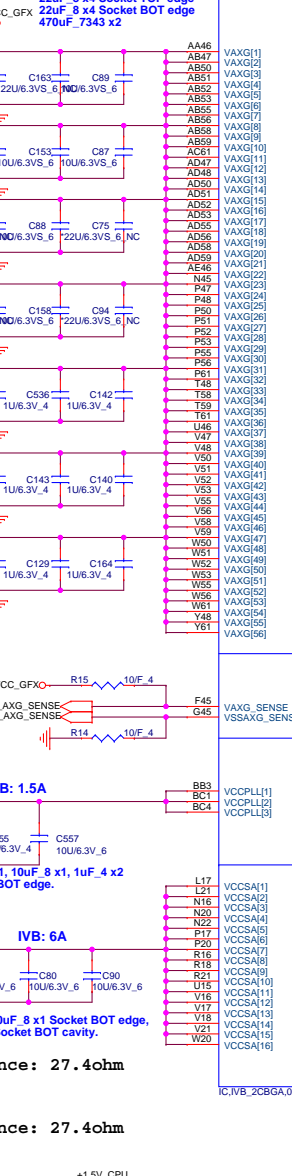
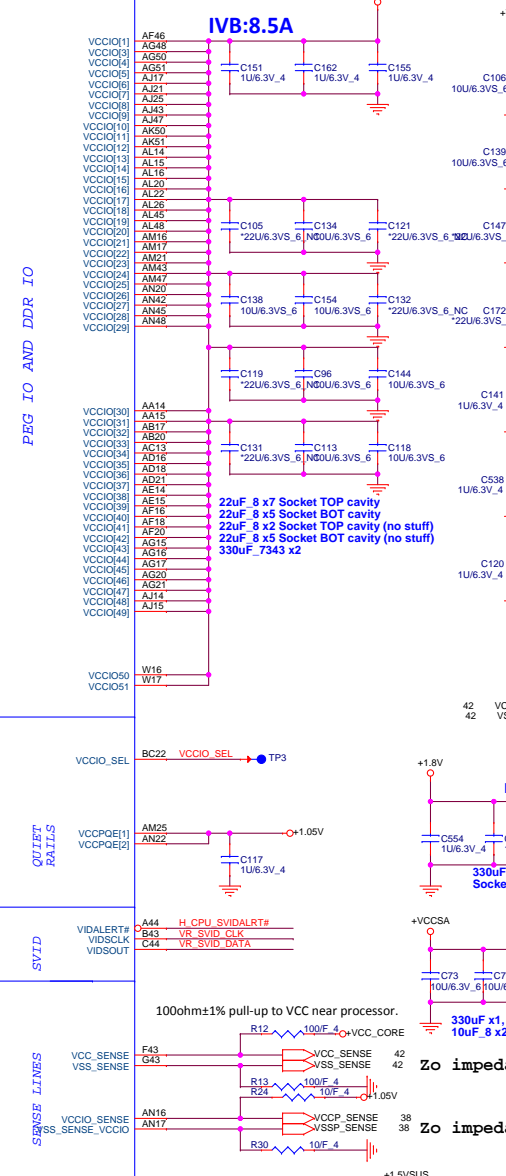
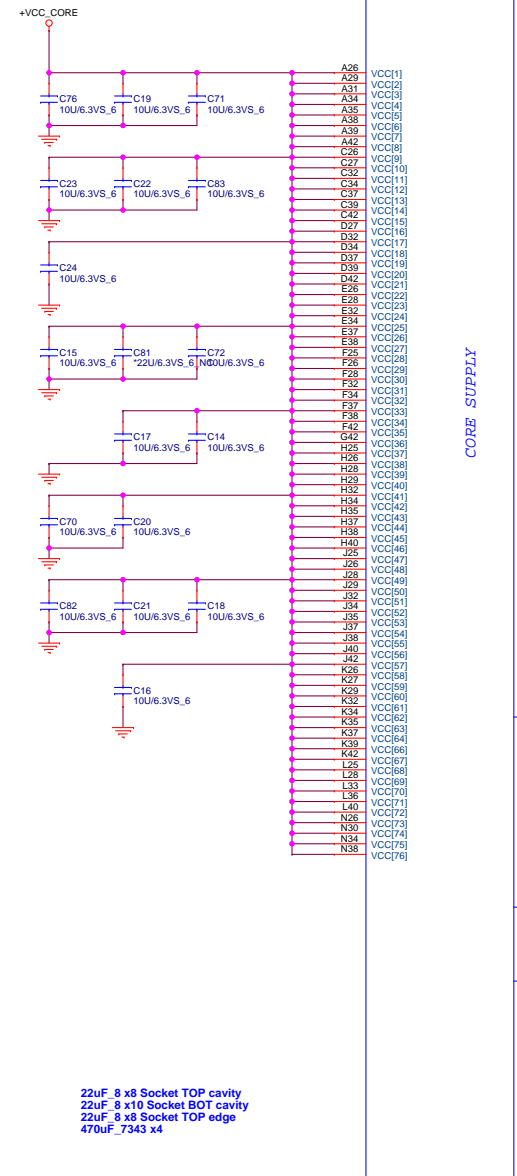
Ivy Bridge Processor (DDR3)

07



POWER

POWER



22uF 8 x8 Socket TOP cavity
 22uF 8 x10 Socket BOT cavity
 22uF 8 x8 Socket TOP edge
 470uF_7343 x4

22uF 8 x7 Socket TOP cavity
 22uF 8 x5 Socket BOT cavity
 22uF 8 x2 Socket TOP cavity (no stuff)
 22uF 8 x5 Socket BOT cavity (no stuff)
 330uF_7343 x2

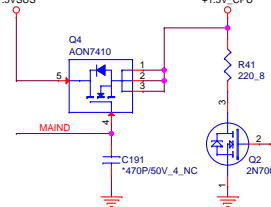
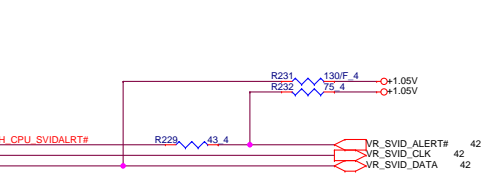
100ohm±1% pull-up to VCC near processor.
 Zo impedance: 27.4ohm

Zo impedance: 27.4ohm

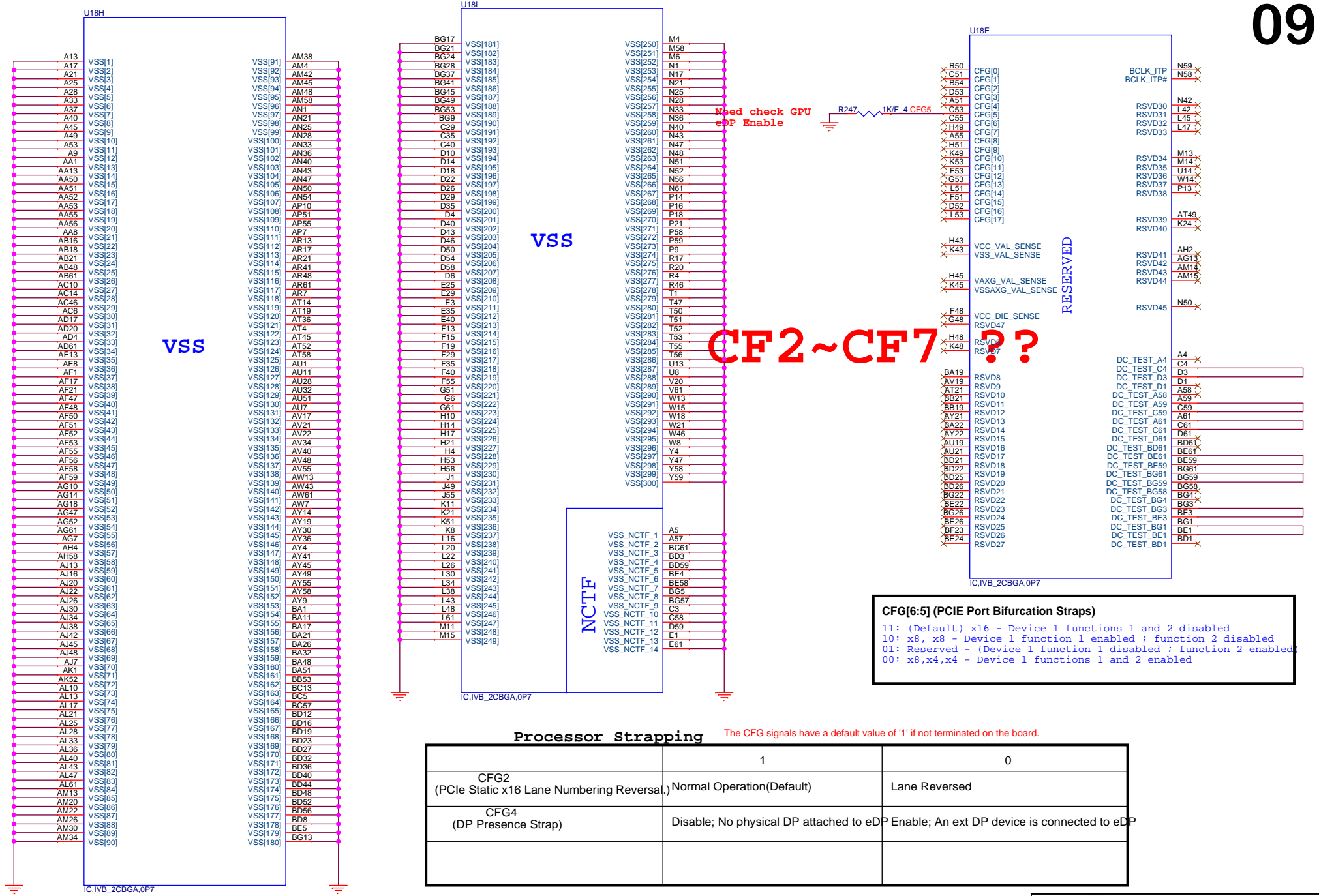
IC:IBV_2C8GA.0P7

IC:IBV_2C8GA.0P7

CPU VDDQ



Quanta Computer Inc.
 PROJECT : JW8
 Processor 3/4 (POWER)
 Date: Friday, November 02, 2012 Sheet 08 of 46



CF2~CF7??

Need check GPU eDP Enable

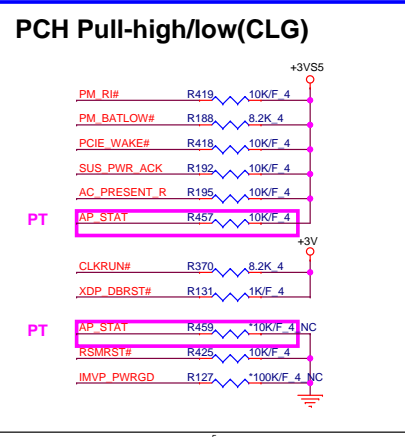
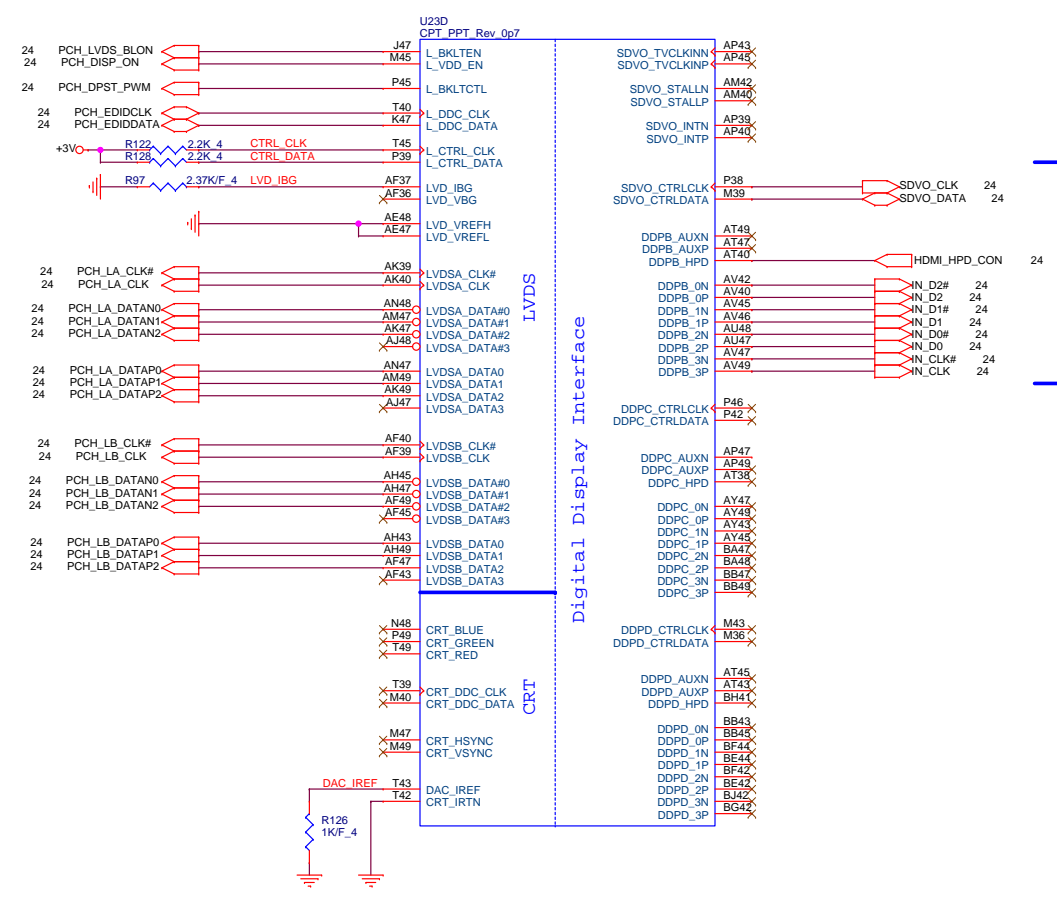
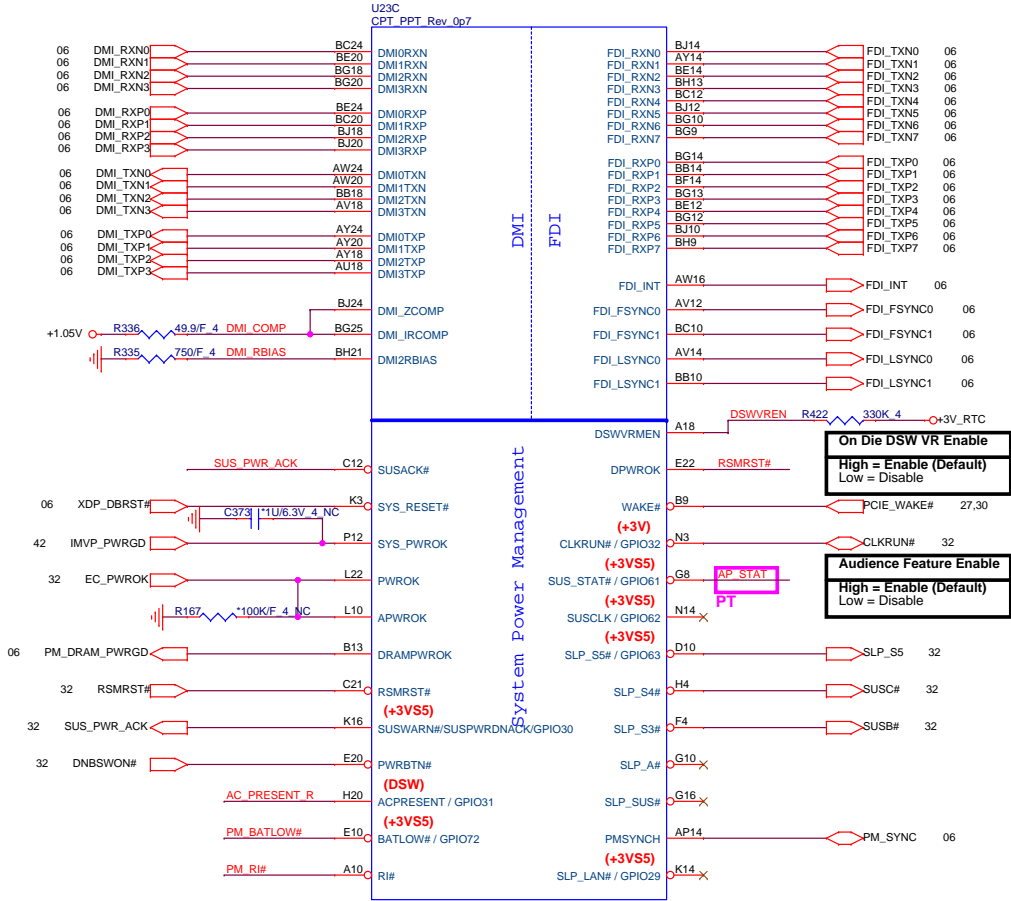
CFG[6:5] (PCIe Port Bifurcation Straps)
 11: (Default) x16 - Device 1 functions 1 and 2 disabled
 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Processor Strapping The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PCIe Static x16 Lane Numbering Reversal)	Normal Operation(Default)	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP Enable; An ext DP device is connected to eDP	

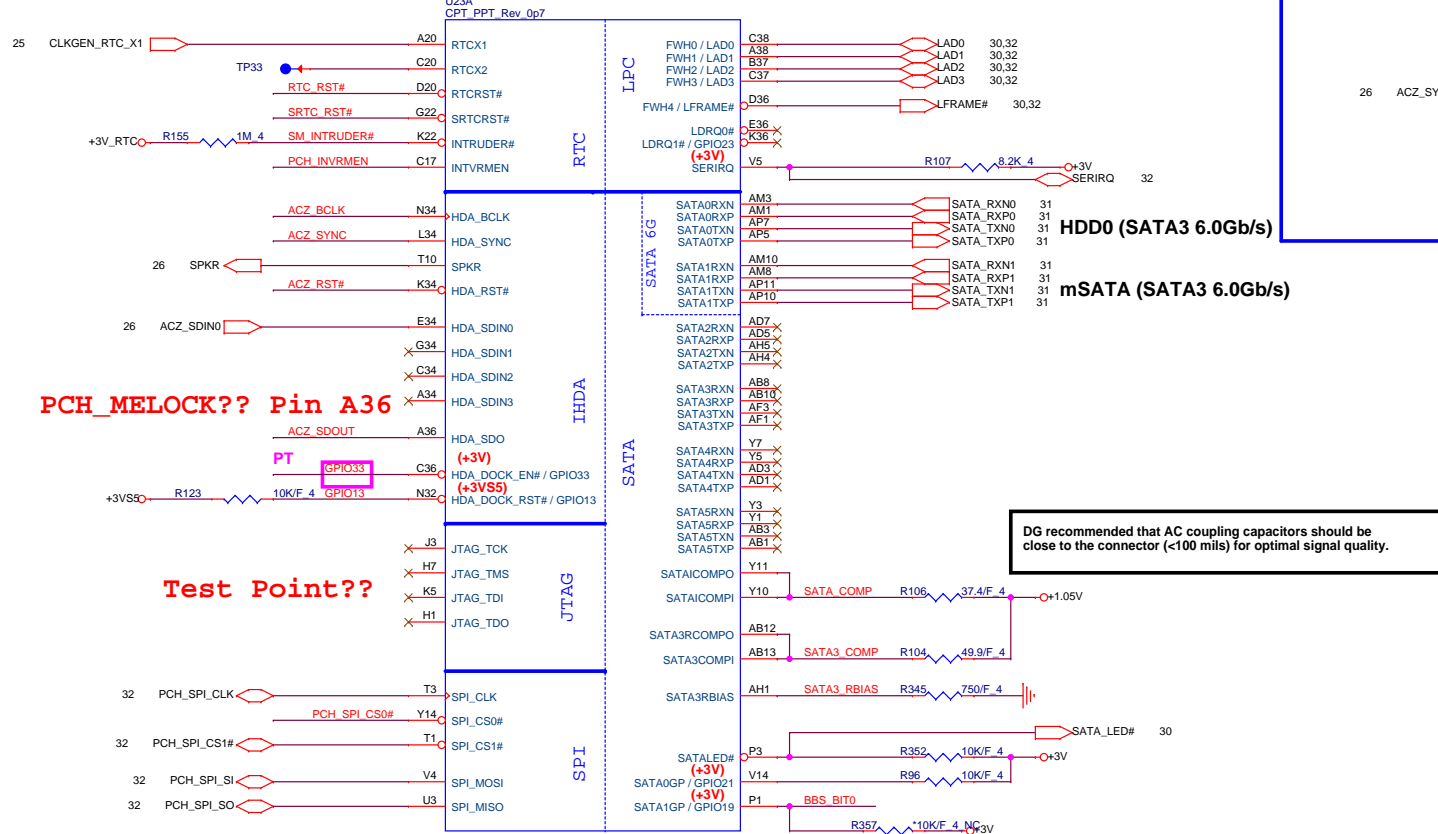
Cougar Point/Panther Point (DMI,FDI,PM)

Cougar Point/Panther Point (LVDS,DDI)



R126 Change 5%

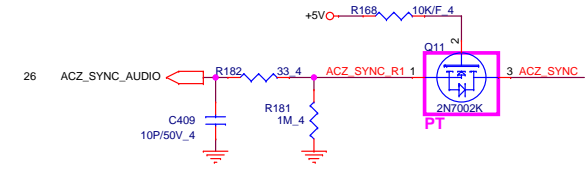
Cougar Point/Panther Point (HDA,JTAG,SATA)



PCH_MELOCK?? Pin A36

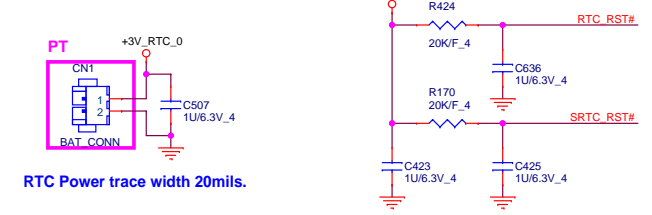
Test Point??

DG recommended that AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.



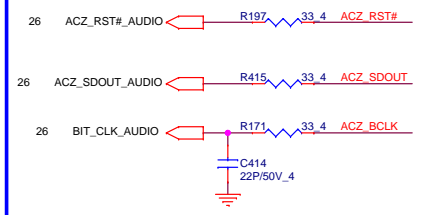
HDD0 (SATA3 6.0Gb/s)
mSATA (SATA3 6.0Gb/s)

RTC Circuitry(RTC)



RTC Power trace width 20mils.

HDA Bus(CLG)

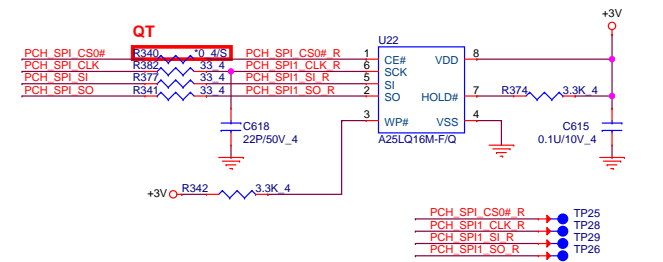


PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	+3V ₀ - R387 10K/F 4 - PCL_GNT3# 12
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V _{RTC0} - R423 330K 4 PCH_INVRMEN
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 - R444 *1K/F 4 NC - ACZ_SDOUT 32 PT
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#	R356 *1K/F 4 NC - BBS_BIT0
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		R381 *1K/F 4 NC - BBS_BIT1 12
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm	+1.8V ₀ - R343 2.2K 4 - R344 1K/F 4 - NV_CLE 13 H_SNB_IVB# 06
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3VSS ₀ - R164 1K/F 4 - ACZ_SYNC
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	+3VSS ₀ - R445 *1K/F 4 NC - ACZ_SDOUT PT
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	

Vender	Size	P/N
AMIC	2MB	AKE38ZN0802 (A25LQ16M-F/Q)
GGD	2MB	AKE38GN0Q00 (GD25Q16BSIGR)

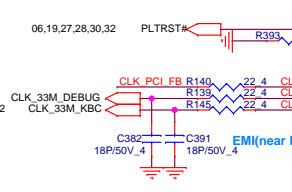
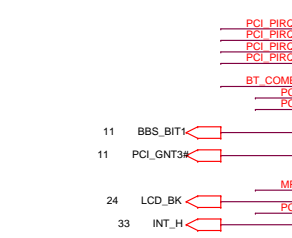
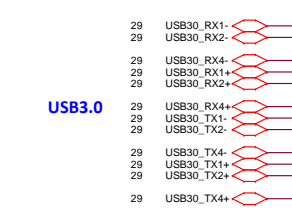
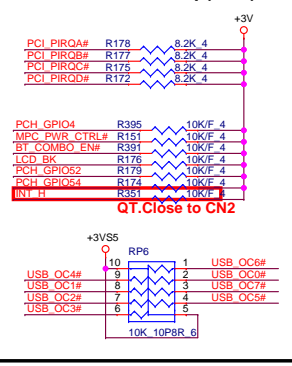
PCH SPI ROM(CLG)



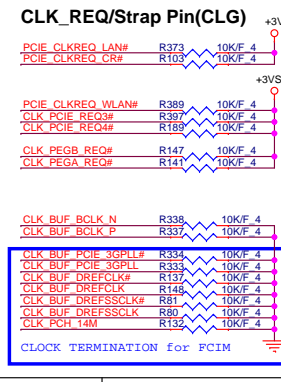
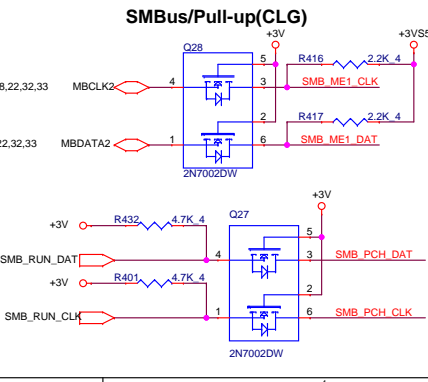
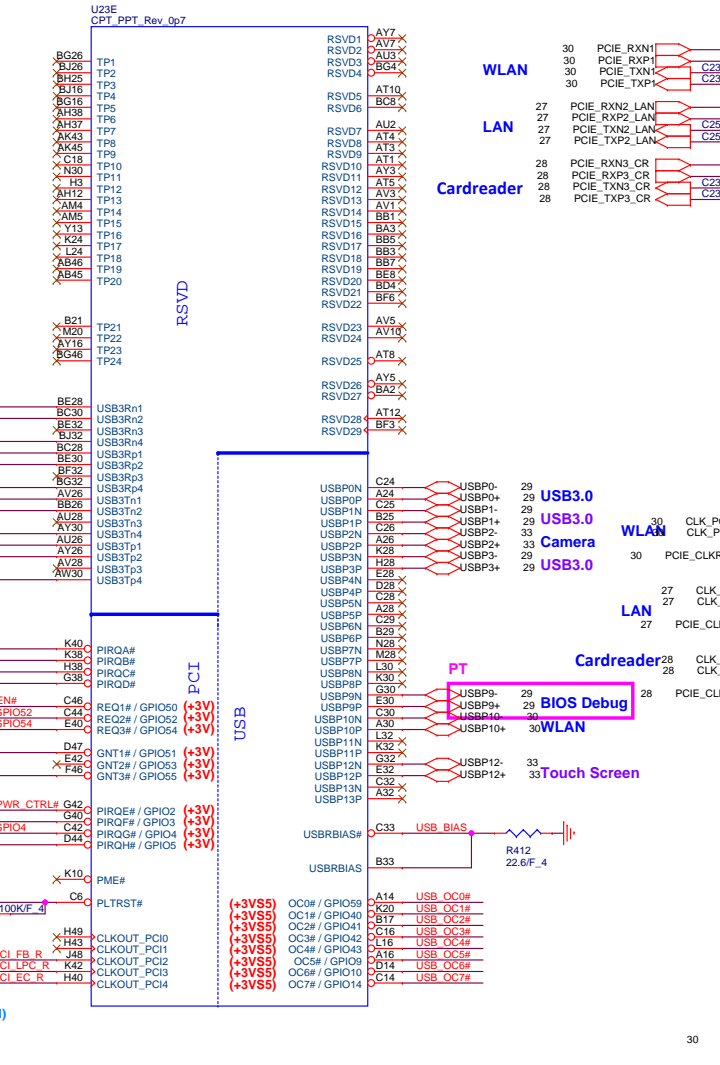
Quanta Computer Inc.
PROJECT : JW8

Size: Document Number: PCH 2/6 (HDA/RTC/SATA/SPI) Rev 3A
Date: Friday, November 02, 2012 Sheet 11 of 46

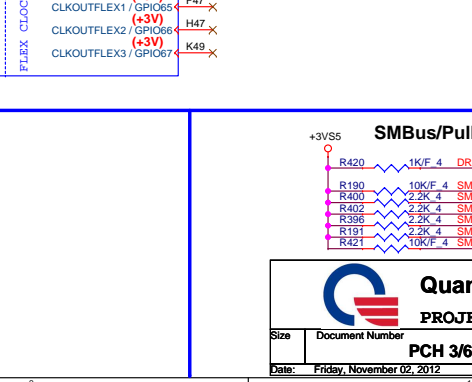
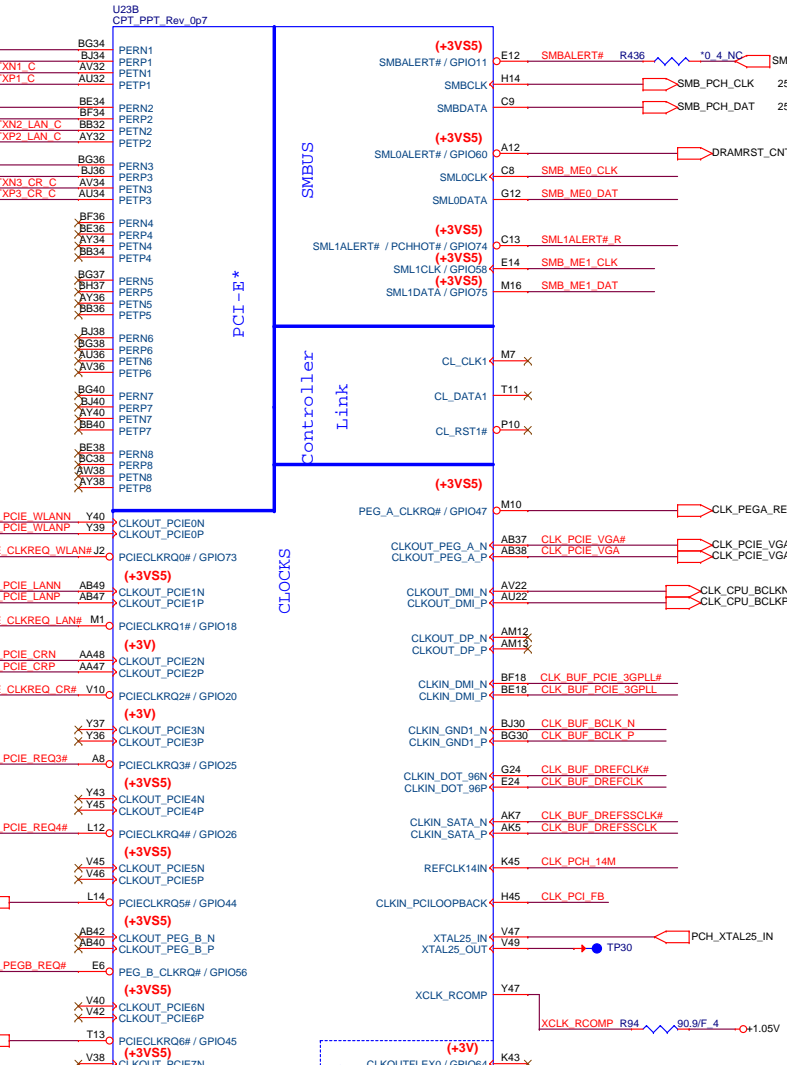
PCI/USBOC# Pull-up(CLG)



Cougar Point-M/Panther Point (PCI,USB,NVRAM)



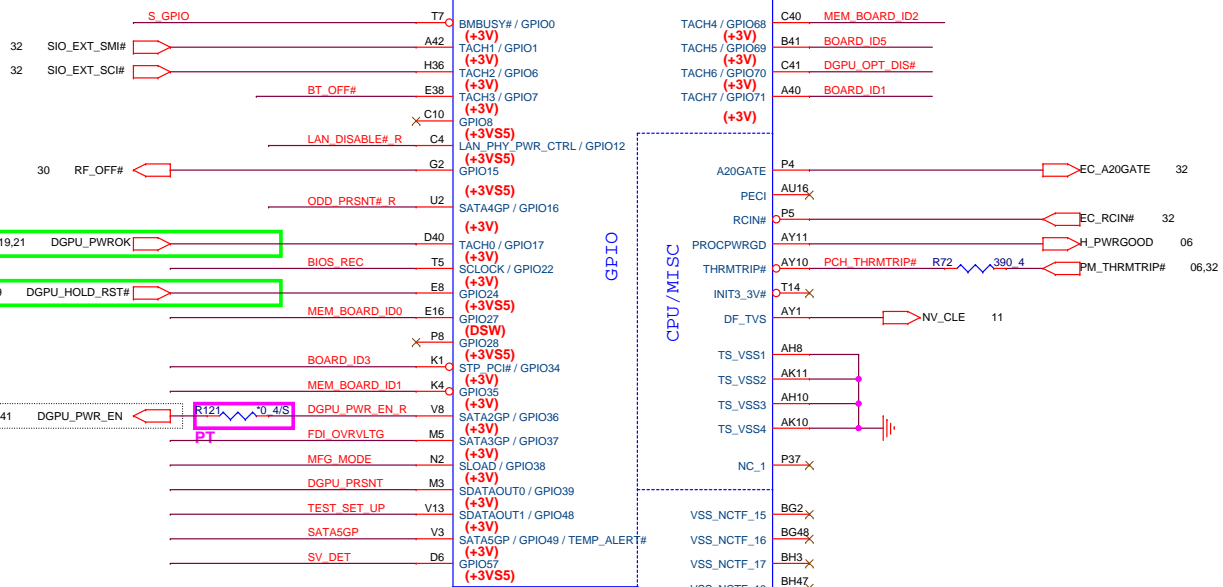
Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)



Quanta Computer Inc. PROJECT : JW8. Size Document Number PCH 3/6 (Clock/PCI/PCIE/USB) Rev 3A. Date: Friday, November 02, 2012 Sheet 12 of 46

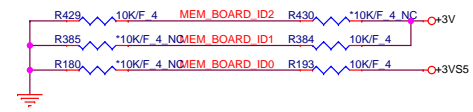
Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)

U23F
CPT_PPT_Rev_0p7



OPTIMUS POWER control pin	
DGPU_PWROK	GPIO17
DGPU_HOLD_RST#	GPIO24
DGPU_PWR_EN	GPIO36

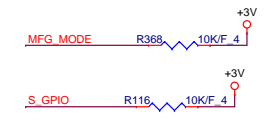
Default: HYNIX DDR3-1600 2GB



System Memory BOARD ID SETTING

	GPIO68 MEM_BOARD_ID2	GPIO35 MEM_BOARD_ID1	GPIO27 MEM_BOARD_ID0
HYNIX DDR3-1600 2GB	0	0	0
SAMSUNG DDR3-1600 2GB	0	0	1
On Board DDR3 N.C	0	1	1
RESERVE	0	1	0
RESERVE	1	0	0
RESERVE	1	0	1
RESERVE	1	1	1
RESERVE	1	1	0

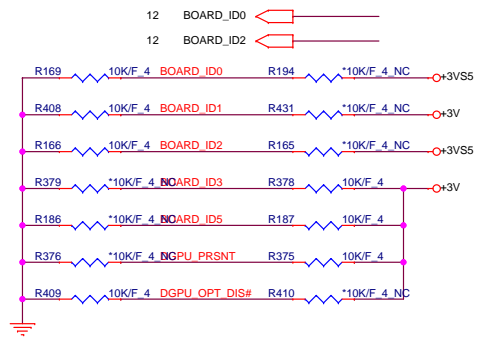
MFG-TEST



BOARD_ID[3:0]	Model Name
0000	ST2 SV nonTouch
0001	ST2 ULV nonTouch
0010	ST2 SV Touch
0011	ST2 ULV Touch
0100	QT SV nonTouch
0101	QT ULV nonTouch
0110	QT SV Touch
0111	QT ULV Touch
1000	ST1 SV nonTouch
1001	Reserve
1010	ST1 SV Touch
1011	Reserve

Chief River BOARD ID SETTING

BOARD_ID0	GPIO44	SV=0, ULV=1
BOARD_ID1	GPIO71	NonTouch=0, Touch=1
BOARD_ID2	GPIO46	Phase select
BOARD_ID3	GPIO34	Phase select
BOARD_ID5	GPIO69	HM76=0, HM77=1
DGPU_PRSN#	GPIO39	Optimus=1, UMA=0
DGPU_OPT_DIS#	GPIO70	Optimus=0, Dis only=1



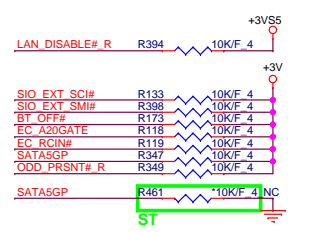
Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

BIOS RECOVERY High = Disable (Default)
Low = Enable

SV_SET_UP High = Strong (Default)

TEST DETECT Low = Default

GPIO Pull-up/Pull-down(CLG)



FDI TERMINATION VOLTAGE OVERRIDE Reserved only

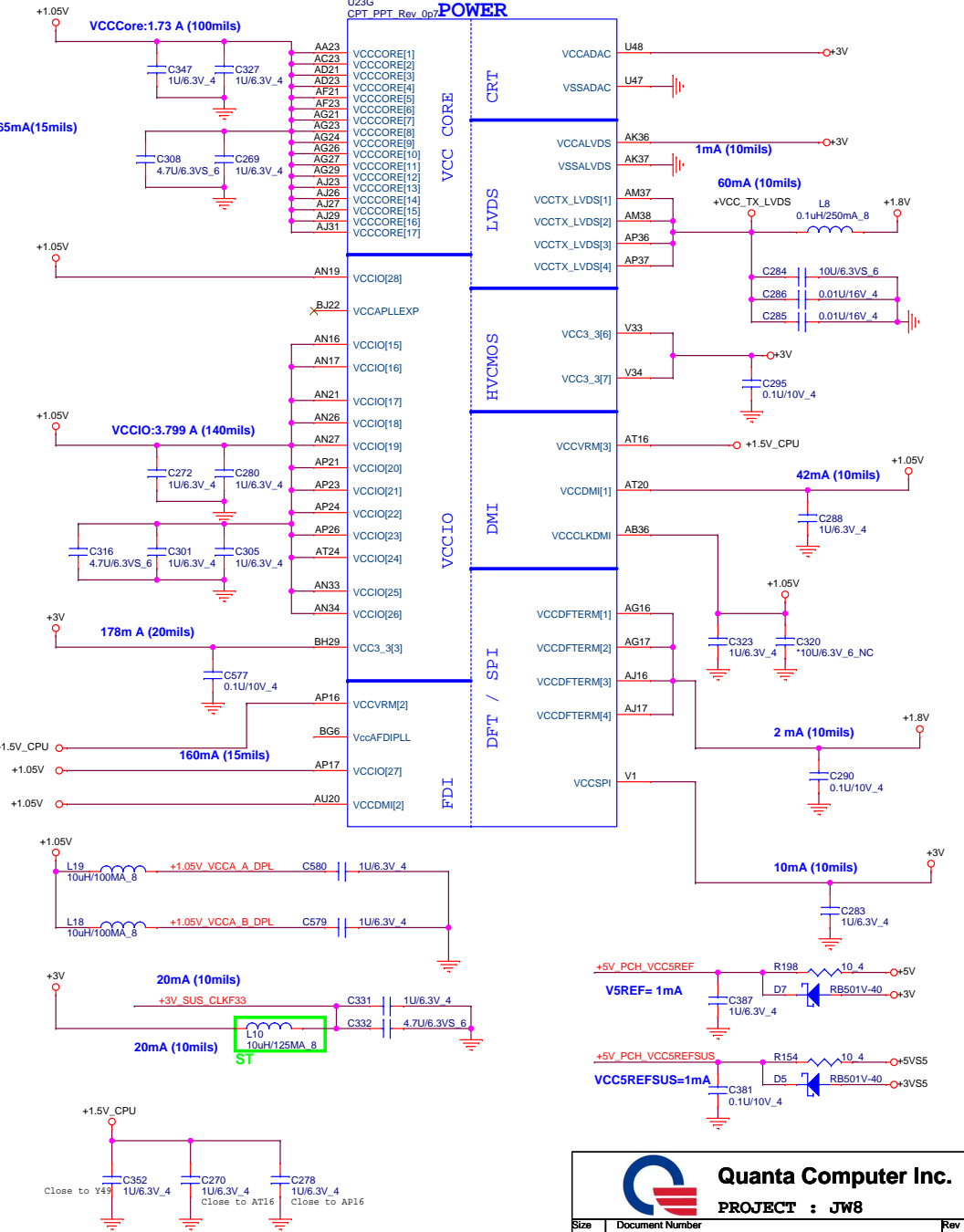
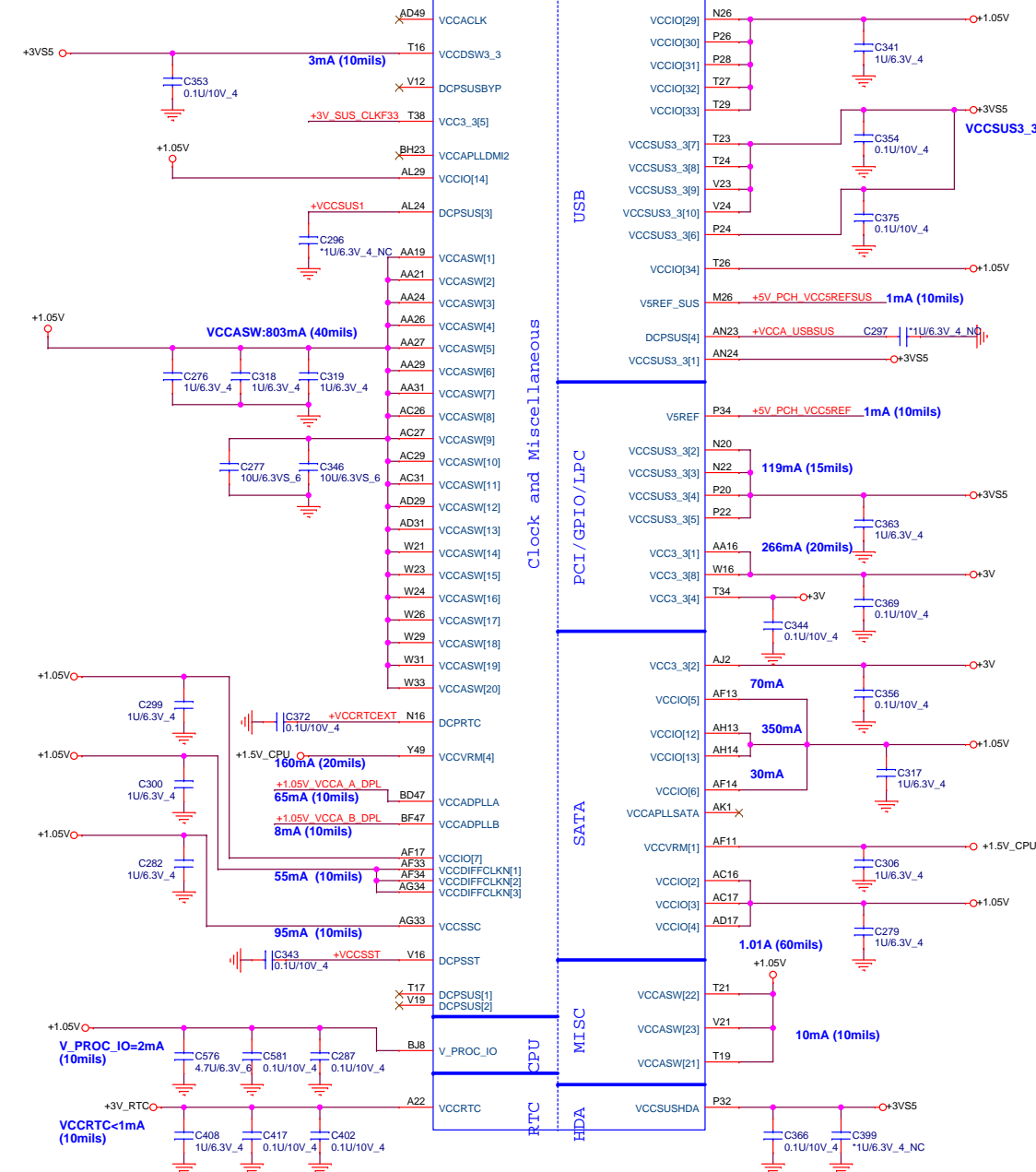
Quanta Computer Inc.
PROJECT : JW8

Size	Document Number	PCH 4/6 (GPIO)	Rev 3A
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U23J
CPT_PPT_Rev_0p7
POWER

Cougar Point/Panther Point (POWER)

U23G
CPT_PPT_Rev_0p7
POWER

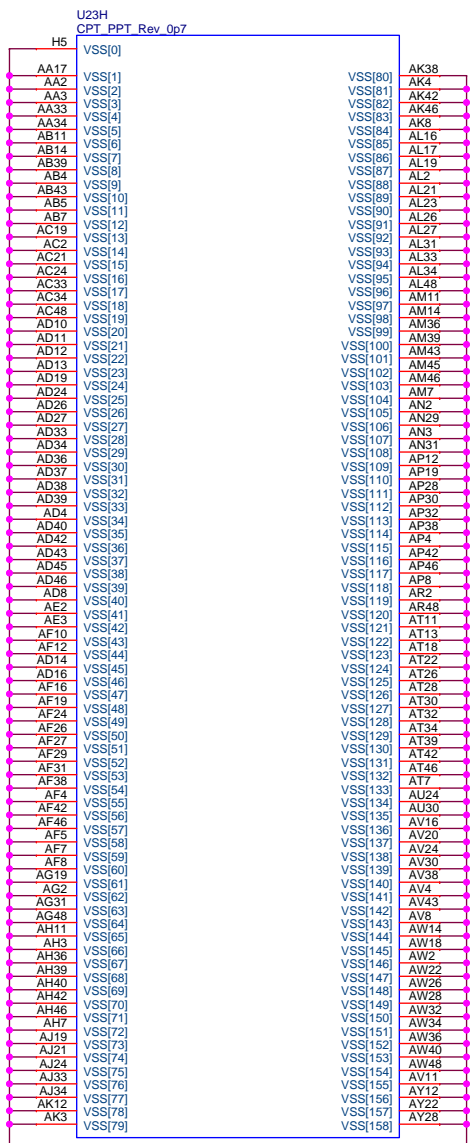
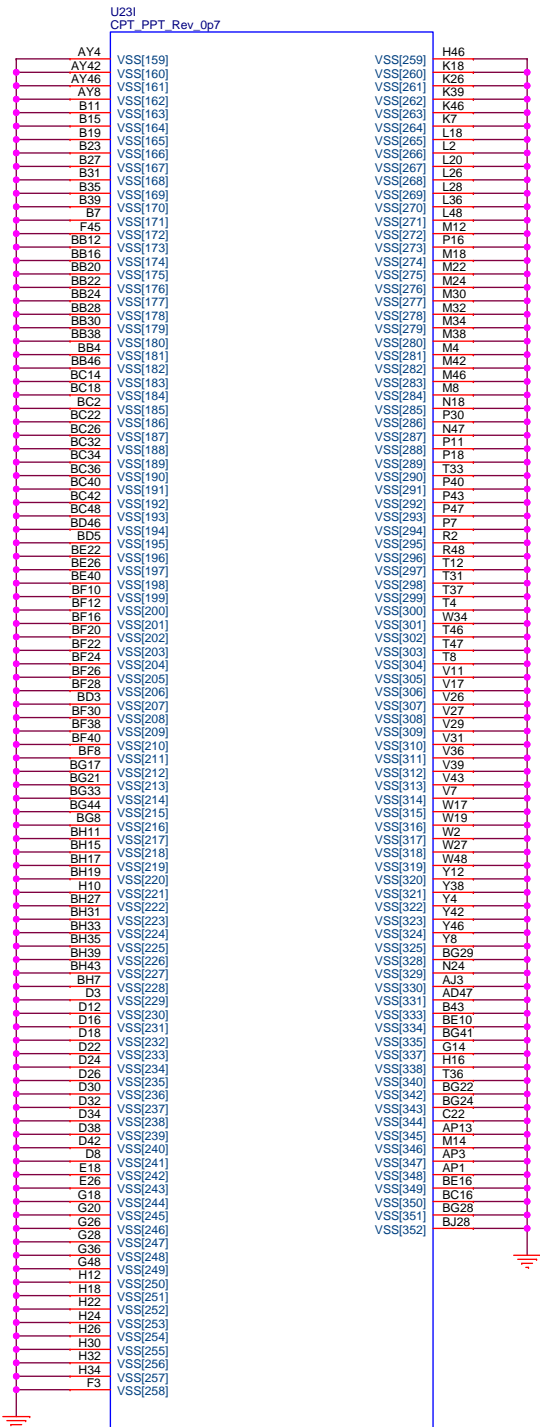



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PROJECT : JW8

Size	Document Number	PCH 5/6 (Power)	Rev 3A
Date:	Friday, November 02, 2012	Sheet 14 of 46	

Cougar Point/Panther Point (GND)

Cougar Point/Panther Point (GND)

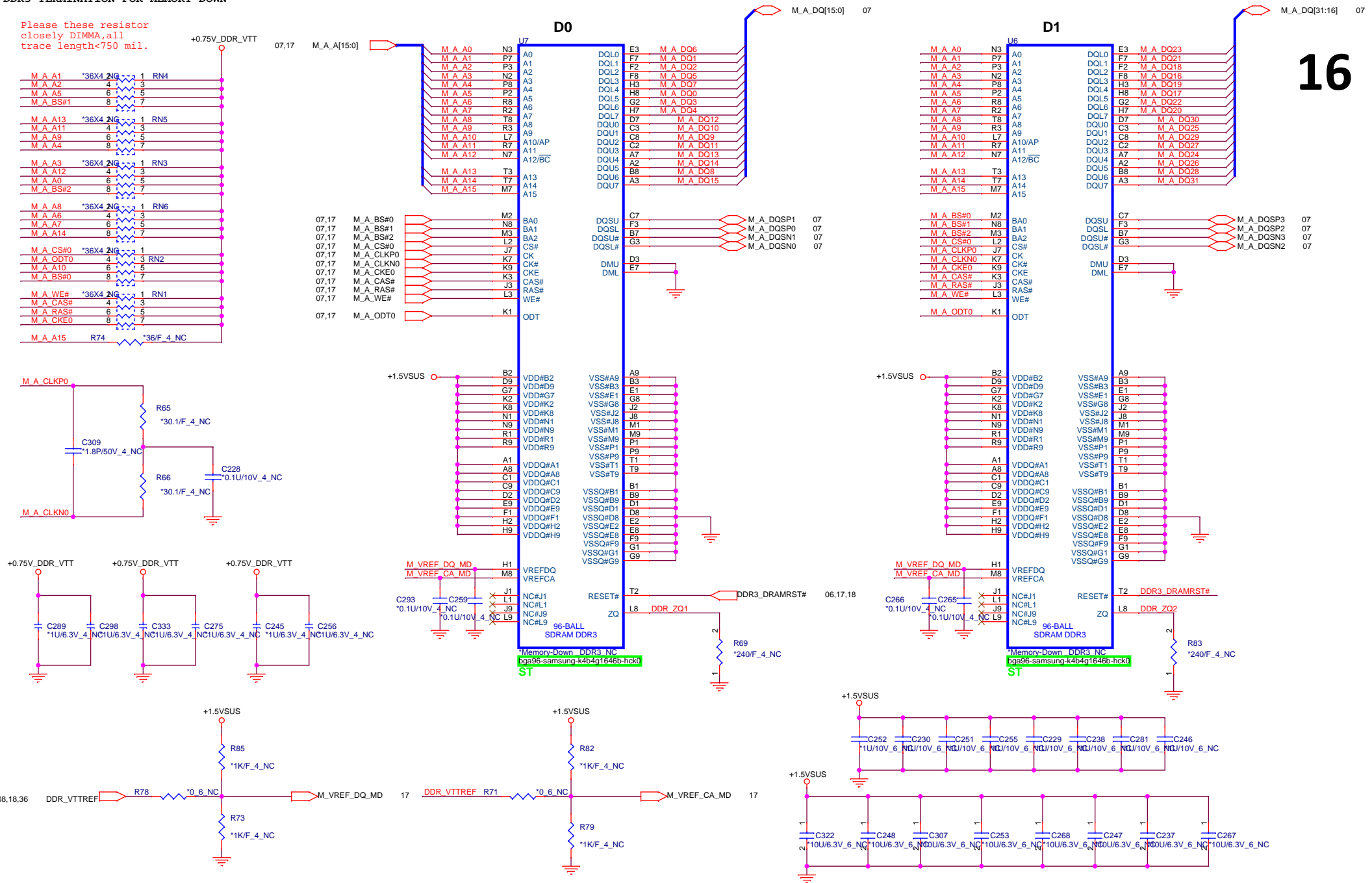


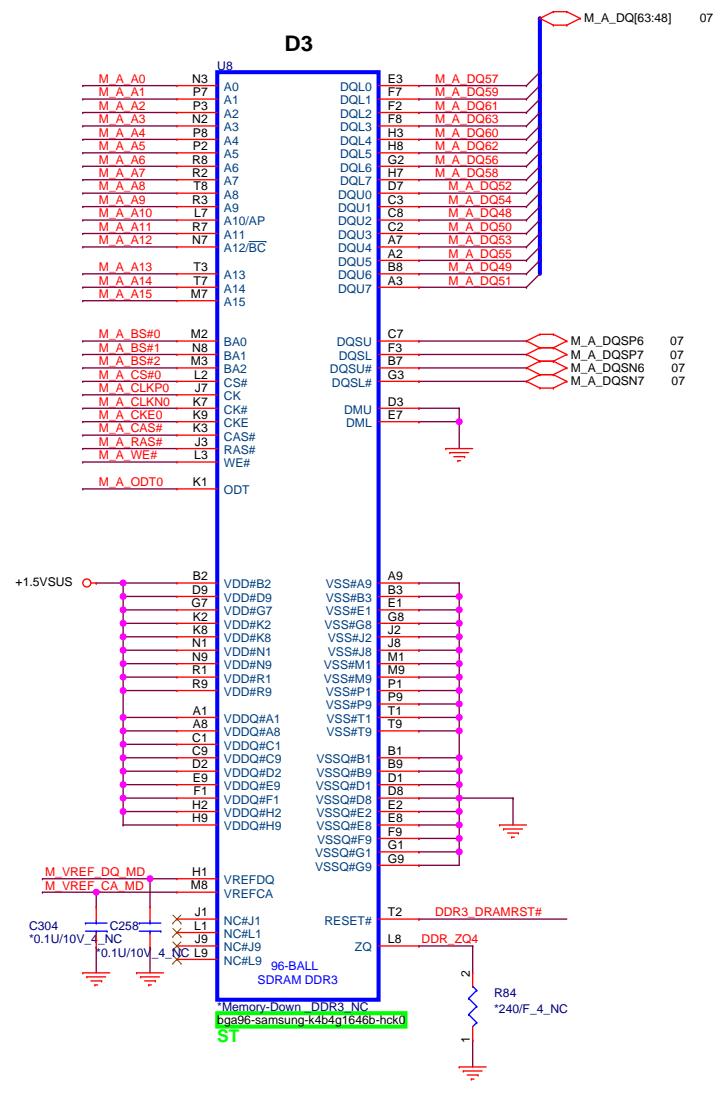
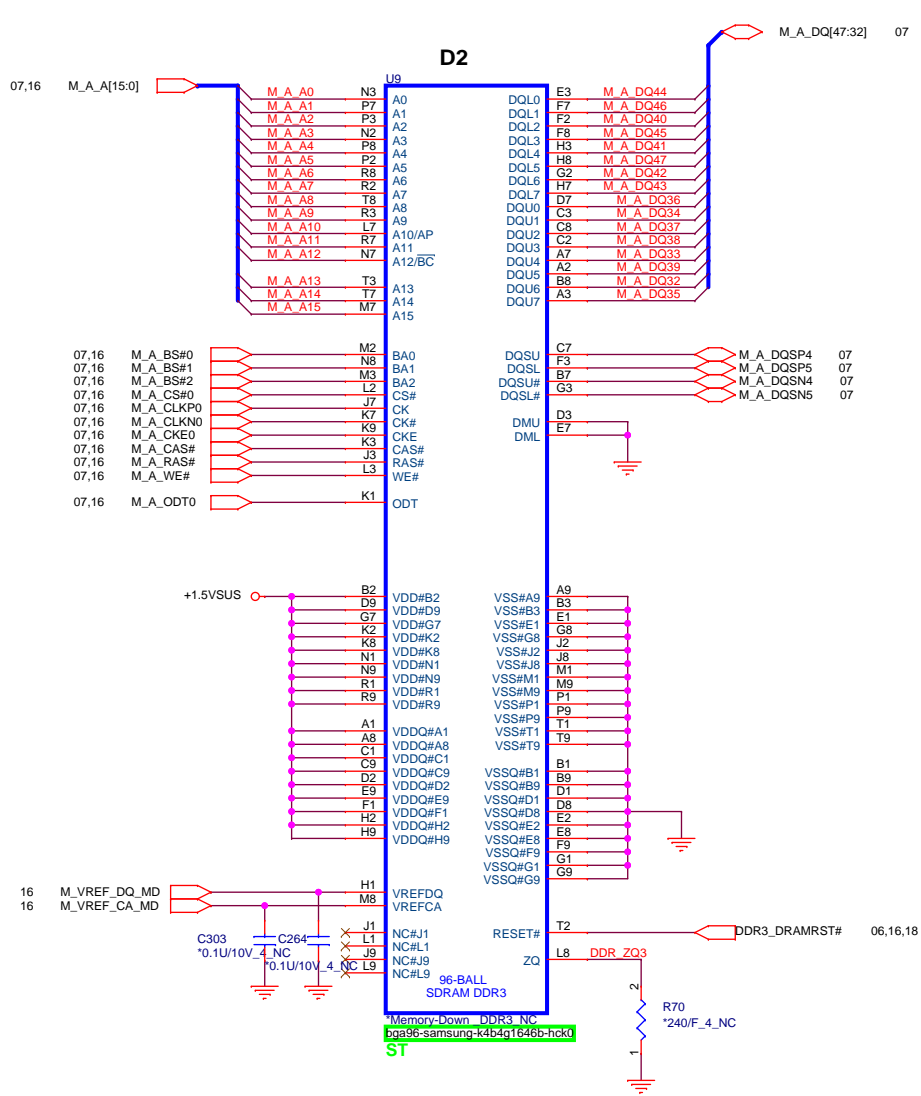
 **Quanta Computer Inc.**
PROJECT : JW8

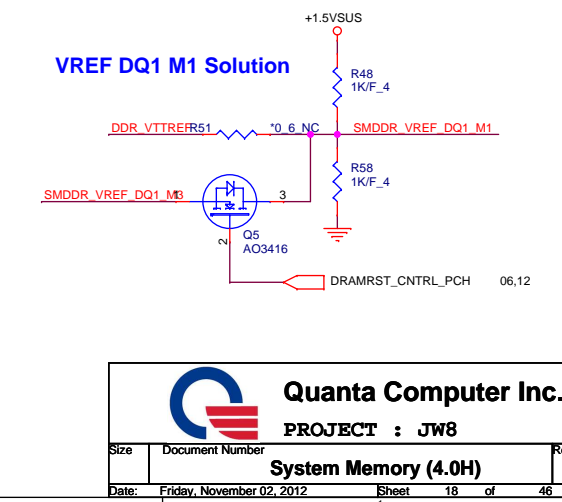
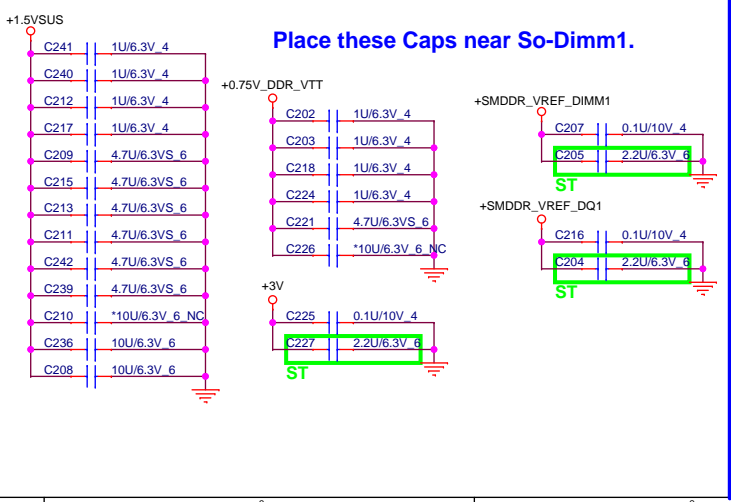
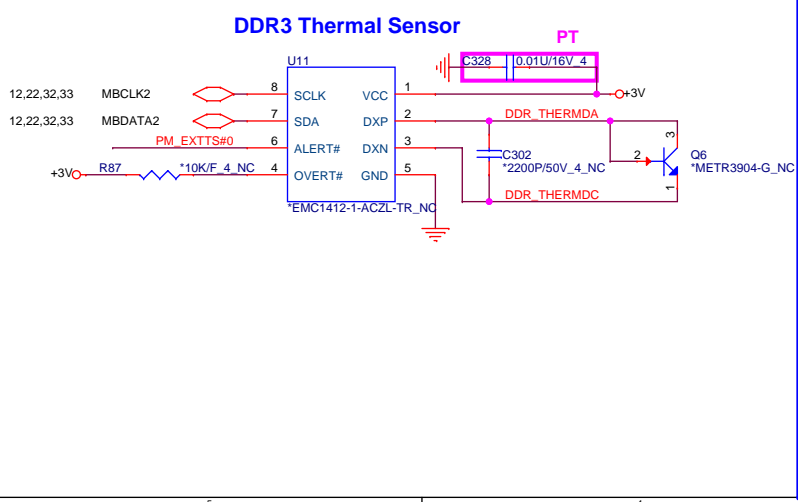
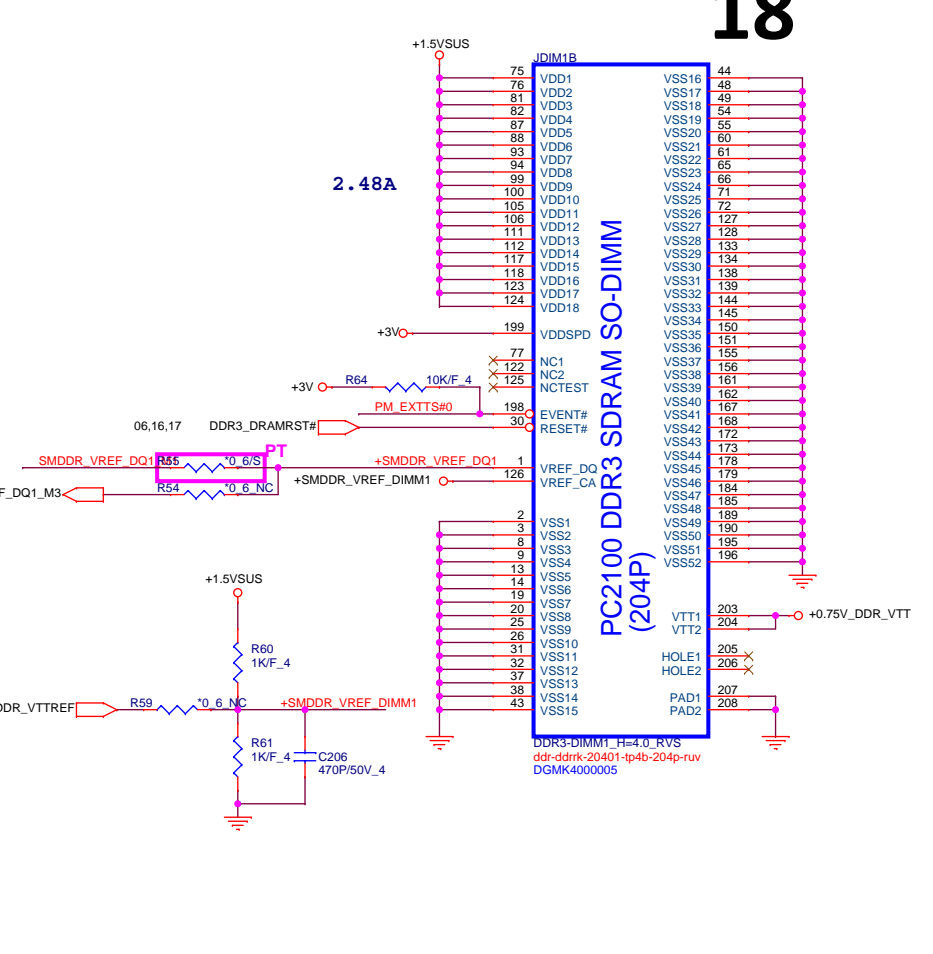
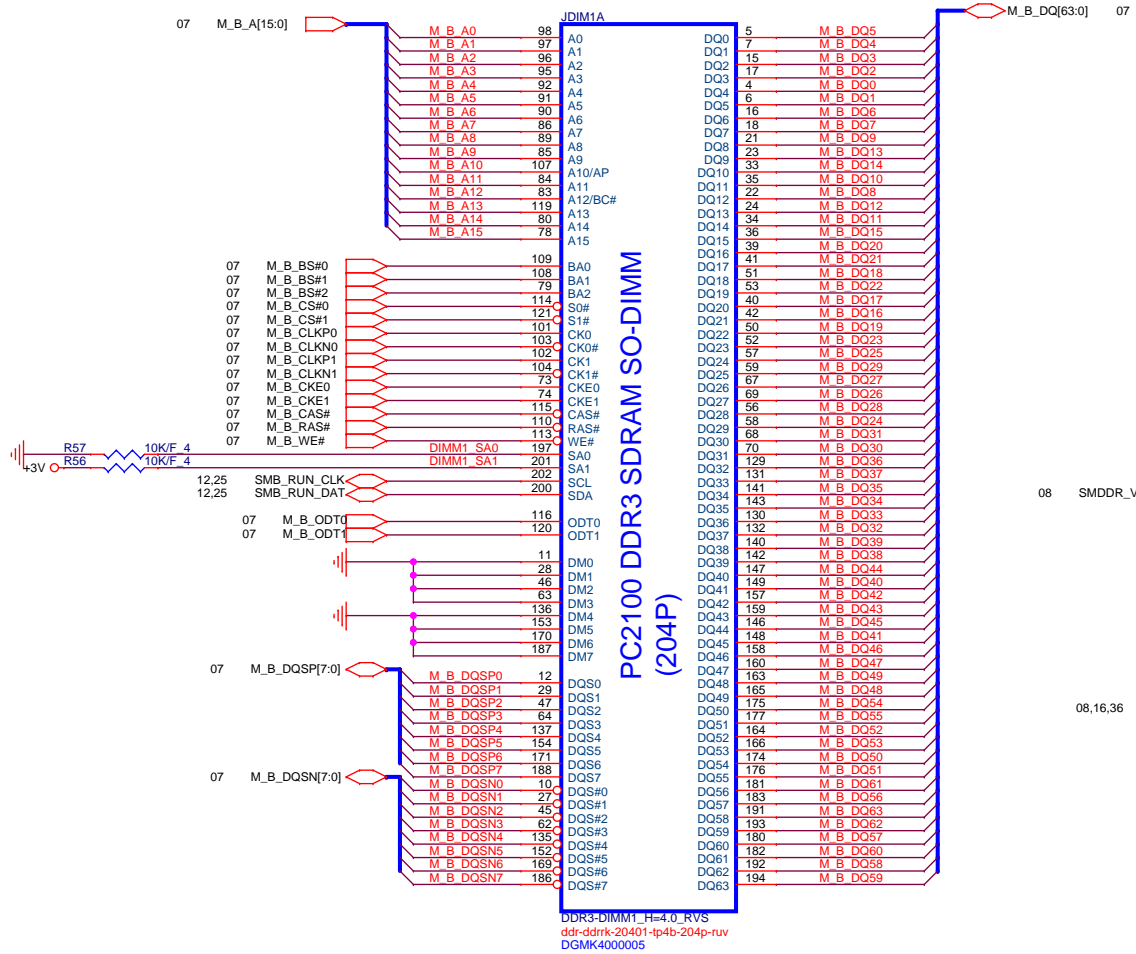
Size	Document Number	Rev
	PCH 6/6 (Ground)	3A
Date: Friday, November 02, 2012		Sheet 15 of 46

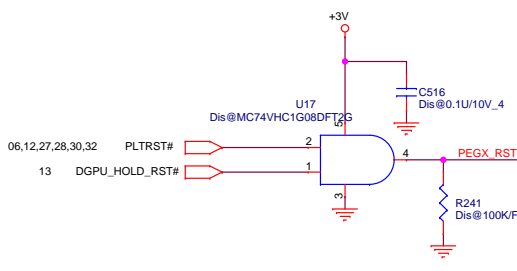
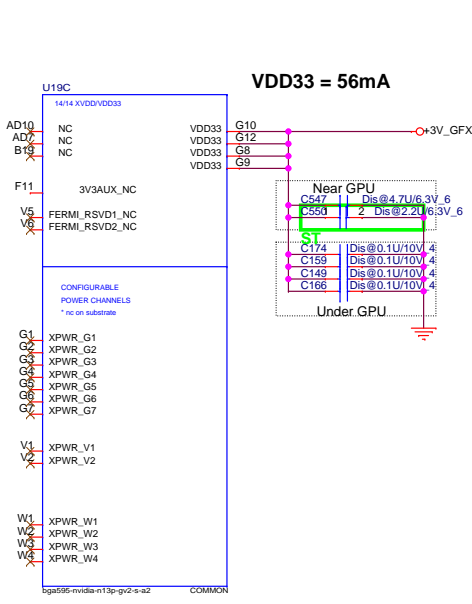
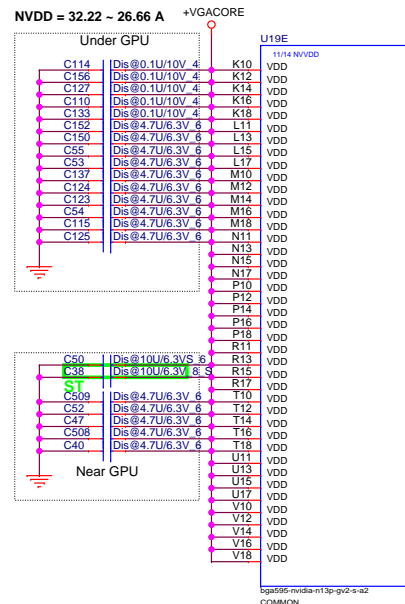
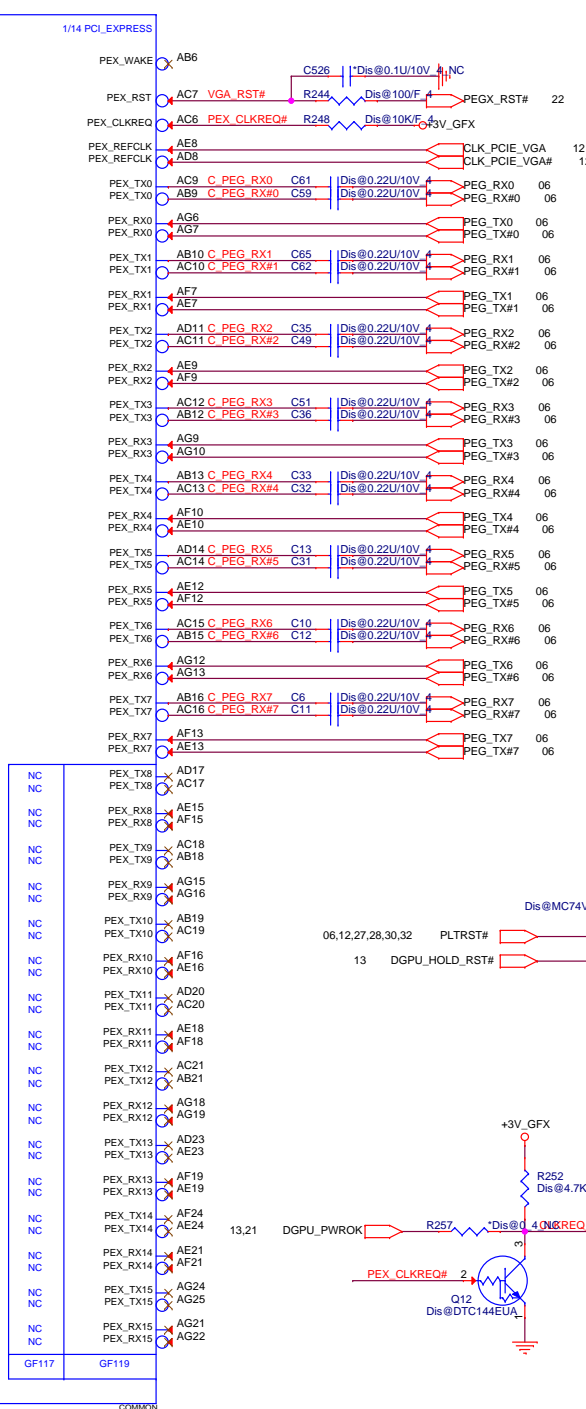
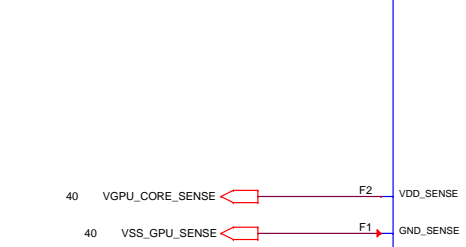
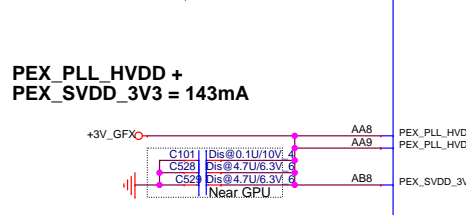
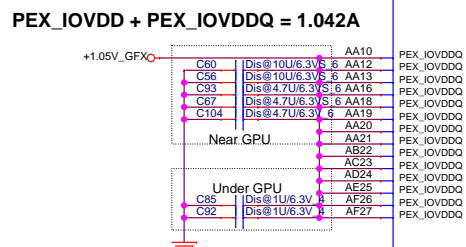
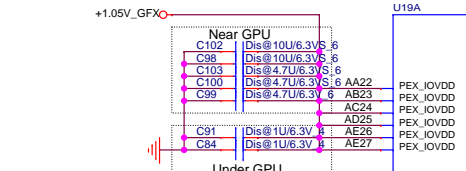
DDR3 TERMINATION FOR MEMORY DOWN

Please these resistor closely DIMMA, all trace length < 750 mil.

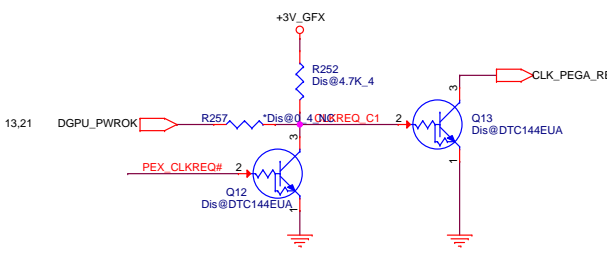
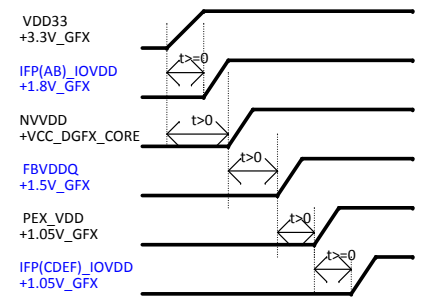




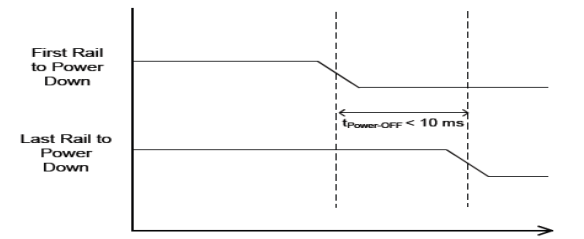




Power up sequence

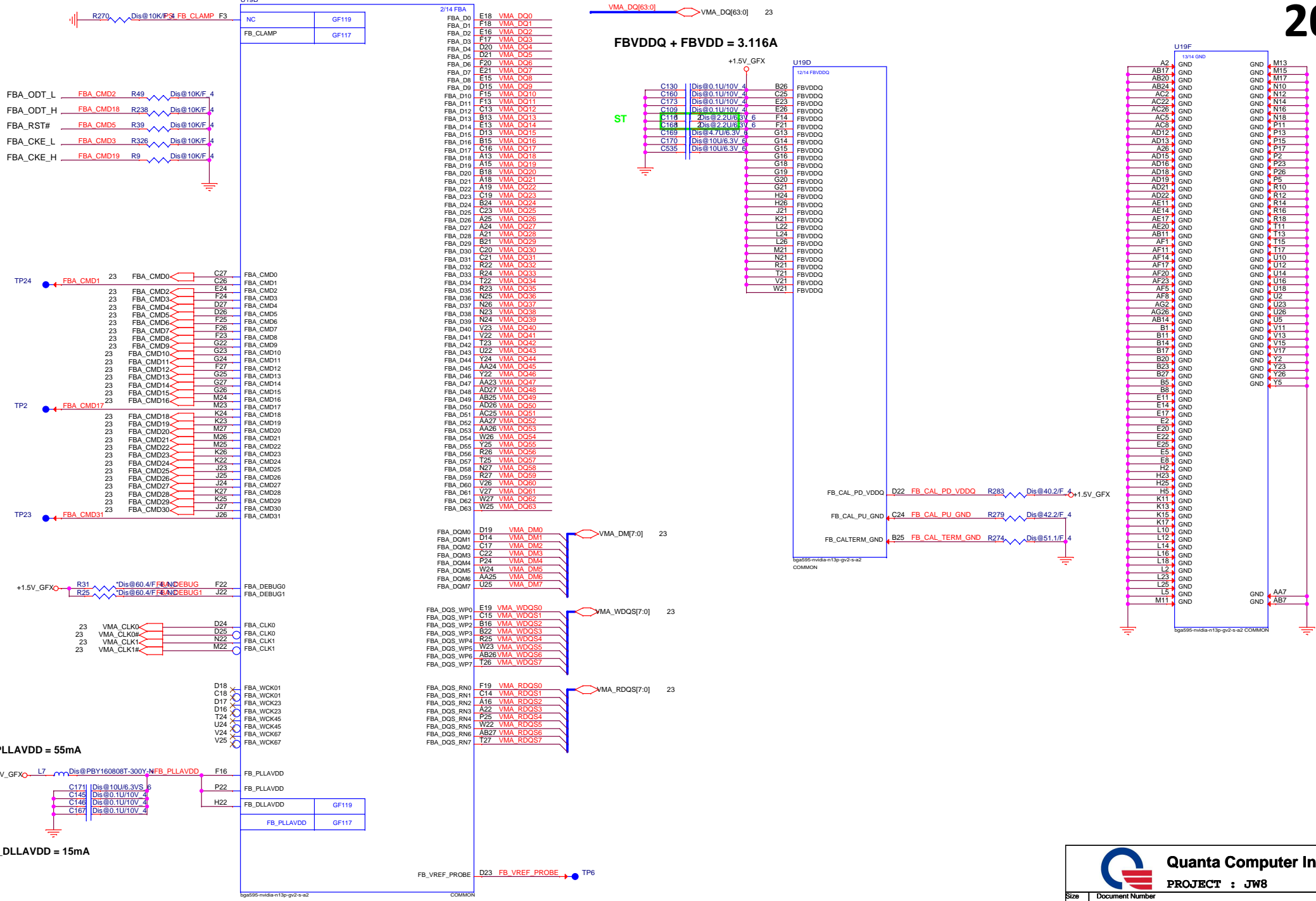


Power down sequence



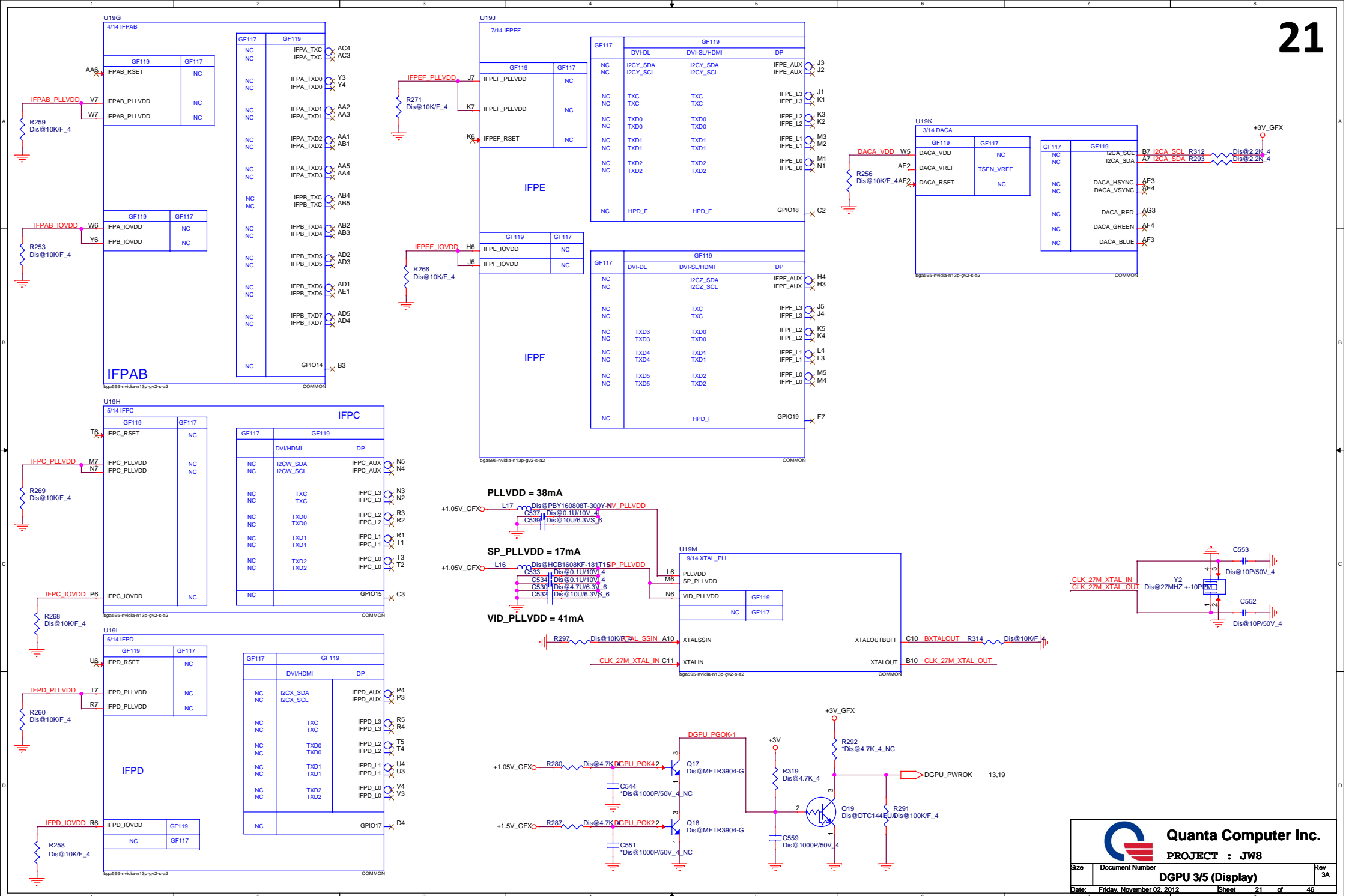
Quanta Computer Inc.
PROJECT : JW8

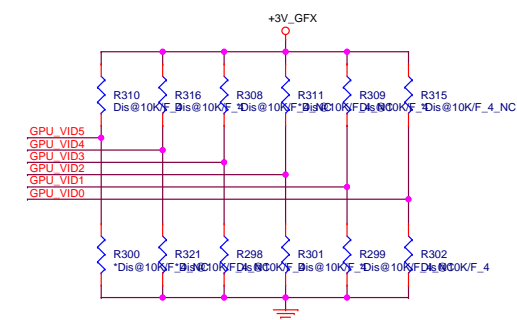
Size	Document Number	DGPU 1/5 (PEG)	Rev 3A
Date: Friday, November 02, 2012		Sheet 19 of 46	



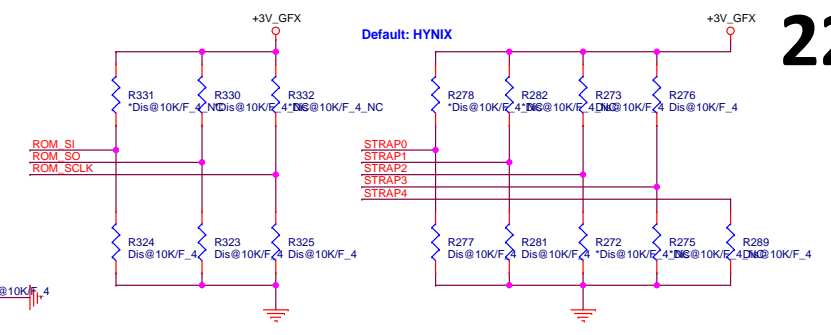
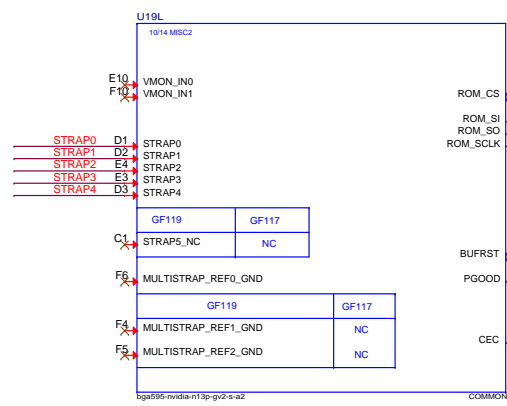
Quanta Computer Inc.
PROJECT : JW8

Size	Document Number	Rev
	DGPU 2/5 (Memory)	3A
Date:	Friday, November 02, 2012	Sheet 20 of 46



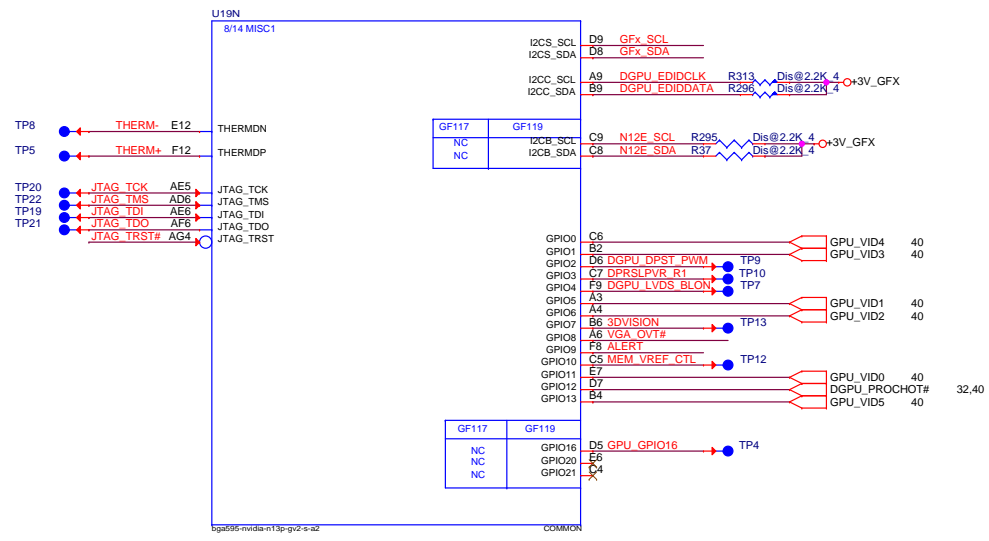


N13P-GV2 NVDD HW BOOT Voltage = 0.875V
VID = 110010



Binary Strap Mode Mapping

Strap Pin name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10Kohm	Pull-down to GND
ROM_SI	SUB_VENDOR	10Kohm	Pull-UP to 3V3 if VBIO ROM Exists Pull-down to GND (no dispaly)
ROM_SO	VGA_DEVICE	10Kohm	Pull-down to GND (no dispaly)
STRAP0	RAMCFG[0]	10Kohm	USER defined
STRAP1	RAMCFG[1]	10Kohm	USER defined
STRAP2	RAMCFG[2]	10Kohm	USER defined
STRAP3	RAMCFG[3]	10Kohm	USER defined
STRAP4	PCIE_MAX_SPEED	10Kohm	Pull-down to GND

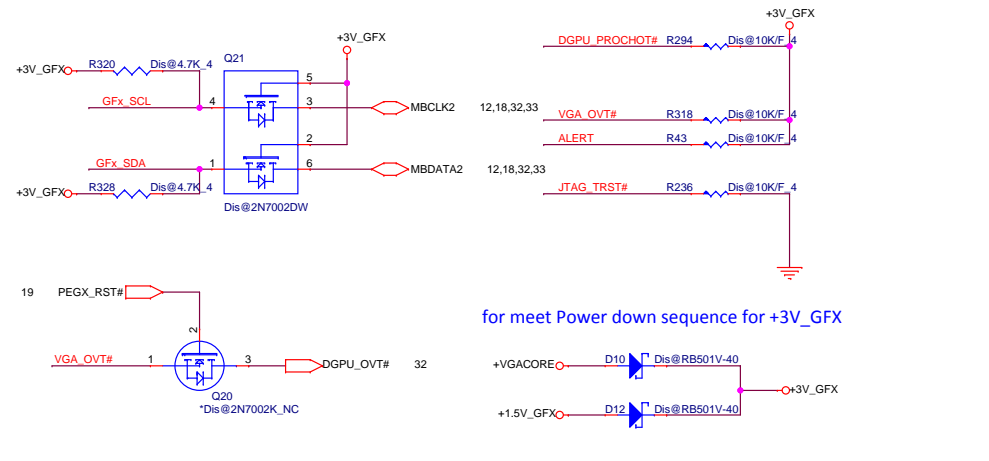


VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	QCI P/N
0000		Reserved		
1100	DDR3 128Mx16x4, 64bit, 2Gb,900MHz	HYNIX	H5TQ2G63DFR-11C	AKD5MGWTW16
1011	DDR3 128Mx16x4, 64bit, 2Gb,900MHz	SAMSUNG	K4W2G1646E-BCL11	AKD5MGWT526
	DDR3 256Mx16x4, 64bit, 4Gb,900MHz	HYNIX	H5TQ4G63MFR-11C	AKD5PGWTW04
	DDR3 256Mx16x4, 64bit, 4Gb,900MHz	SAMSUNG	K4W4G1646B-HC11	AKD5MGWT516

GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	OUT	GPU_VID4	GPU CORE_VDD VID4
1	OUT	GPU_VID3	GPU CORE_VDD VID3
2	OUT	CD_BL_PWM	LCD BACKLIGHT PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	GPU_VID1	GPU CORE_VDD VID1
6	OUT	GPU_VID2	GPU CORE_VDD VID2
7	OUT	3D VISION	3D VISION LEFT/RIGHT VISION
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM VREF	MEMORY VREF CONTROL
11	OUT	GPU_VID0	GPU CORE_VDD VID0
12	IN	PWR_LEVEL	Power Detect ,HIGH=AC, LOW=DC
13	OUT	GPU_VID5	GPU CORE_VDD VID5
14	IN	HPD_AB	HOT PLUG DETECT FOR IFPAB
15	IN	HPD_C	HOT PLUG DETECT FOR IFPC
16	OUT	MEM_VDD	MEMORY VDD CONTROL
17	IN	HPD_D	HOT PLUG DETECT FOR IFPD
18	IN	HPD_E	HOT PLUG DETECT FOR IFPE
19	IN	HPD_F	HOT PLUG DETECT FOR IFPF
20/21		RESERVE	



for meet Power down sequence for +3V_GFX

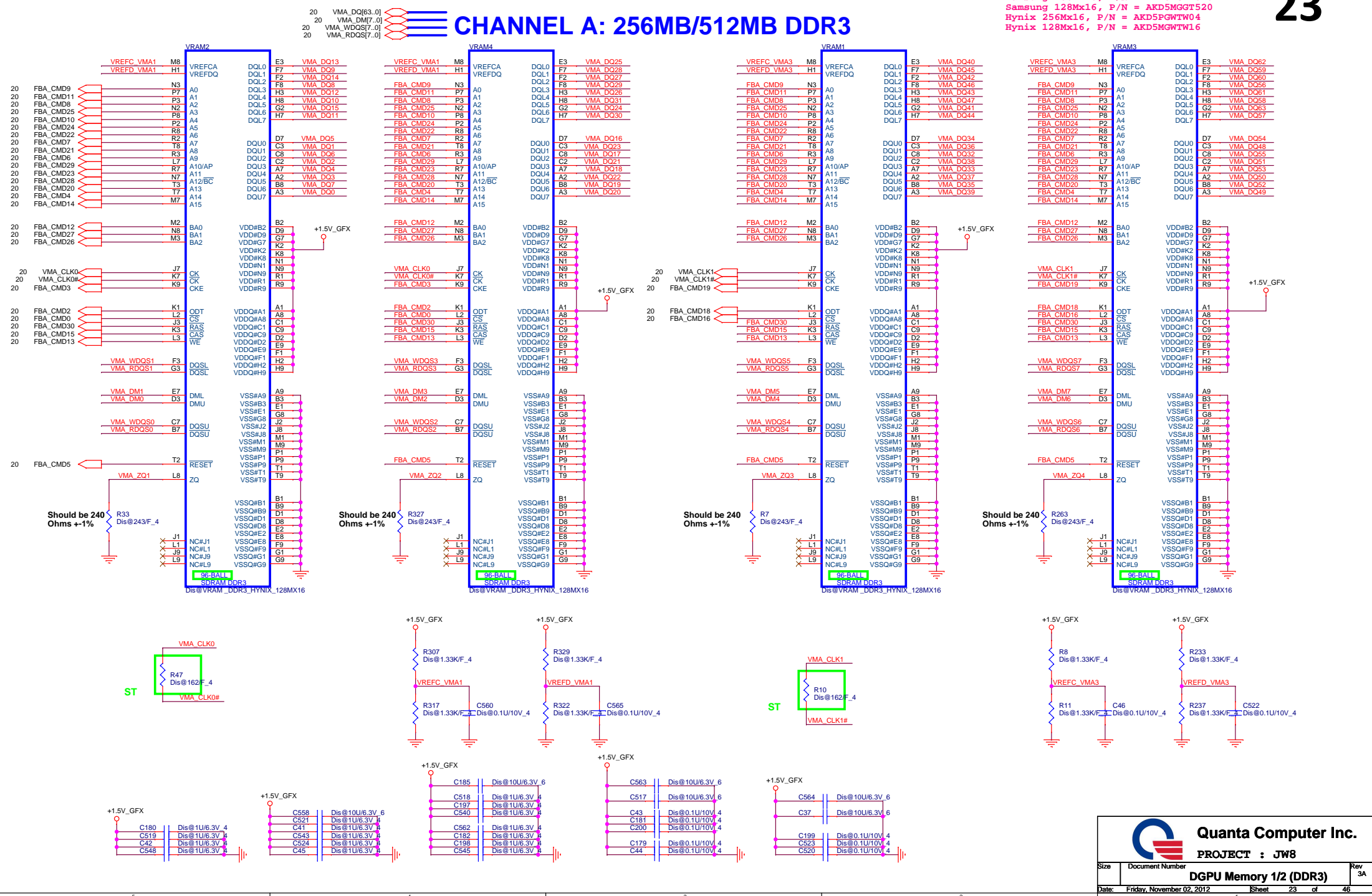
Quanta Computer Inc.
PROJECT : JW8

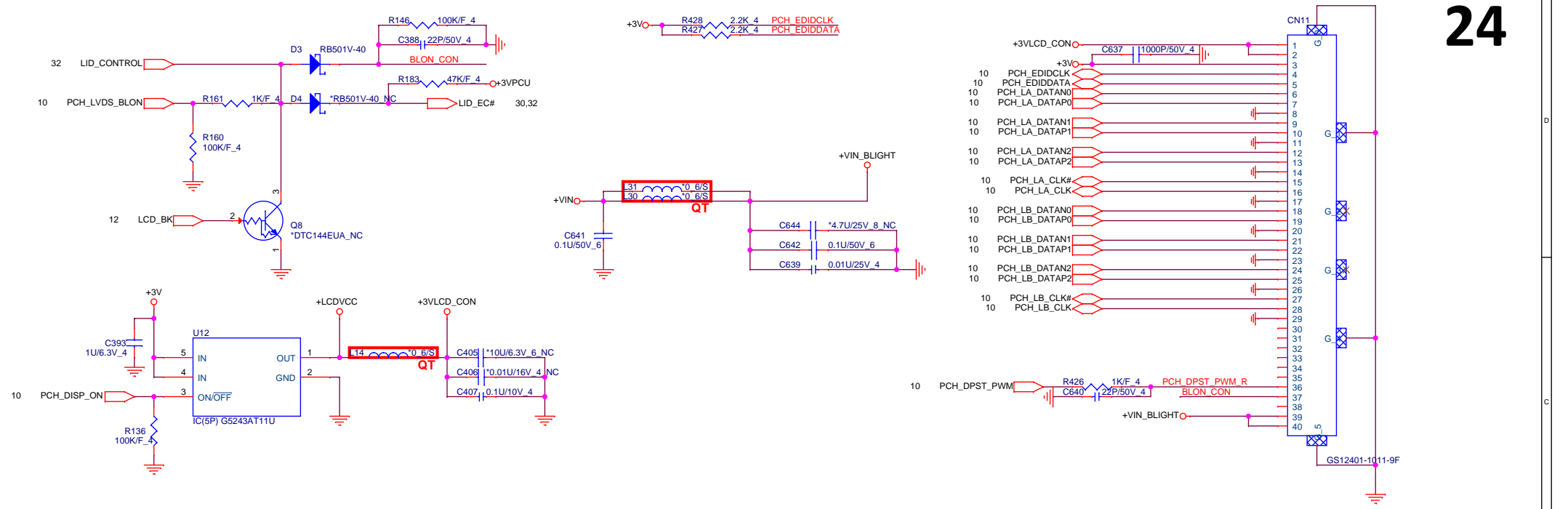
Size	Document Number	Rev
	DGPU 4/5 (MIO/GPIO)	3A

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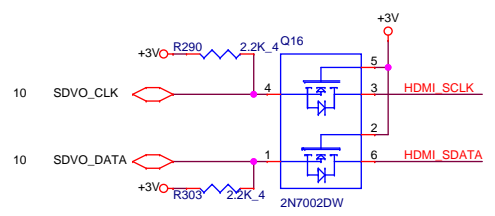
900MHz VRAM size:
Samsung 256Mx16, P/N = AKD5MGWT516
Samsung 128Mx16, P/N = AKD5MGWT520
Hynix 256Mx16, P/N = AKD5PGWTW04
Hynix 128Mx16, P/N = AKD5MGWTW16

CHANNEL A: 256MB/512MB DDR3

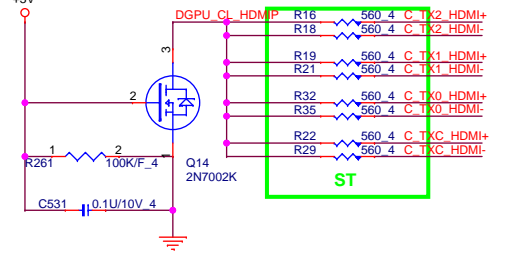




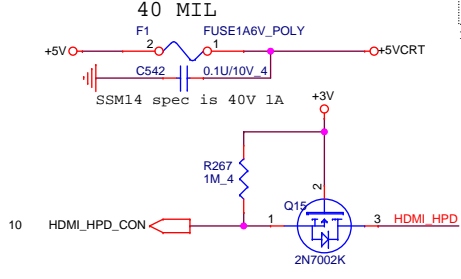
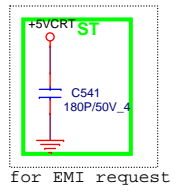
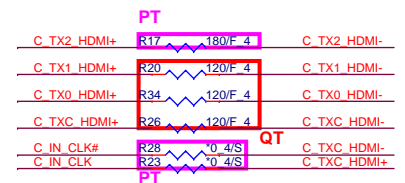
HDMI SMBus Isolation



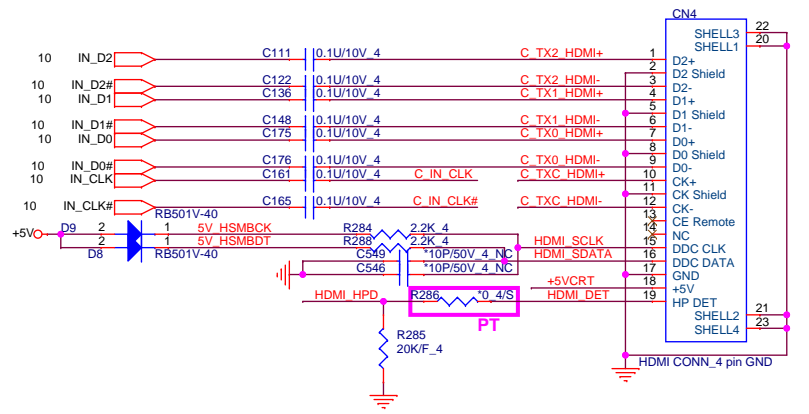
Close to HDMI connector



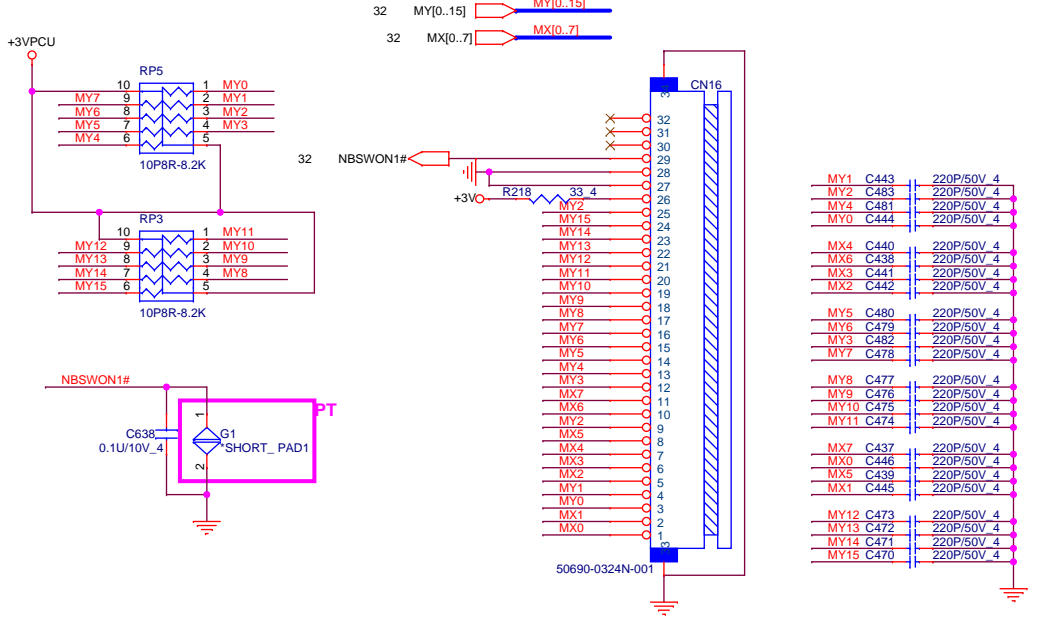
EMI Solution



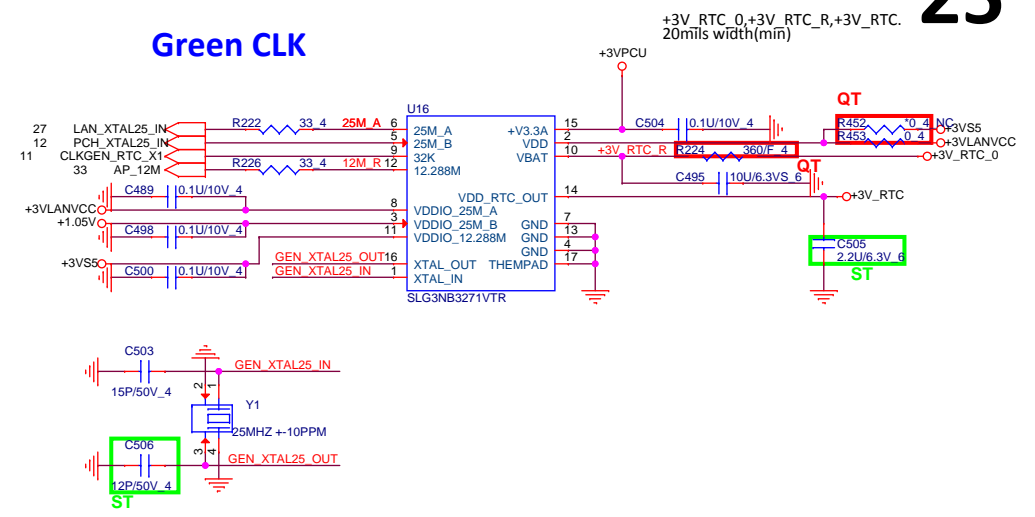
HDMI PORT



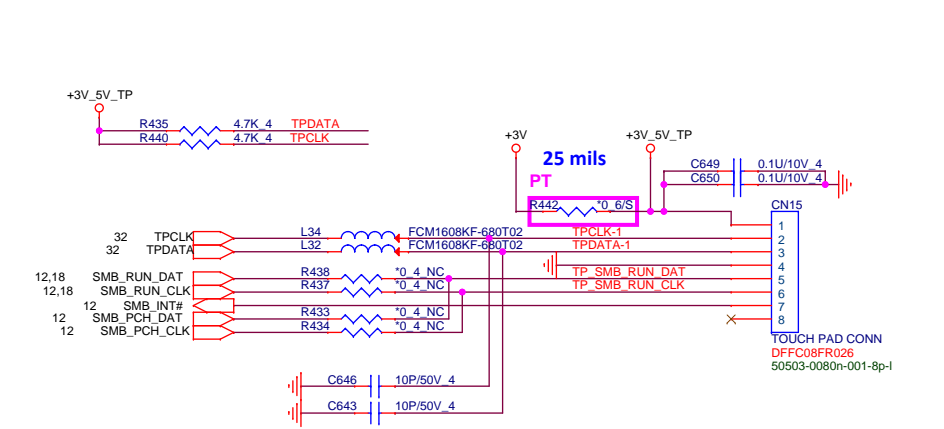
Keyboard Connector



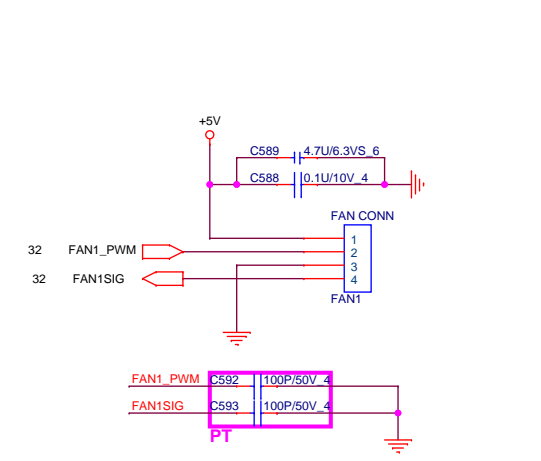
Green CLK



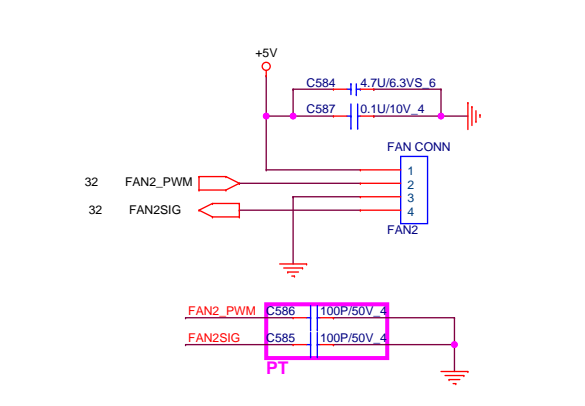
Touch Pad Connector

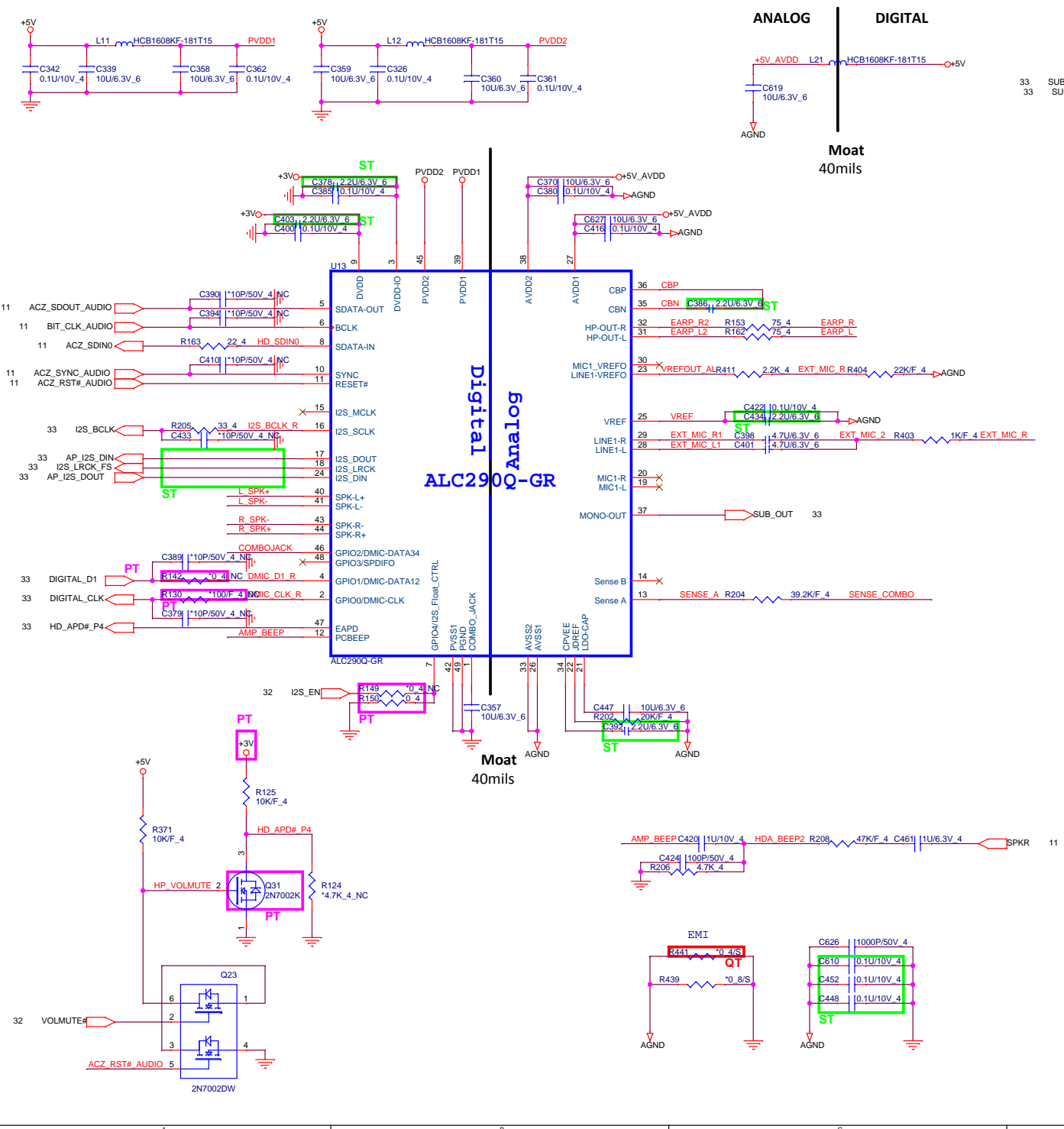


CPU FAN

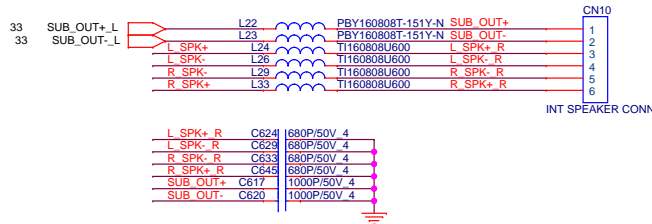


GPU FAN

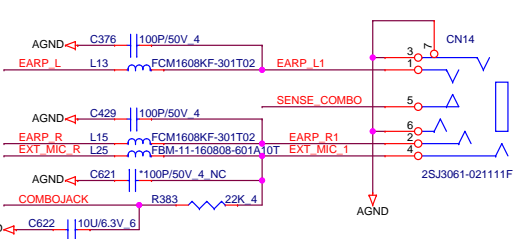
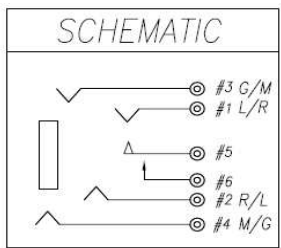
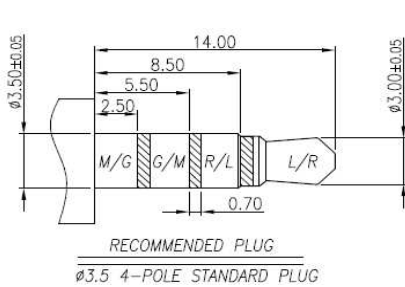




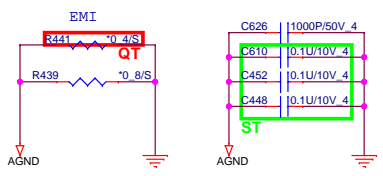
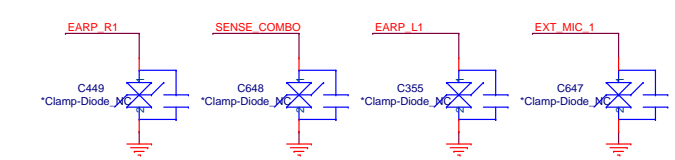
Int. Speaker



Audio Combo Jack

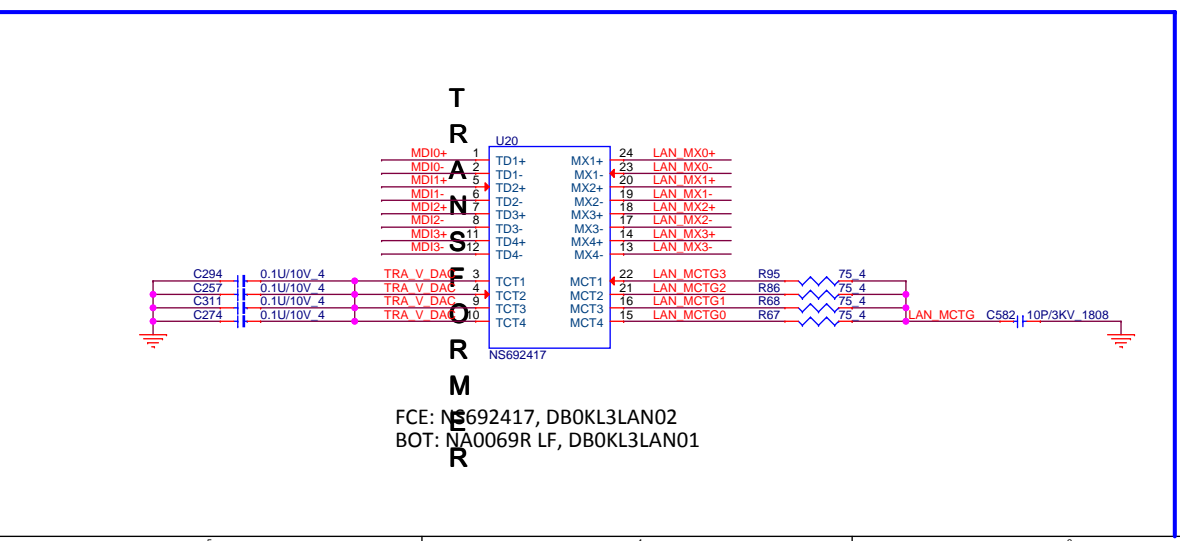
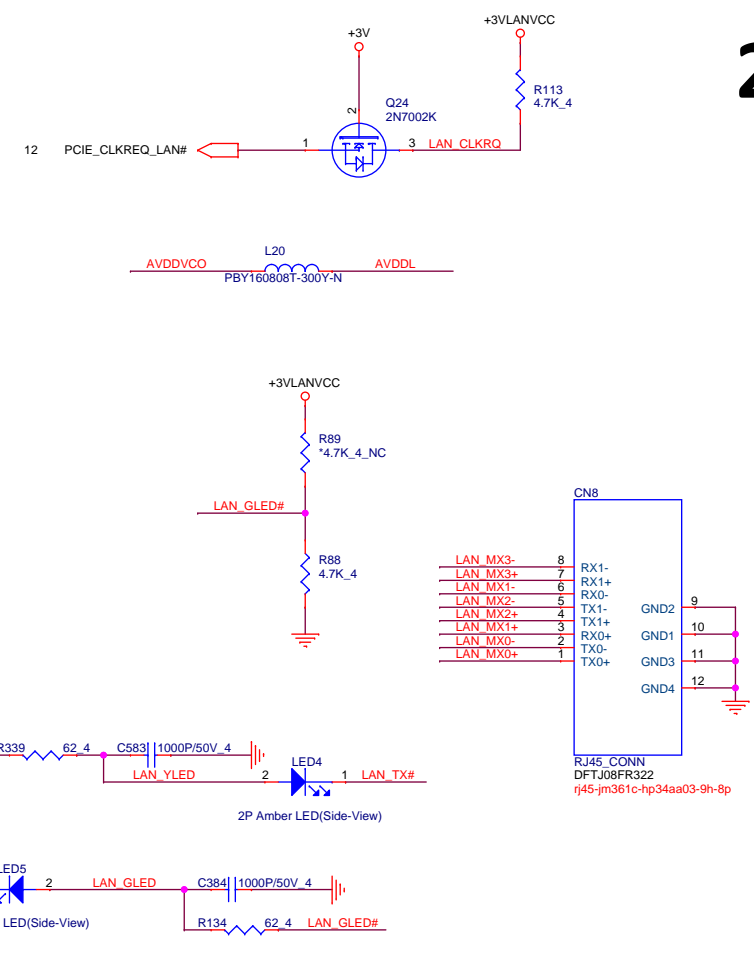
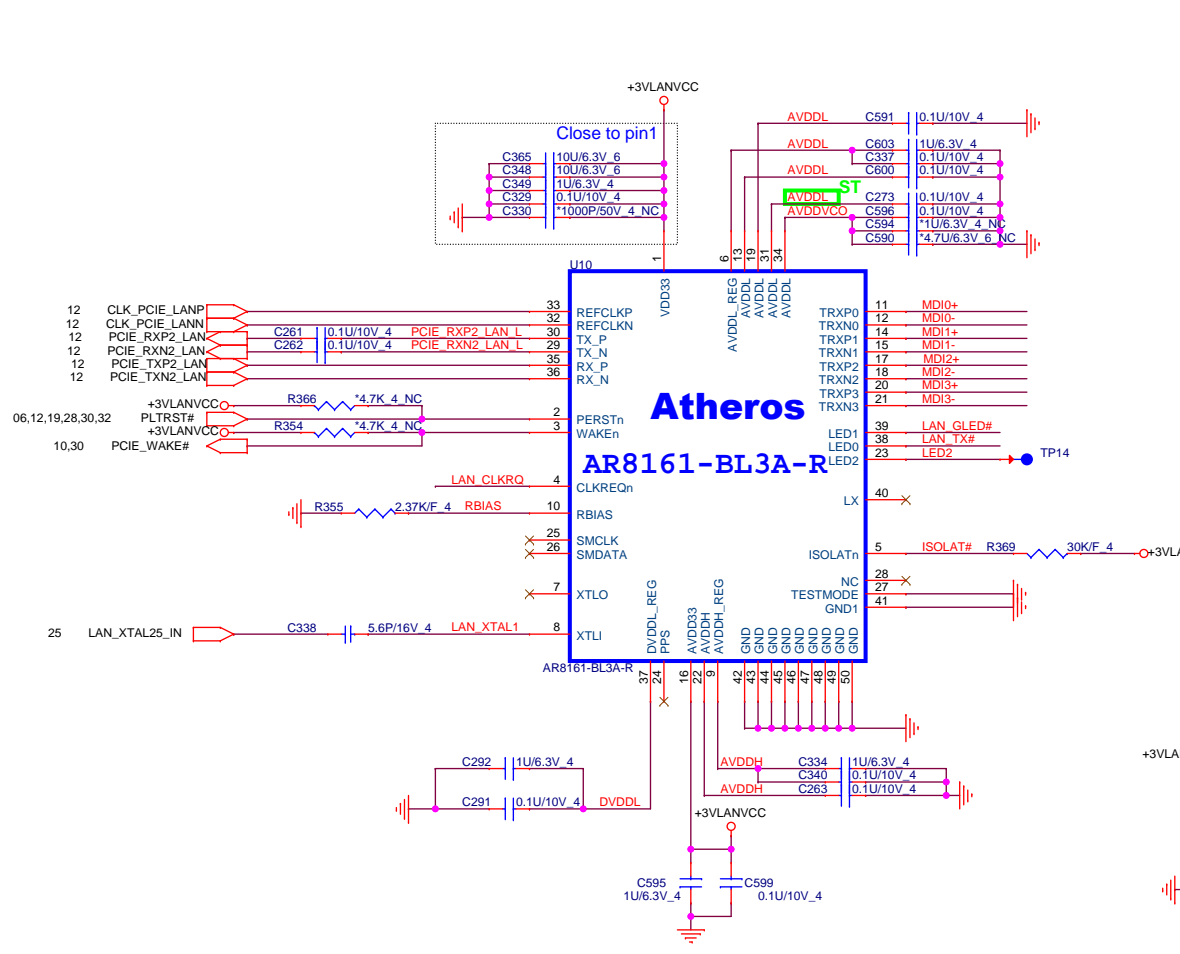


Audio Jack type:
Normal Open
Combo Jack (IPHONE)




Quanta Computer Inc.
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Size	Document Number	Audio Codec ALC290Q-GR	Rev 3A
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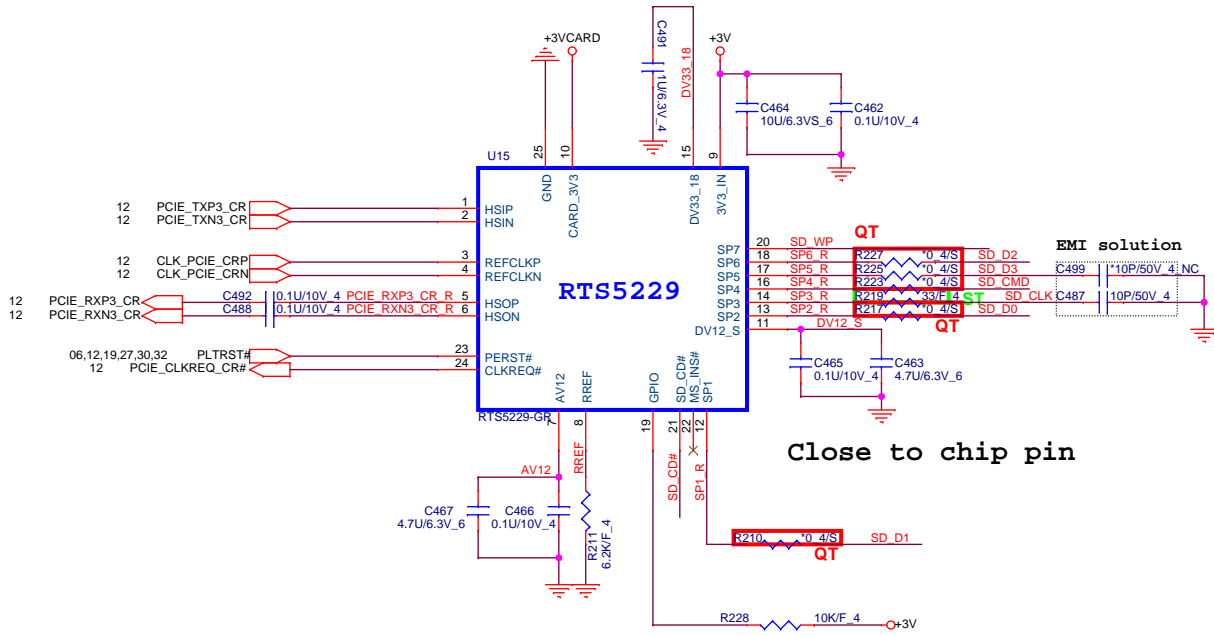


FCE: NS692417, DBOKL3LAN02
 BOT: NA0069R LF, DBOKL3LAN01

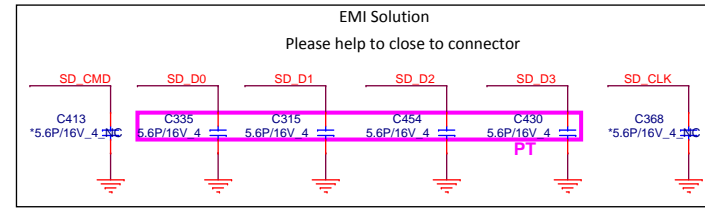


Quanta Computer Inc.
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Size	Document Number	Rev
	LAN Controller (Atheros_AR8161)	3A
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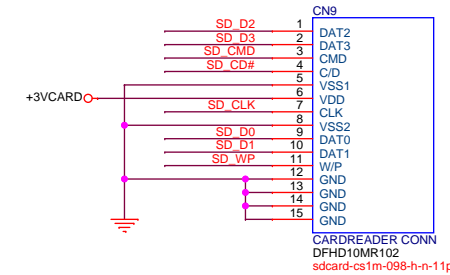
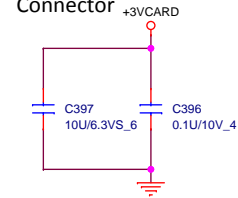


Share Pin

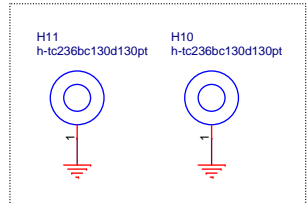


SD / MMC
CARD READER

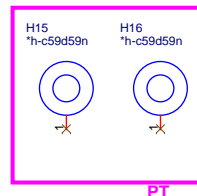
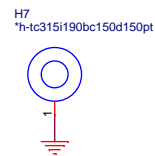
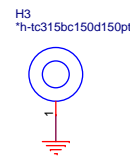
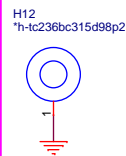
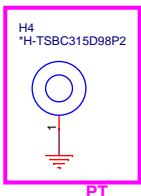
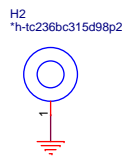
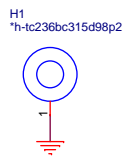
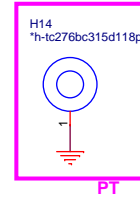
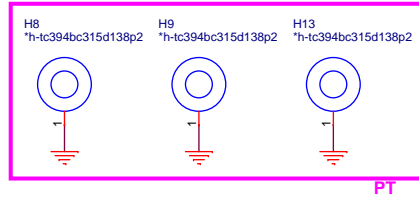
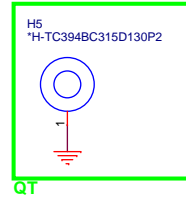
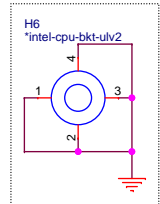
Place close to
Connector



Mini-PCIE



CPU BKT

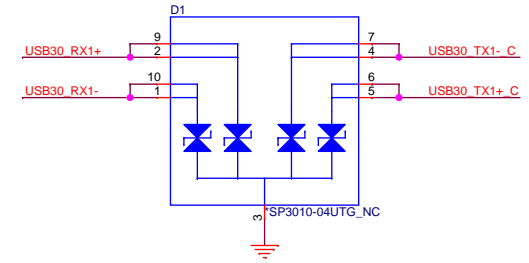
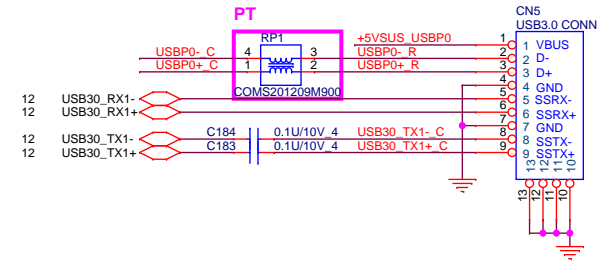
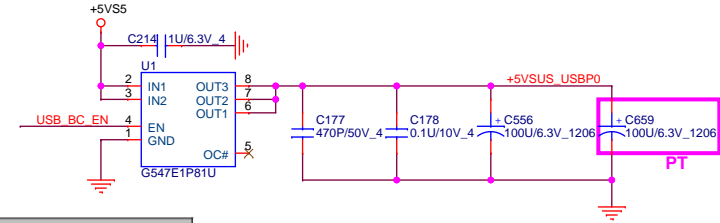
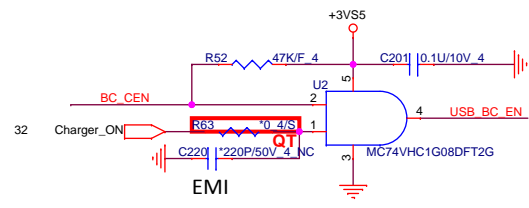
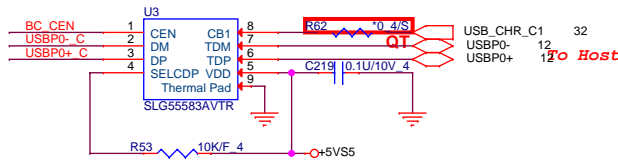


Charger USB

USB3.0/2.0 COMBO X 1

29

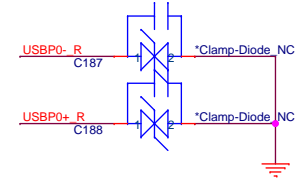
USB 3.0



CB	SELCDP	Function
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	80 charging with SDP only
1	1	80 charging with CDP or SDP only (depending on external device)

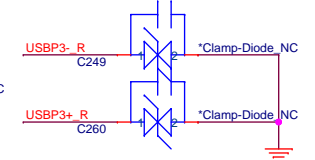
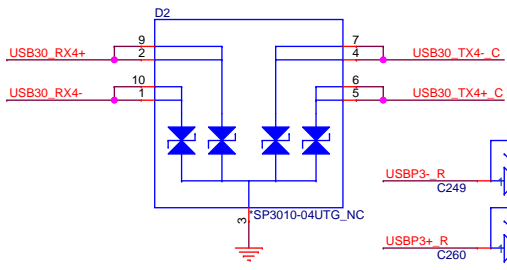
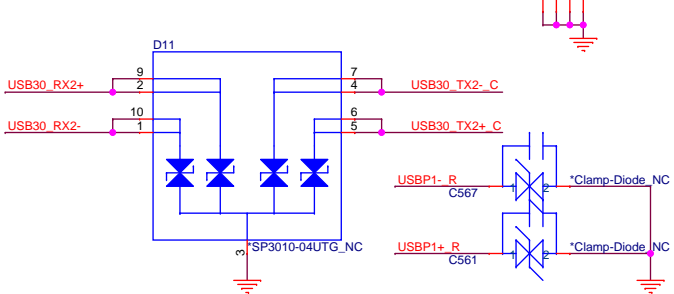
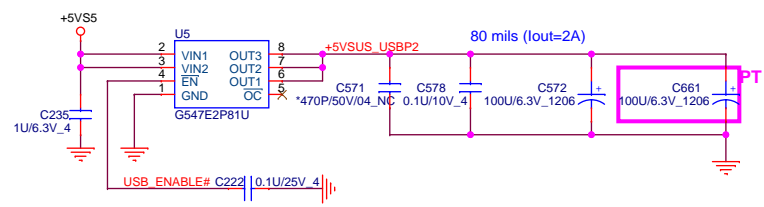
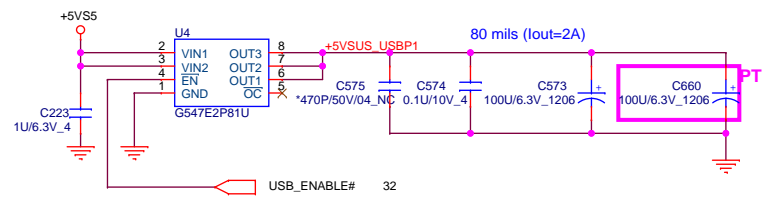
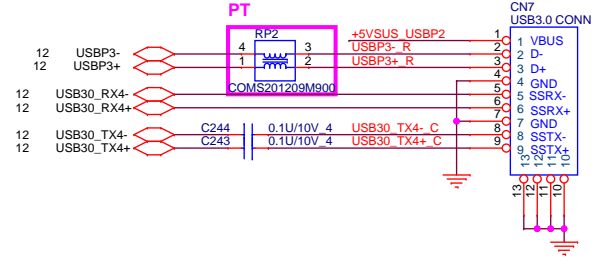
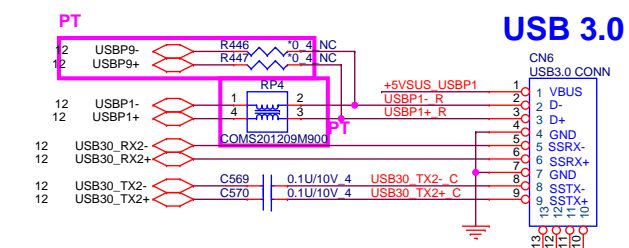
• USB Charge at S0 / S3 / S4 / S5 (Set by BIOS)

Current Battery Capacity	USB Charge (Set by BIOS)	S0		S3		S4/S5		EC wake up to read battery capacity from deep sleep mode	
		AC	DC	AC	DC	AC	DC	AC	DC
> battery level (20%)	Enable	CDP	CDP	DCP	DCP	DCP	DCP	No	Yes
	Disable (Default)	CDP	CDP	Off	Off	Off	Off	No	No
<= battery level (20%)	Enable	CDP	CDP	DCP	Off	DCP	Off	No	No
	Disable (Default)	CDP	CDP	Off	Off	Off	Off	No	No




USB3.0/2.0 COMBO X 2

USB 3.0



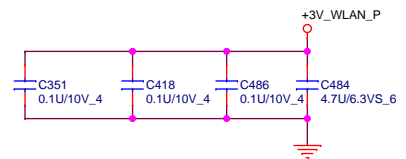
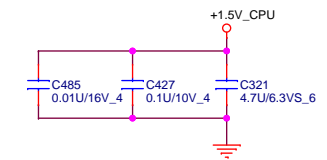
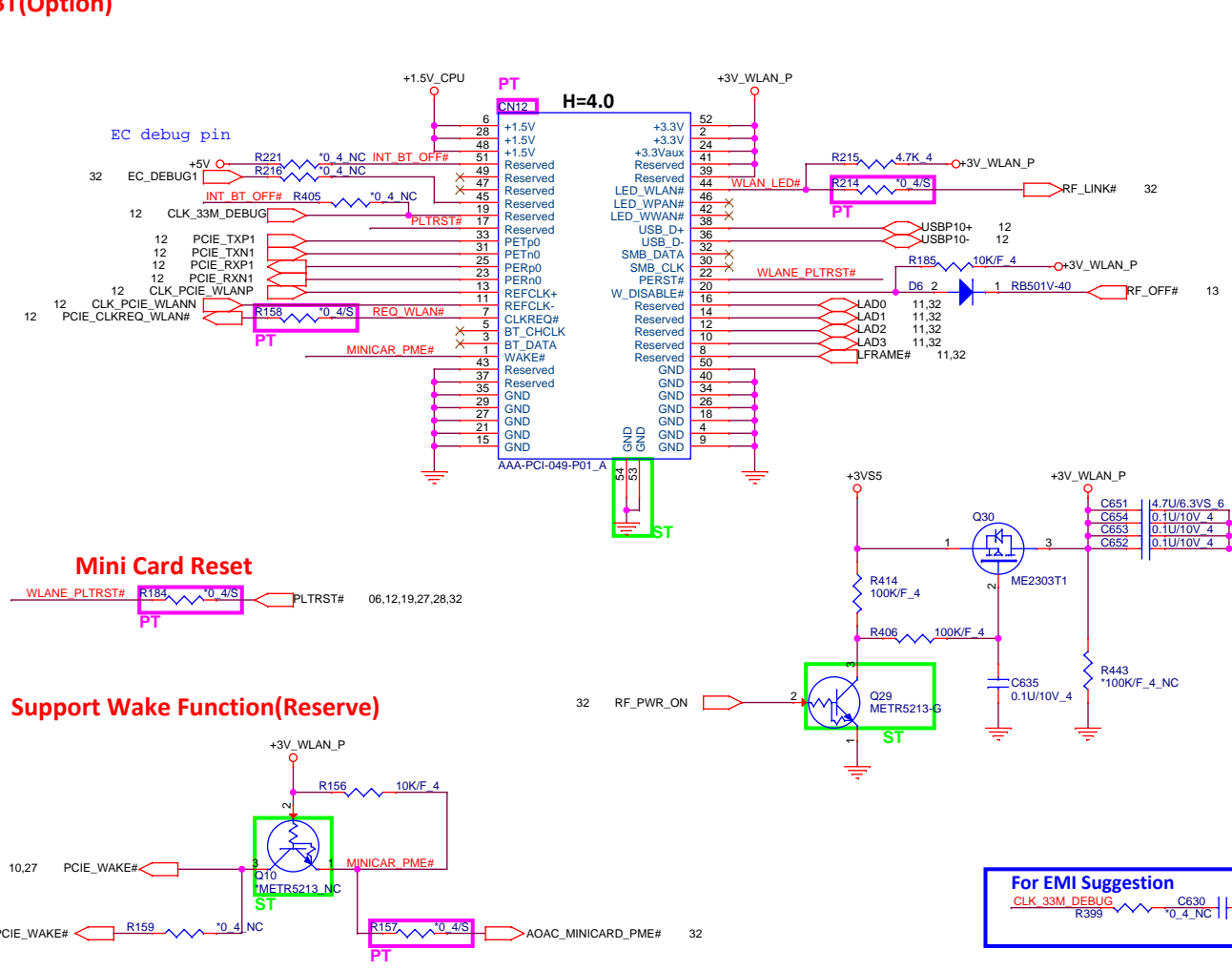
14,31,35,36,37,38,40,42,44 +5VS5



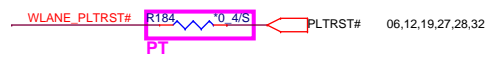
Quanta Computer Inc.
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Size	Document Number	Rev
	USB3/USB Charger	3A
Date:	Friday, November 02, 2012	Sheet 29 of 46

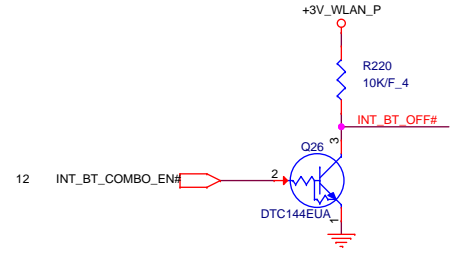
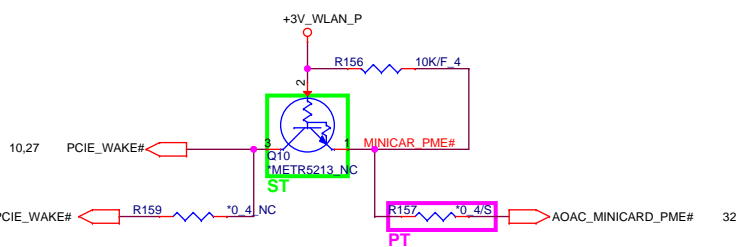
Mini Card
WLAN/BT(Optional)



Mini Card Reset



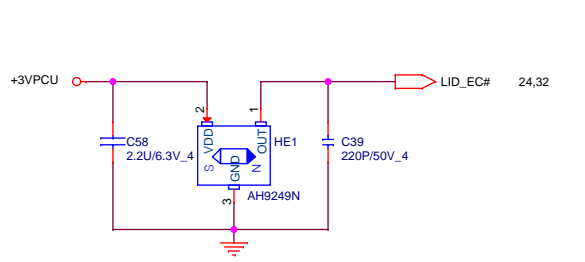
Support Wake Function(Reserve)



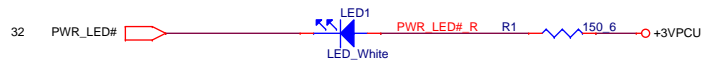
LGE mini-pcie power status		
WLAN	Bluetooth	+3V_WLAN_P
Radio-ON	Radio-ON	Power-ON
Radio-ON	Radio-OFF	Power-ON
Radio-OFF	Radio-ON	Power-ON
Radio-OFF	Radio-OFF	Power-OFF

For EMI Suggestion
 CLK_33M_DEBUG R399 *0.4_NC || *33P/50V_4

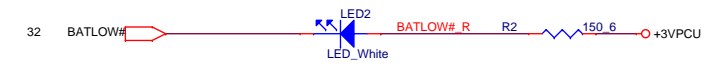
LED Status



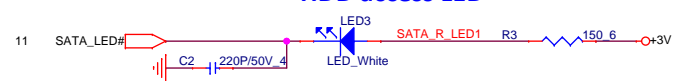
System status LED



Battery charger LED



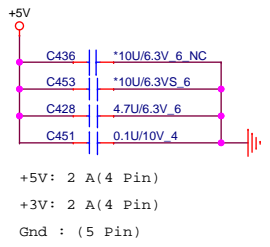
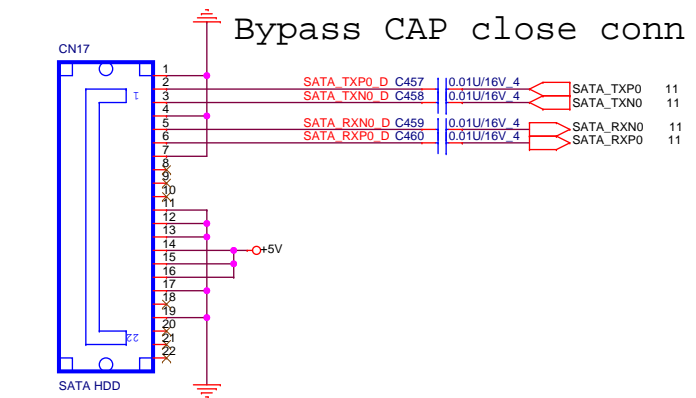
HDD access LED



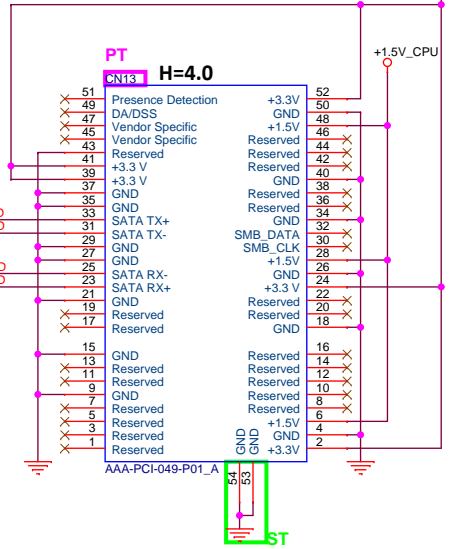
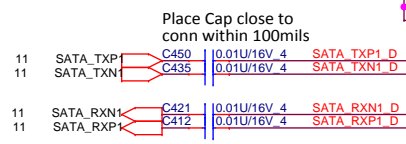
Quanta Computer Inc.
 PROJECT : JW8

Size	Document Number	Rev
	WLAN/BT/LED	3A
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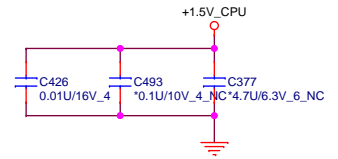
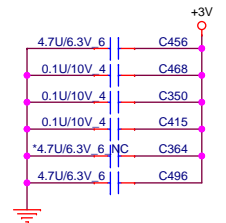
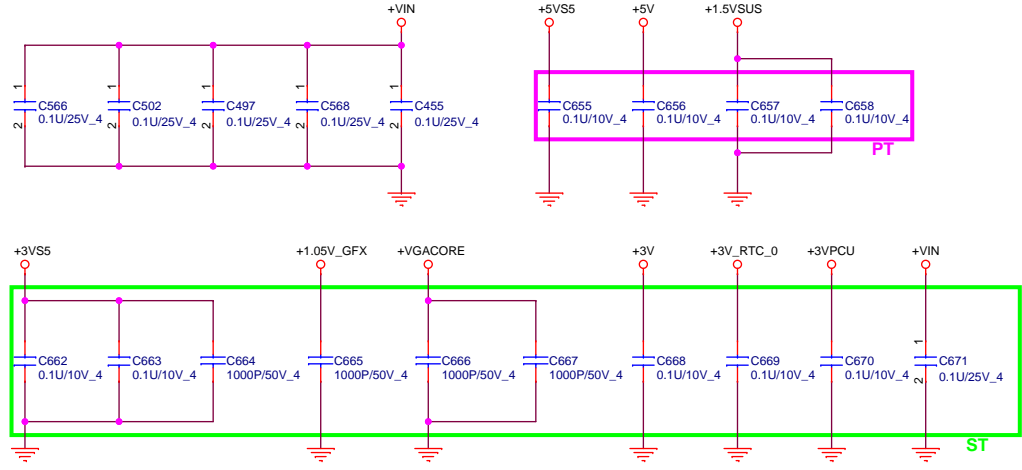
SATA HDD Connector

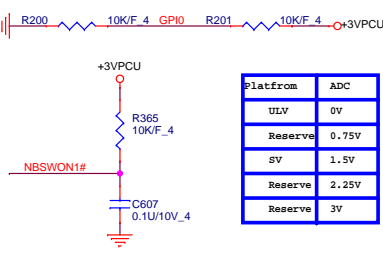
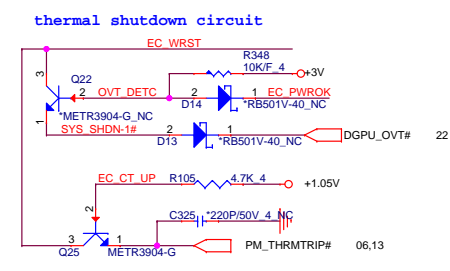
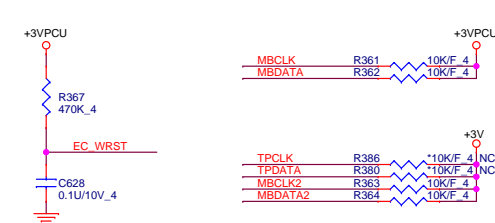
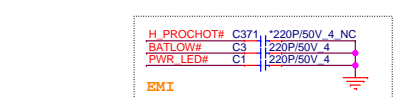
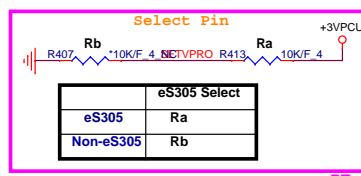
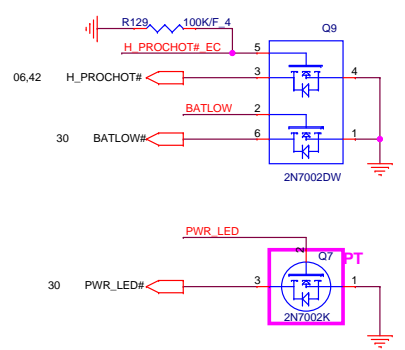
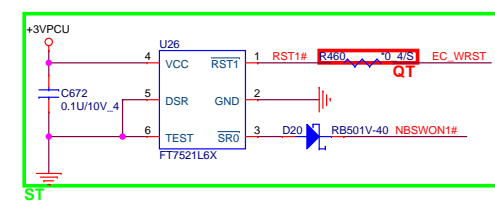
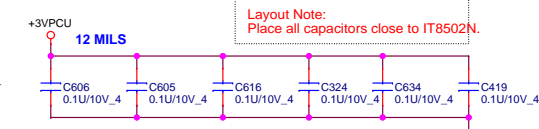
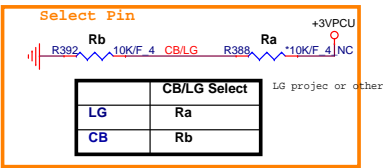
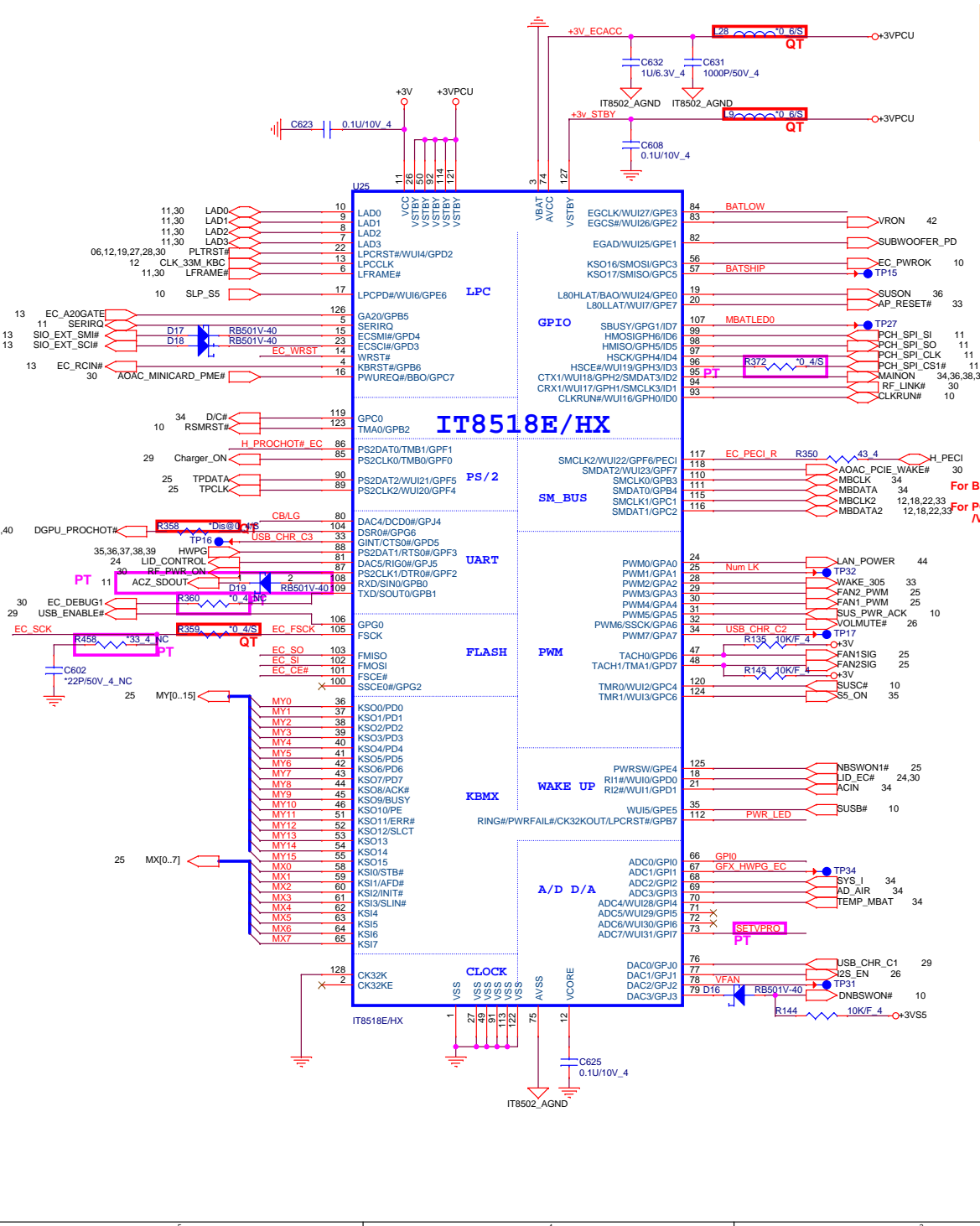


mSATA

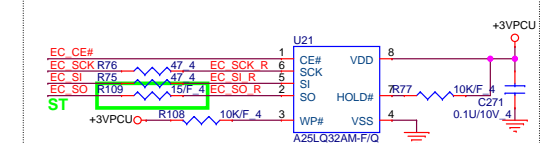


EMI





Vender	Size	P/N
AMIC	4MB	AKE39F-0800 (A25LQ32AM-F/Q)
GGD	4MB	AKE39GN0Q00 (GD25Q32BSIGR)



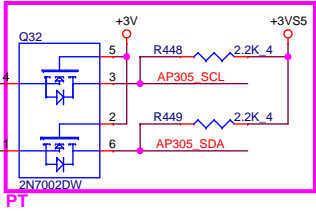
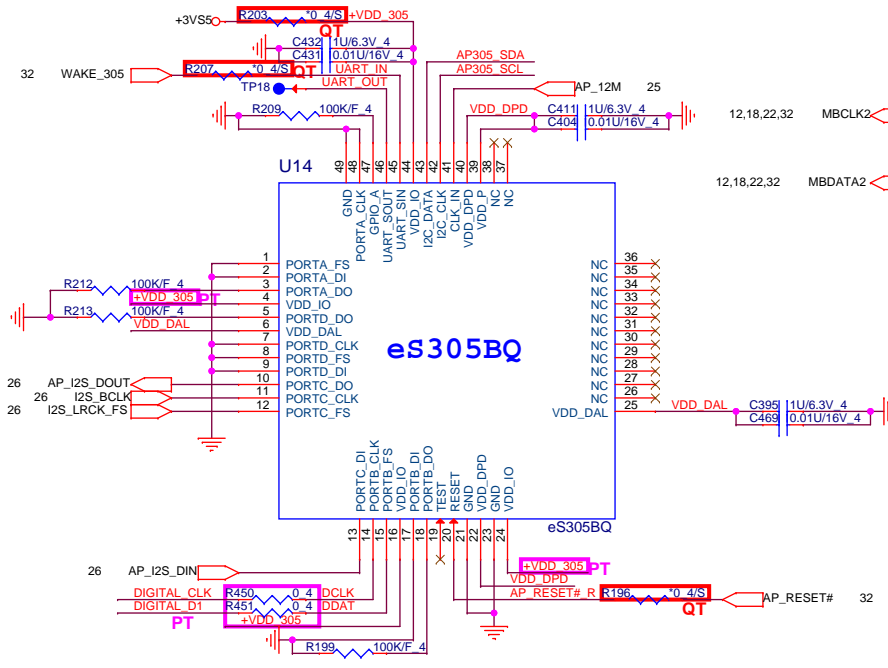
Quanta Computer Inc.

PROJECT : JW8

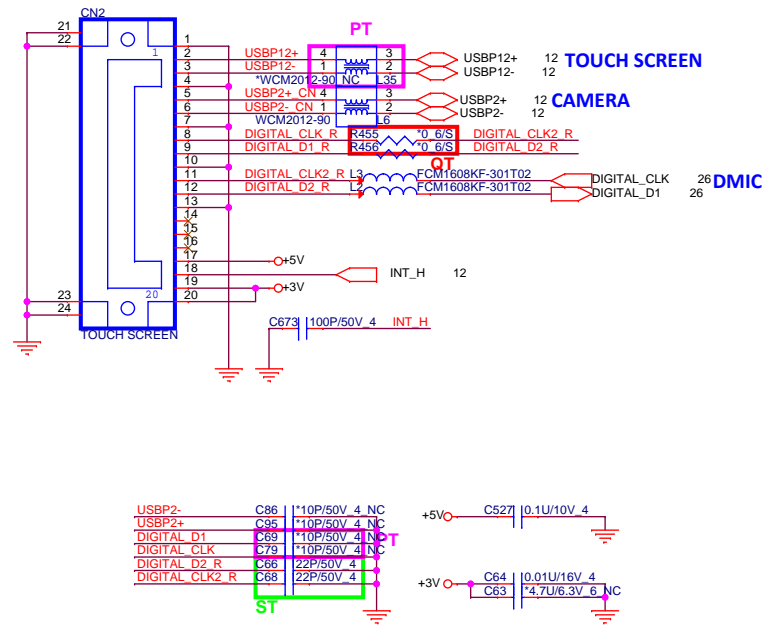
Size Document Number
Embedded Controller (ITE_IT8518) Rev 3A

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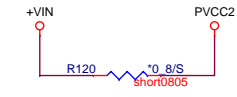
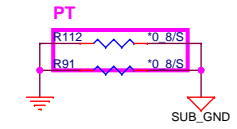
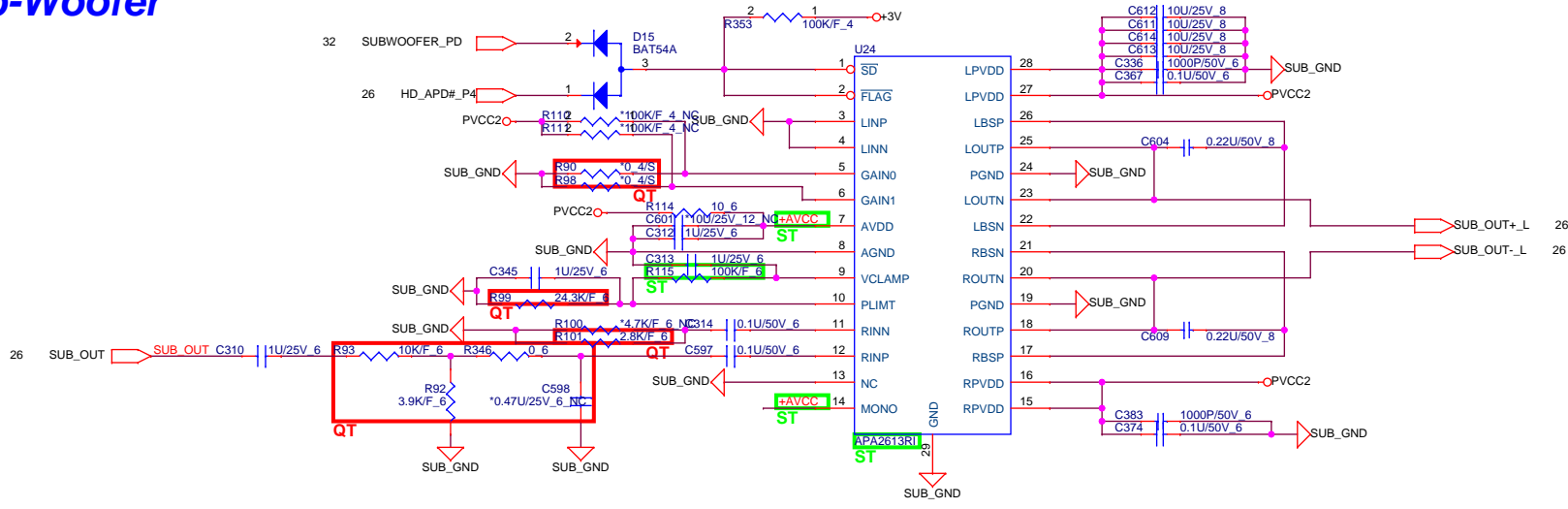
Audio Processor



Touch Screen




Sub-Woofer



GAIN1	GAIN0	dB
0	0	20
0	1	26
1	0	32
1	1	36

ANC: APA2613RI-TRG, AL002613K00
 TIC: TPA3111D1PWPR, AL003111K00



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Size	Document Number	Rev
	AudioDSP/TouchScreen/Subwoofer	3A
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TOP DC JACK
90W/4.75A

Place this ZVS close to
idea diode

Do Not add test point on BATDIS_G signal

Kelvin Connections for the
Current-Sense Resistors

Place this ZVS close to
Far-Far away +VIN

Parallel routing

Place this cap
close to EC

include charger boost function

Using Kelvin connection
for layout

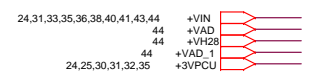
Place this cap
close to IC

Place this cap
close to EC

EMI Suggestion

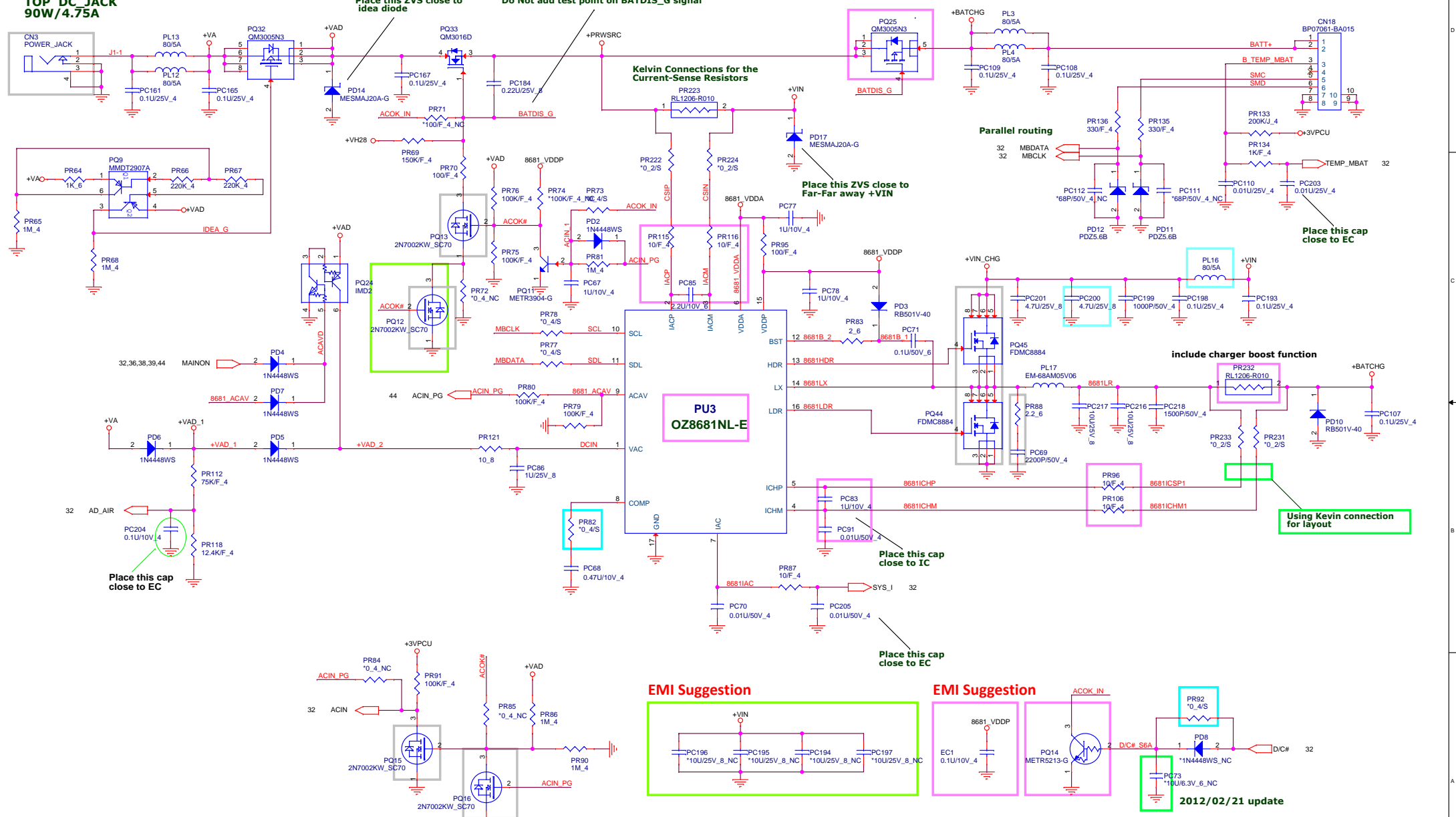
EMI Suggestion

2012/02/21 update



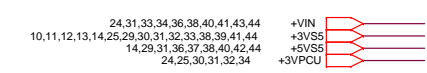
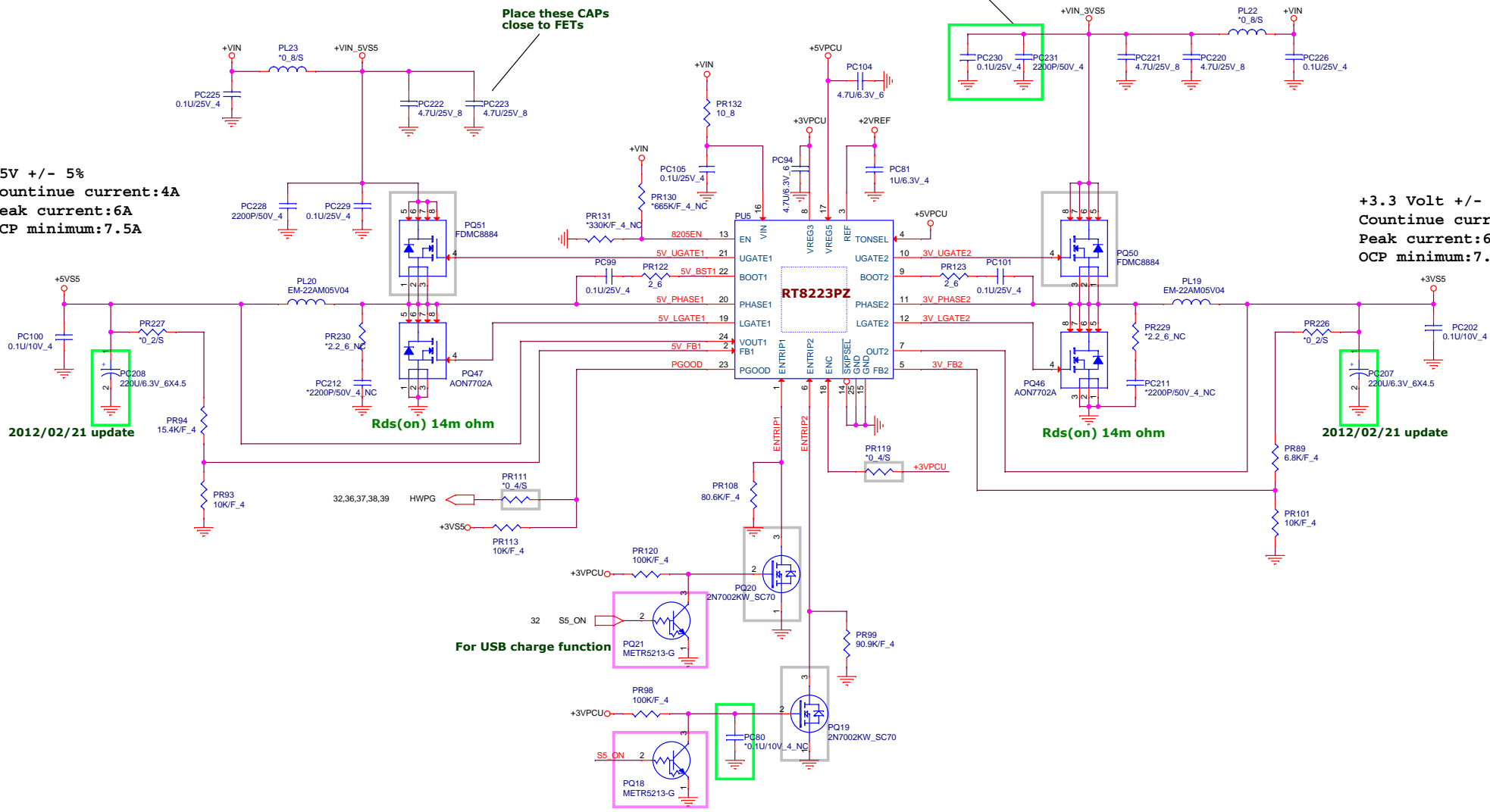
Quanta Computer Inc.
PROJECT : JW8

Size	Document Number	Rev
	Charger (OZ8681)	3A
Date:	Friday, November 02, 2012	Sheet 34 of 46

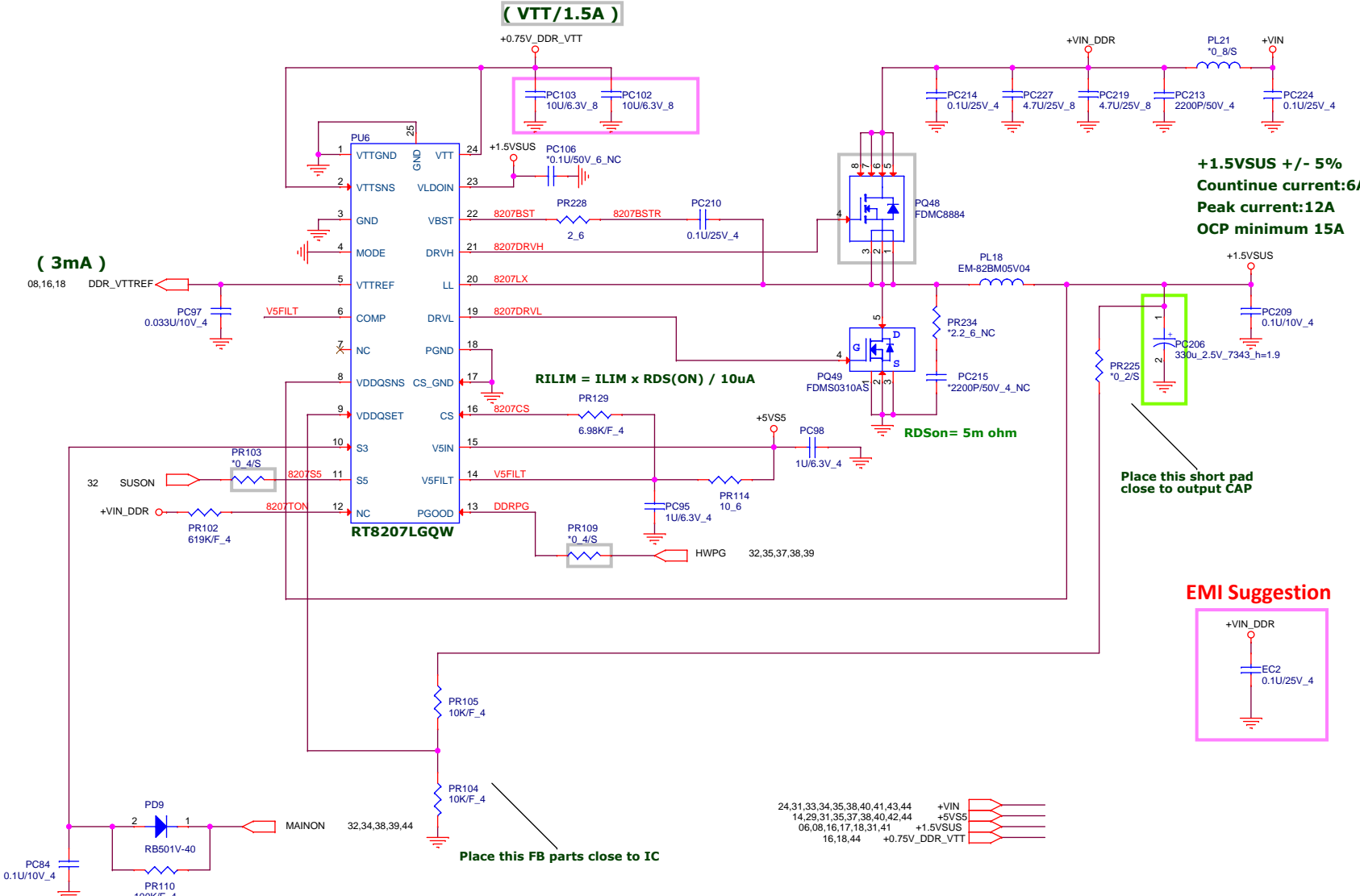


+5V +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A



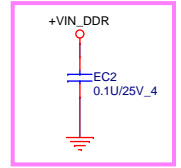
<p>Quanta Computer Inc. PROJECT : JW8</p>		Rev
		3A
Date:	Friday, November 02, 2012	Sheet
3/5VS5 (RT8223P)		46



+1.5VSUS +/- 5%
Countinue current:6A
Peak current:12A
OCP minimum 15A

Place this short pad close to output CAP

EMI Suggestion

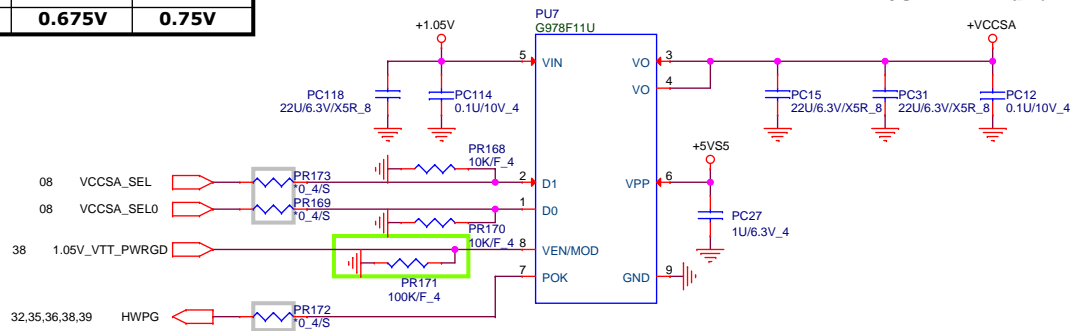


Place this FB parts close to IC

- 24,31,33,34,35,38,40,41,43,44 +VIN
- 14,29,31,35,37,38,40,42,44 +5VS5
- 06,08,16,17,18,31,41 +1.5VSUS
- 16,18,44 +0.75V_DDR_VTT

D0	D1	SV +VCCSA	ULV +VCCSA
0	0	0.9V	0.9V
0	1	0.8V	0.85V
1	0	0.725V	0.775V
1	1	0.675V	0.75V

+VCCSA Volt +/- 5%
 Countinue current:4A
 Peak current:6A
 OCP minimum:7A

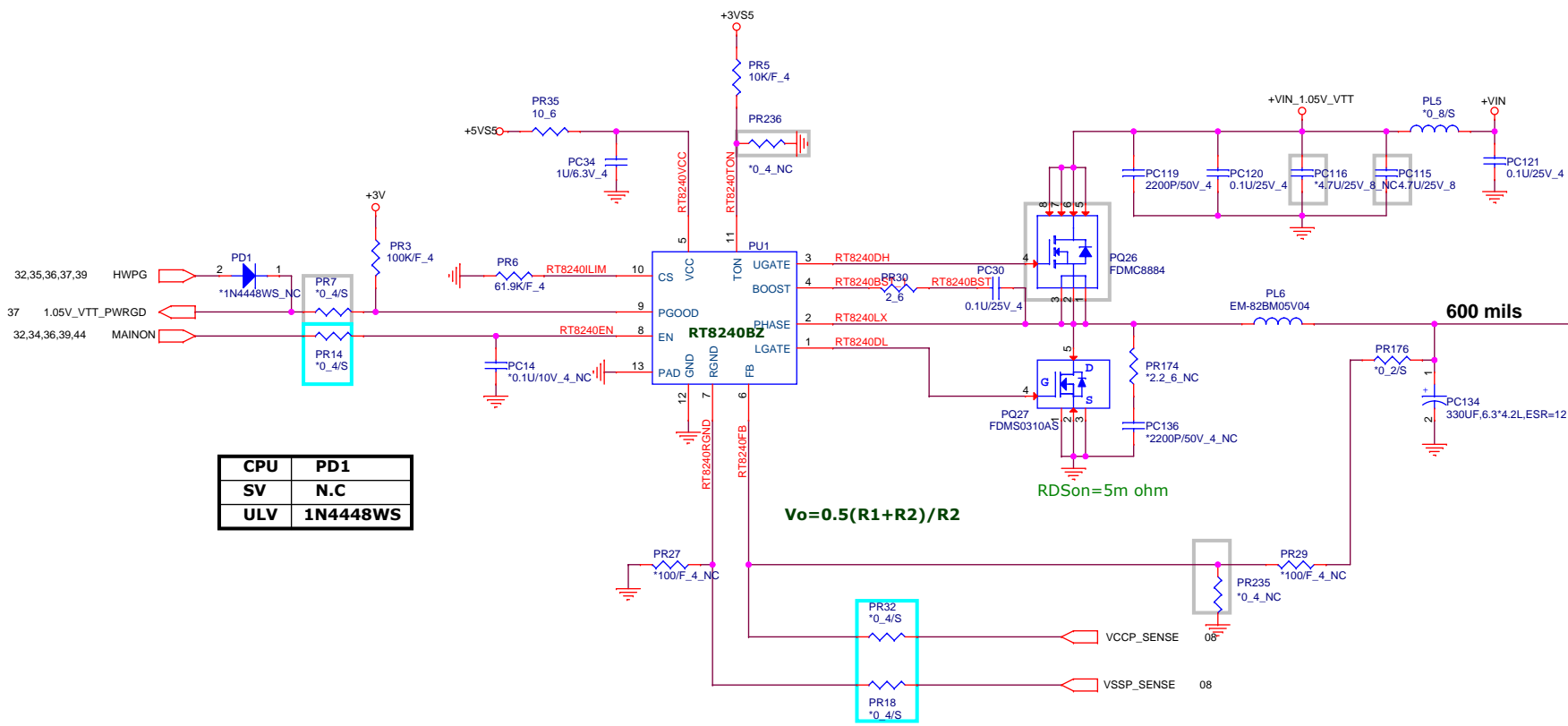


CPU	PR171
SV	100K/F_4
ULV	N.C



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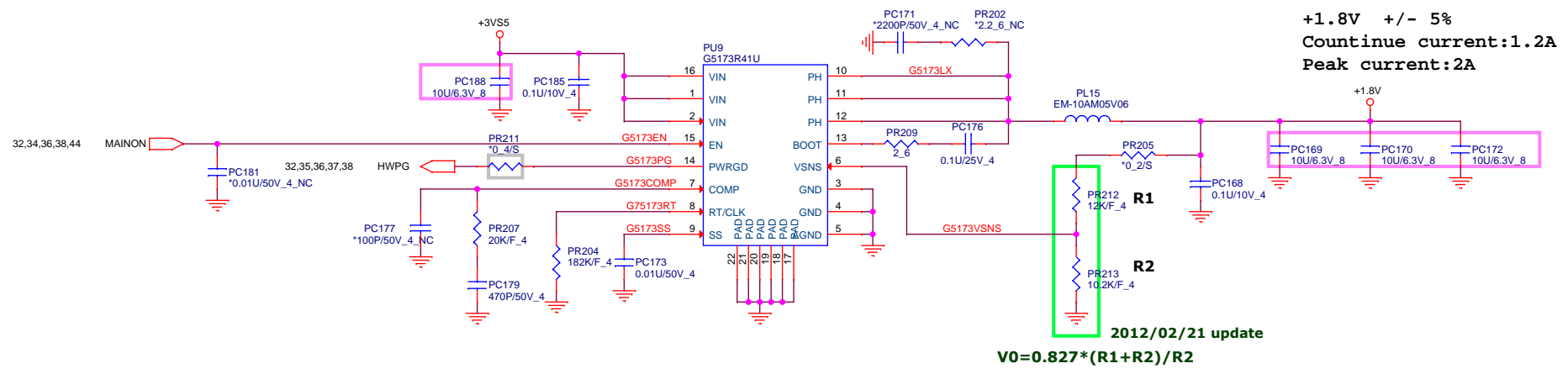
+1.05V_VTT +/- 5%
Countinue current:10A
Peak current: 12A
OCp minimum: 14.5A

CPU	PD1
SV	N.C
ULV	1N4448WS

$$V_o = 0.5(R1 + R2) / R2$$

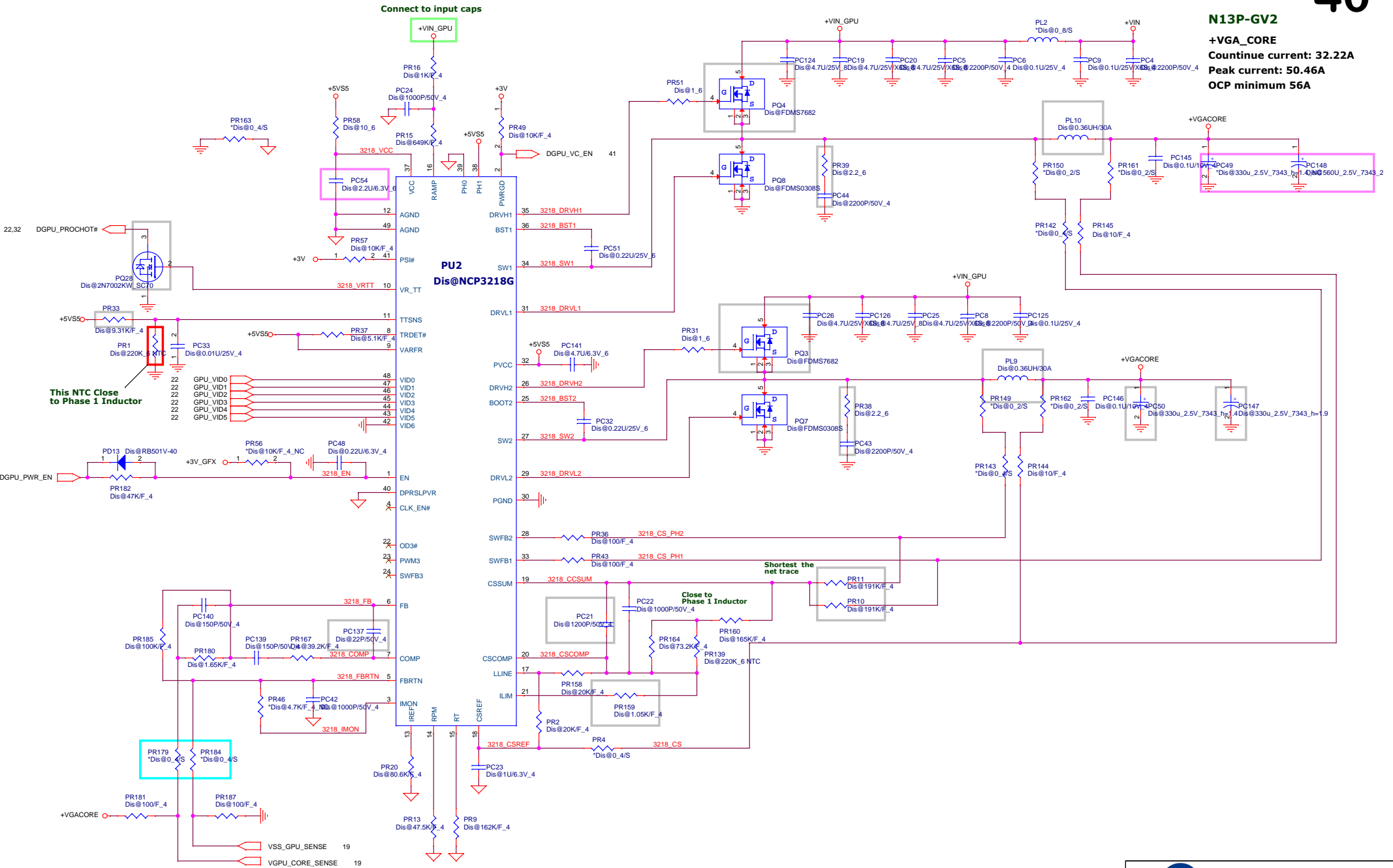
RDson=5m ohm

600 mils



N13P-GV2

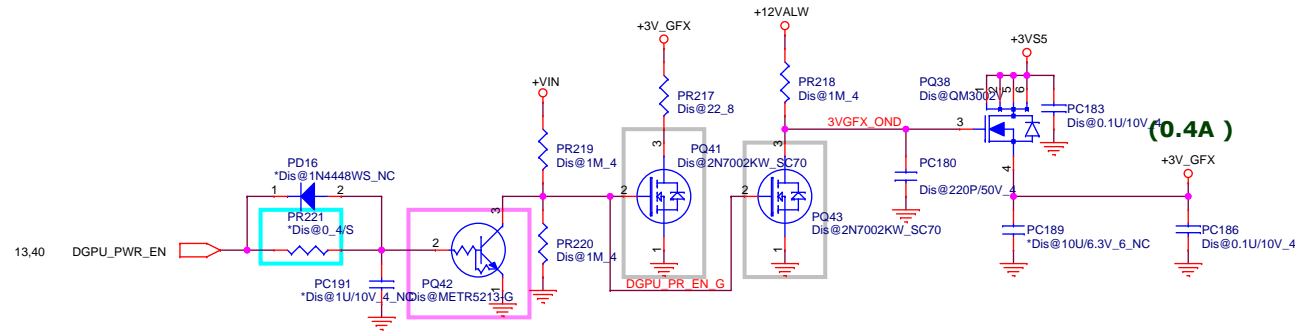
+VGA_CORE
Continue current: 32.22A
Peak current: 50.46A
OCP minimum 56A



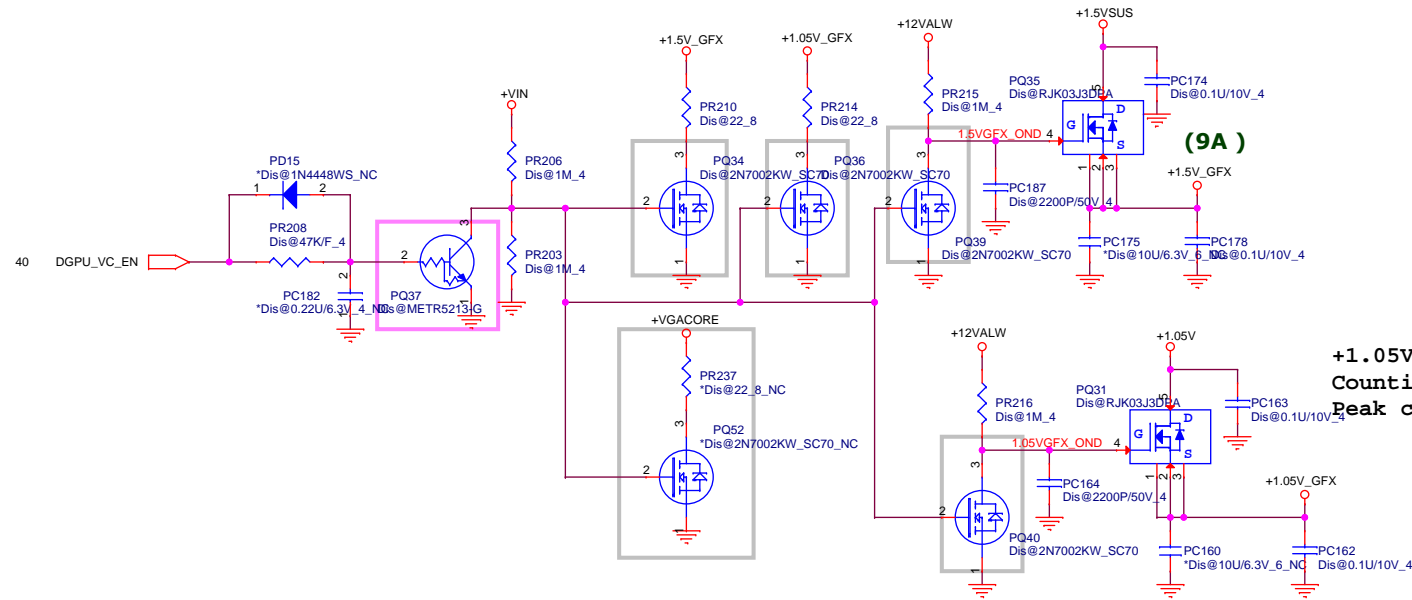
Quanta Computer Inc.
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Size	Document Number	Rev
	+VGA CORE (NCP3218G)	3A
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06,08,16,17,18,31,36	+1.5VSUS	
10,11,12,13,14,25,29,30,31,32,33,35,36,39,44	+3VS5	
19,21,22,40	+3V_GFX	
20,21,22,23	+1.5V_GFX	
19,20,21,31	+1.05V_GFX	
44	+12VALW	
06,08,10,11,12,14,25,32,37,38,42	+1.05V	




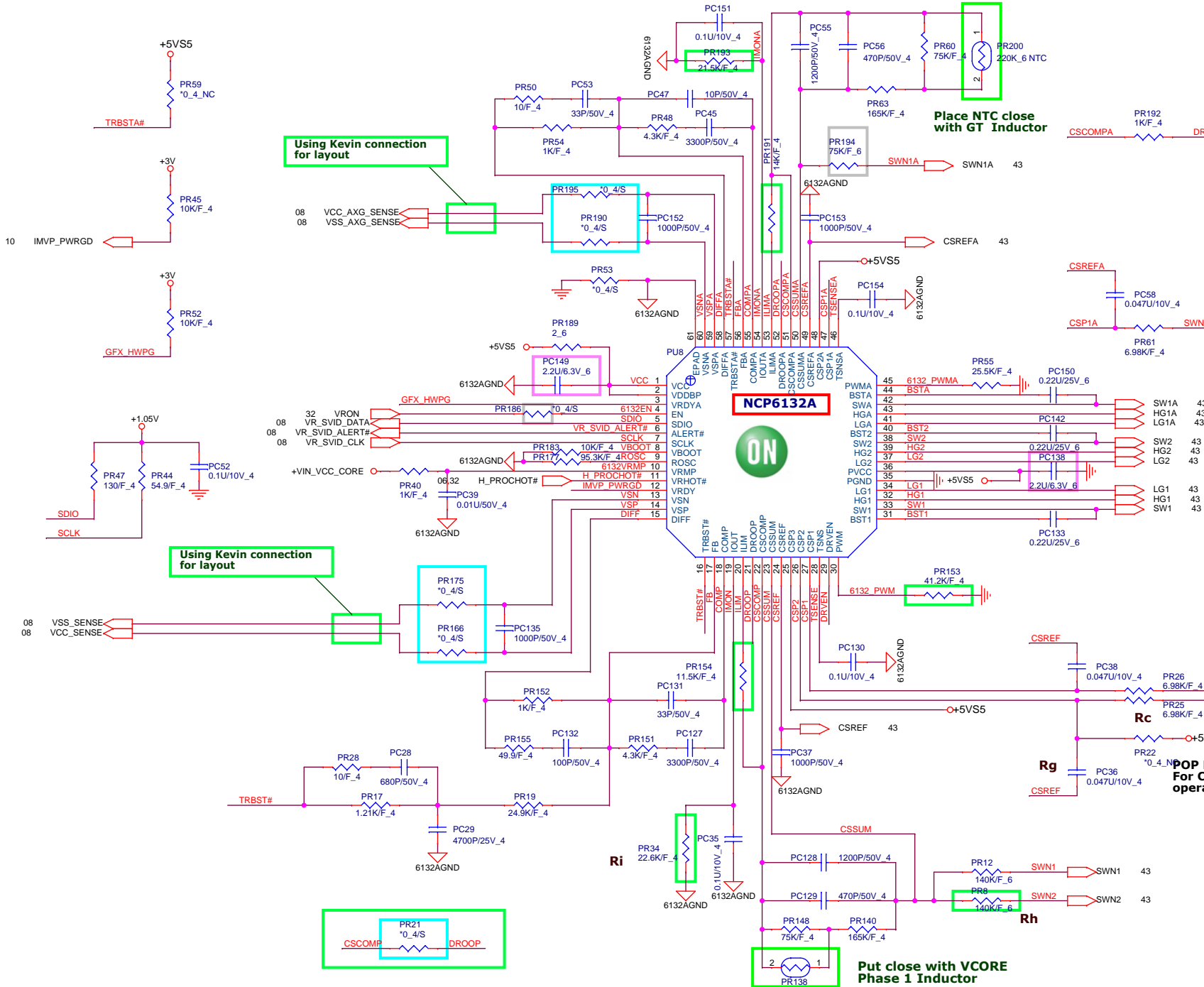
(0.4A)



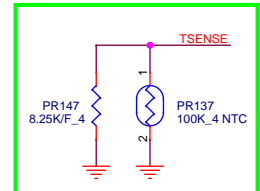
(9A)

+1.05V +/- 3%
 Countinue current:2.1A
 Peak current:3A

 Quanta Computer Inc. PROJECT : JW8		Rev 3A
+VGA POWER		
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ULV Mode N.C
 PR25, PC36, PC142, PR8



+VCC_CORE (ULV 17W)

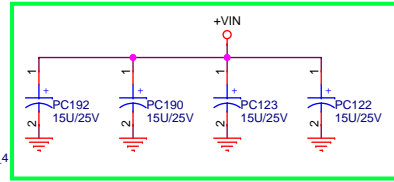
TDC : 25A
Peak current: 33A
Load Line : -2.9mV/A

Countinue current:33A
Peak current: 53A
Load Line : -1.9mV/A

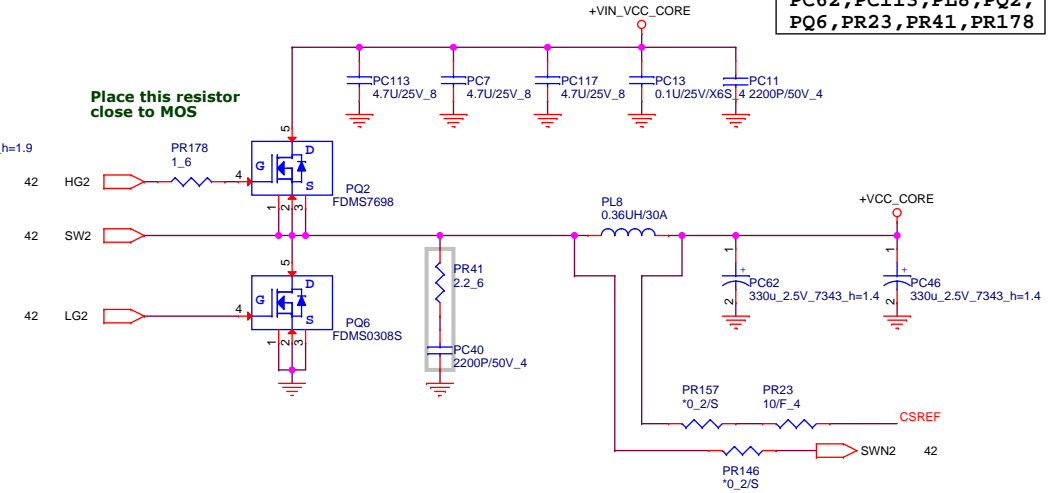
ULV Mode N.C

**PC7,PC11,PC13,PC40,
 PC62,PC113,PL8,PQ2,
 PQ6,PR23,PR41,PR178**

Place this resistor close to MOS

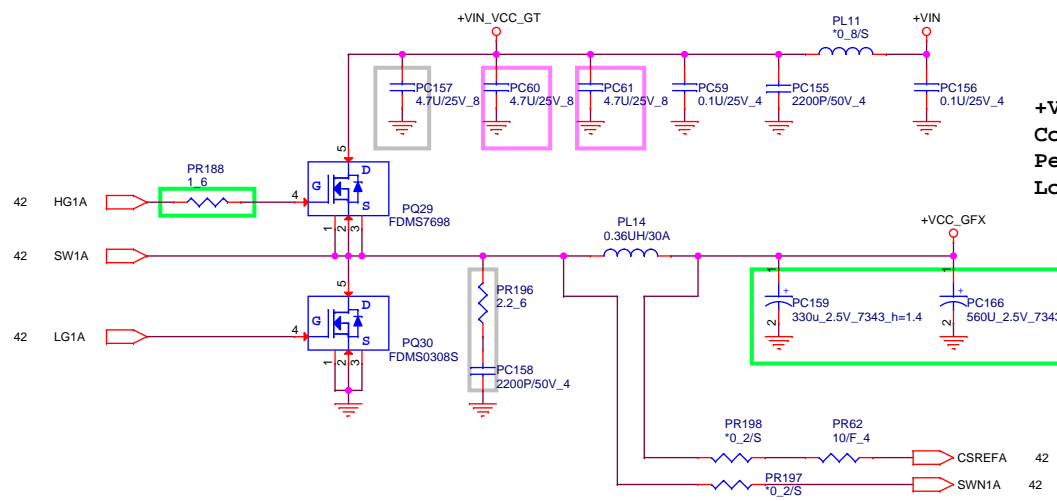
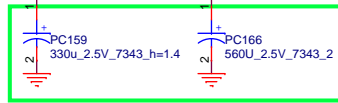


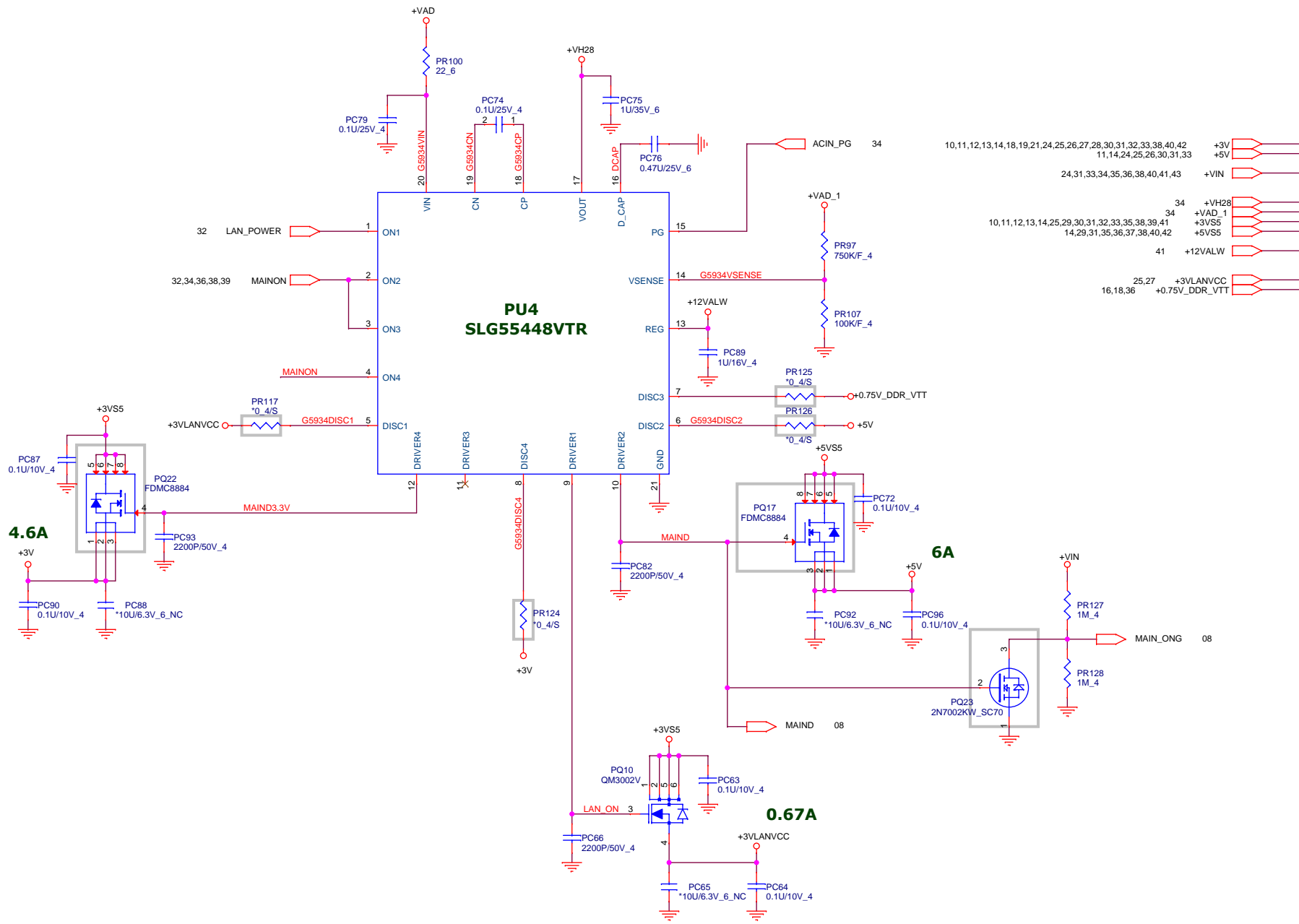
Place this resistor close to MOS




+VCC_GFX

Countinue current:21.5A
Peak current: 33A
Load Line : -3.9mV/A





- 10,11,12,13,14,18,19,21,24,25,26,27,28,30,31,32,33,38,40,42 +3V
- 11,14,24,25,26,30,31,33 +5V
- 24,31,33,34,35,36,38,40,41,43 +VIN
- 34 +VH28
- 34 +VAD_1
- 10,11,12,13,14,25,29,30,31,32,33,35,38,39,41 +3VS5
- 14,29,31,35,36,37,38,40,42 +5VS5
- 41 +12VALW
- 25,27 +3VLANVCC
- 16,18,36 +0.75V_DDR_VTT

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	History	3A
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