

# Compal Confidential

## QBL60 Schematics Document

AMD Sabine

APU Llano / Hudson M2\_M3 / Vancouver Whistler

UMA only / PX Muxless with BACO

2010-04-25

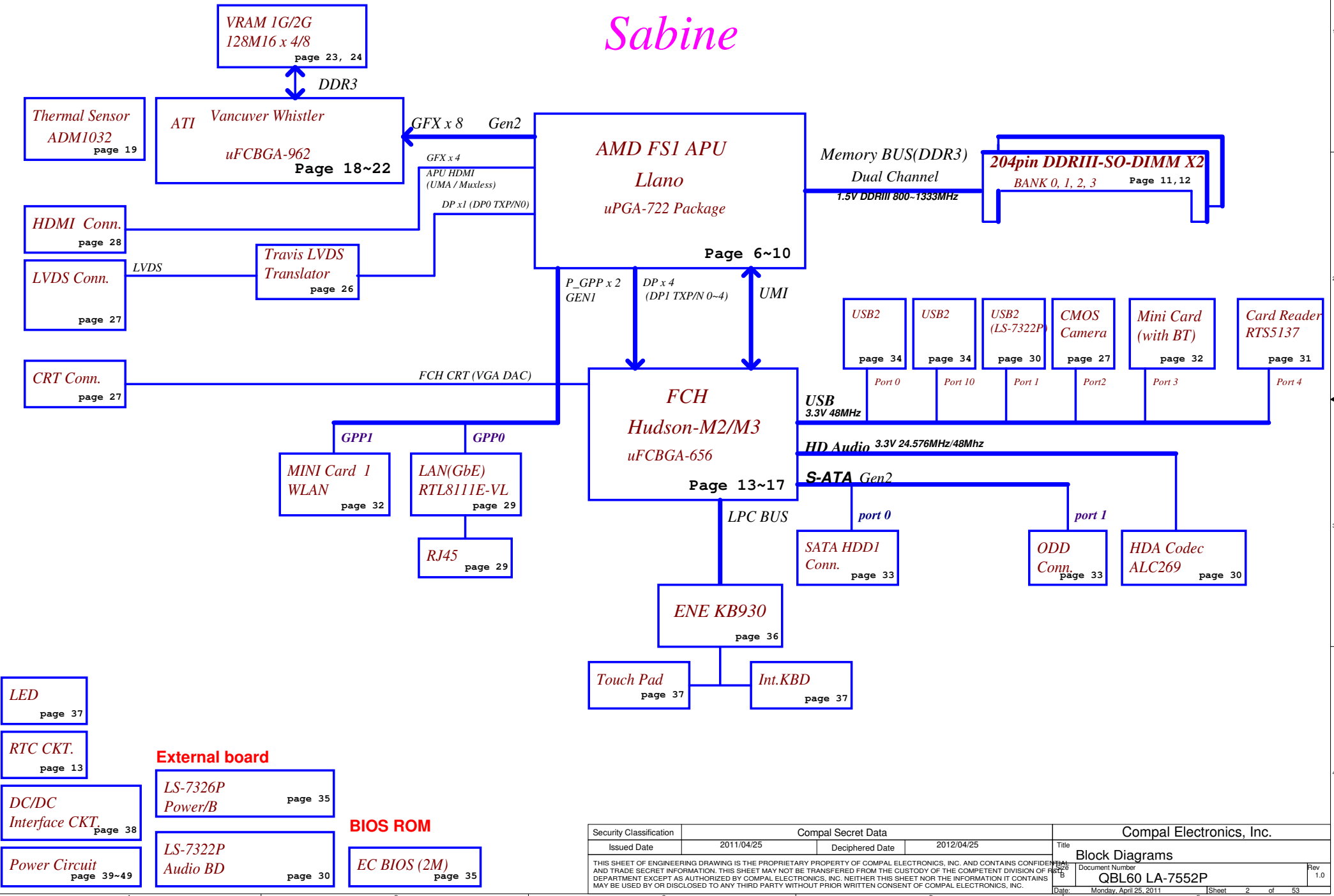
LA-7552P REV: 1.0

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Issued Date	2011/04/25	Deciphered Date	2012/04/25	Title	Cover Page
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# Compal Confidential

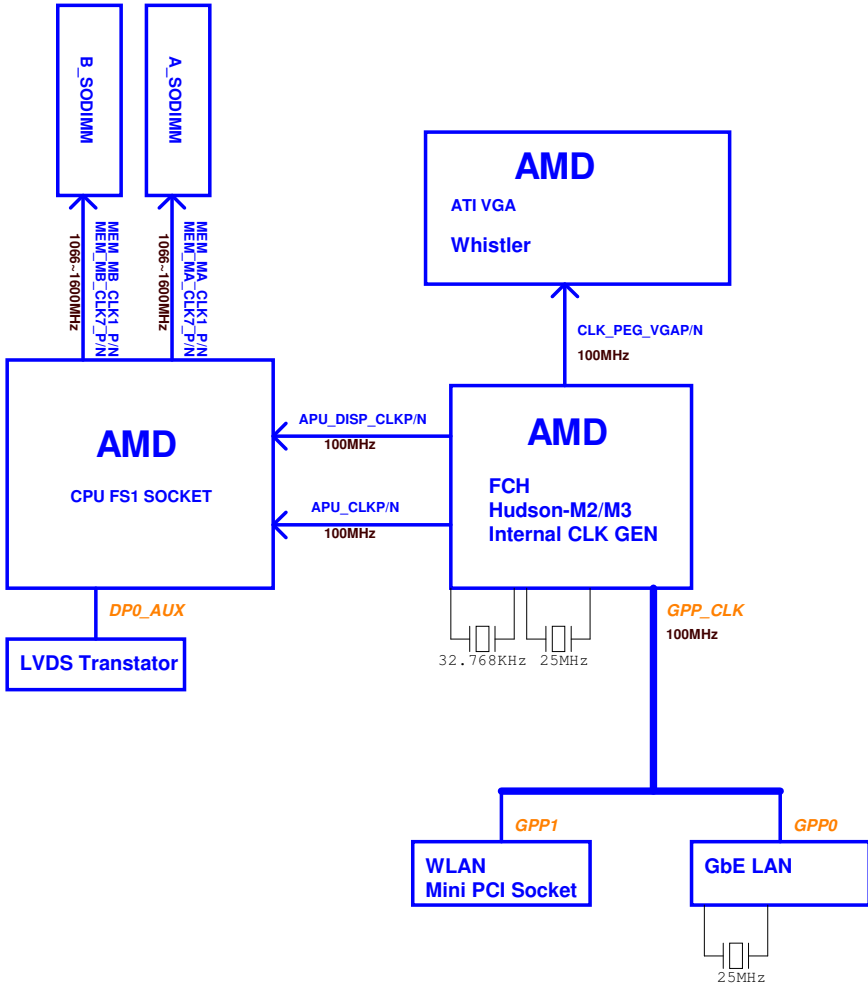
Model Name : QBL60

## Sabine

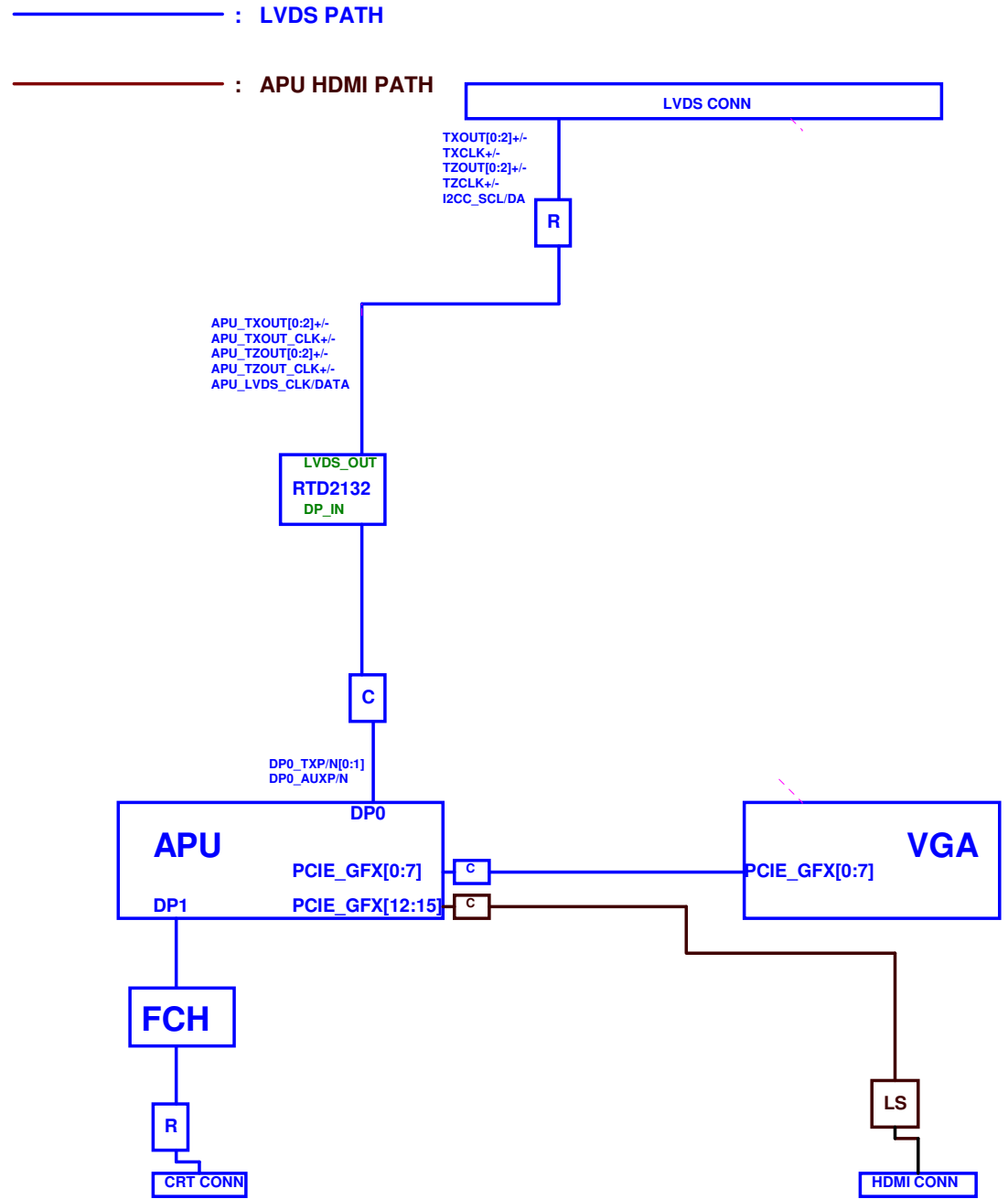


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# CLOCK DISTRIBUTION



# DISPLAY DISTRIBUTION



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## Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	ON	OFF
+1.0VSG	1.0V switched power rail for VGA	ON	OFF	OFF
+1.1ALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.2VS	1.2V switched power rail for APU	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VSG	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+LAN_IO	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

x = 1 is read cmd, x= 0 is write cmd.

### External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

### EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001 011X b	16H

### EC SM Bus2 address

Device	Address	HEX
ADI ADM1032 (VGA)	1001 101X b	9AH
(APU)		
RTD2132S (TL)		

### FCH SM Bus 0 address

Device	Address	HEX
DDR DIMM1	1101 000X b	D0
DDR DIMM2	1101 001X b	D2

### FCH SM Bus 1 address

Device	Address	HEX

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

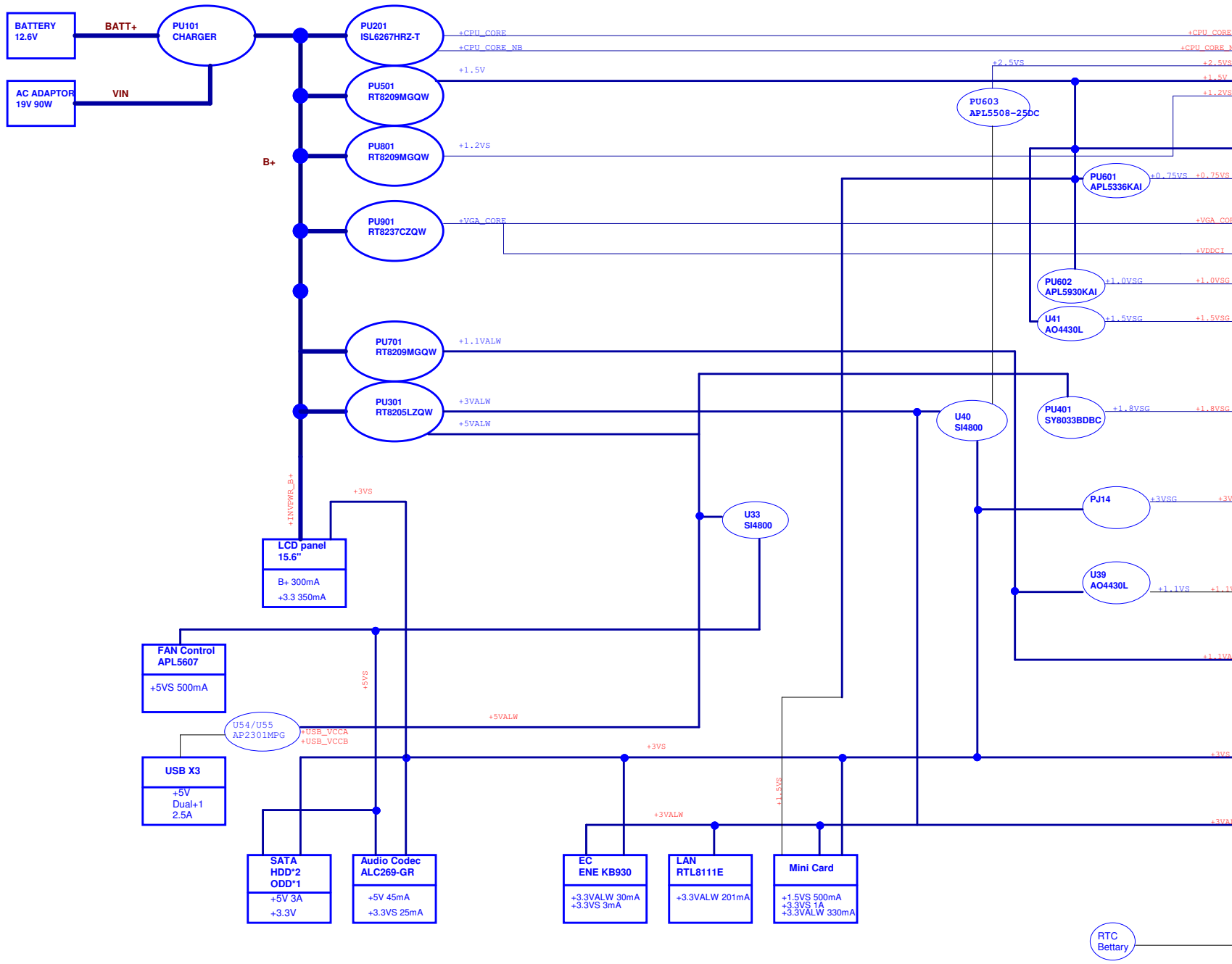
## BTO Option Table

BOM Structure	BTO Item
VGA@	Use VGA (Mux)
X76@	VRAM ID Table
M2@	Use Hudson-M2
M3@	Use Hudson-M3
USB30@	USB30 on M/B
USB20@	USB20 on M/B

M3@ U25  
  
 FCH M3  
 Part Number = SA0000431D0

**BOM Config**

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AMD APU FS1	
0.7~1.475V	VDD CORE 54A
0.7~1.475V	VDDNB 27.5A
+2.5VS	VDDA 500mA
+1.5V	VDDIO 4.6A
+1.2VS	VDDR 6.7A

RAM DDRIII SODIMMx2	
+1.5V	VDD_MEM 4A
+0.75VS	VTT_MEM 0.5A

VGA ATI Whistler/Seymour/Granville	
0.85~1.1V	VDDC 47A
0.9~1.0V	VDDCI 4.6A
+1.0VSG	DPLL_VDDC: 125 mA SPV10: 120 mA PCI_E_VDDC: 2000 mA DPI[A]_VDD10: 680 mA
+1.5VSG	VDDR1: 3400 mA
+1.8VSG	PLL_PVDD: 75 mA TSVDD: 20 mA AVDD: 70 mA VDD1DI: 100 mA VDD2DI: 50 mA AVDDC: 1.5 mA VDD_CT: 110 mA VDDR4: 170 mA PCI_E_PVDD: 40 mA MPV18: 150 mA SPV18: 75 mA PCI_E_VDDR: 400 mA DPI[A]_VDD18: 920 mA DPI[A]_PVDD: 120 mA
+3VSG	A2VDD: 130 mA VDDR3: 60 mA

VRAM 1GB/2GB 64M / 128Mx16 * 4 / 8	
+1.5VSG	2.4 A

FCH AMD Hudson M2/M3	
+1.1VS	VDDPL_11_DAC: 7 mA VDDAN_11_ML: 226 mA VDDCR_11: 1007 mA VDDAN_11_CLK: 340 mA VDDAN_11_PCIE: 1088 mA VDDAN_11_SATA: 1337 mA
+1.1VALW	VDDAN_11_USB_S: 140 mA VDDCR_11_USB_S: 197 mA VDDAN_11_SSUSB_S: 282 mA VDDCR_11_SSUSB_S: 424 mA VDDCR_11_S: 187 mA VDDPL_11_SYS: 70 mA
+3VS	VDDIO_33_PCIE: 131 mA VDDPL_33_SYS: 47 mA VDDPL_33_DAC: 20 mA VDDPL_33_ML: 20 mA VDDAN_33_DAC: 200 mA VDDPL_33_PCIE: 43 mA VDDPL_33_SATA: 93 mA VDDIO_AZ_S: 26 mA
+3VALW	VDDPL_33_SSUSB_S: 20 mA VDDPL_33_USB_S: 17 mA VDDAN_33_USB_S: 658 mA VDDIO_33_S: 59 mA VDDXL_33_S: 5 mA VDDAN_33_HWM_S: 12 mA
GND	VDDIO_33_GBE_S VDDCR_11_GBE_S VDDIO_GBE_S
RTC BAT	VDDBT_RTC_G

18 PCIE\_GTX\_C\_FRX\_P[0..7]

18 PCIE\_GTX\_C\_FRX\_N[0..7]

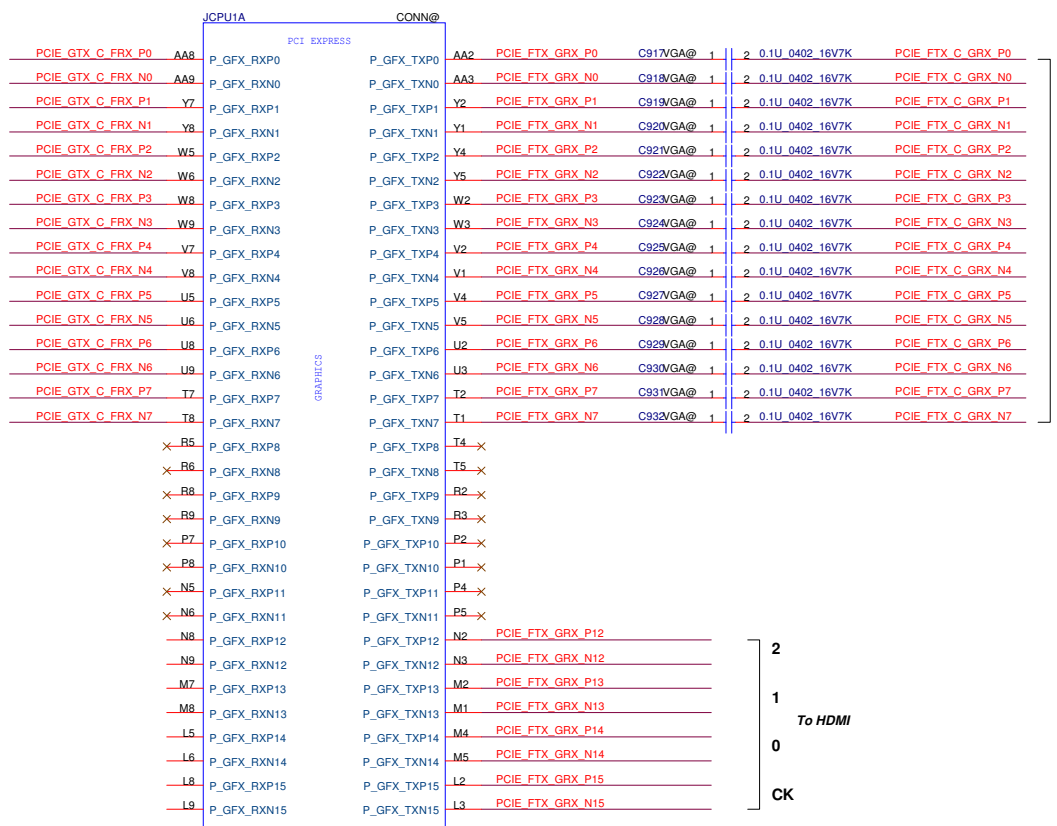
PCIE\_FTX\_C\_GRX\_P[0..7] 18

PCIE\_FTX\_C\_GRX\_N[0..7] 18

**APU To HDMI**

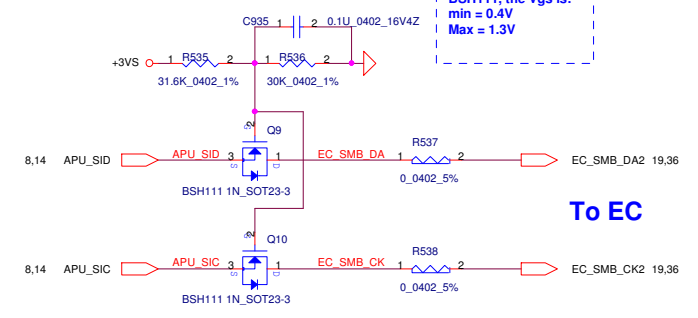
PCIE\_FTX\_GRX\_P[12..15] 28

PCIE\_FTX\_GRX\_N[12..15] 28

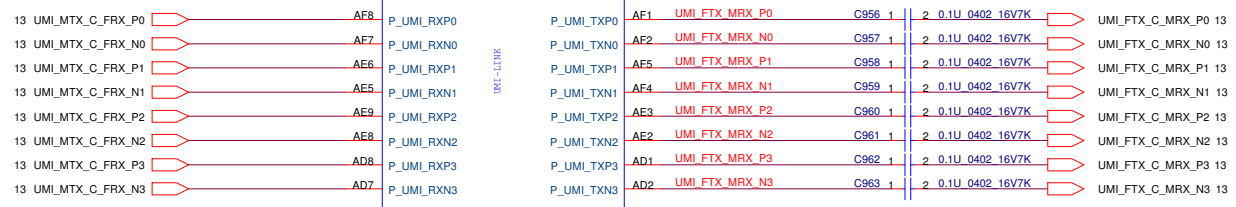
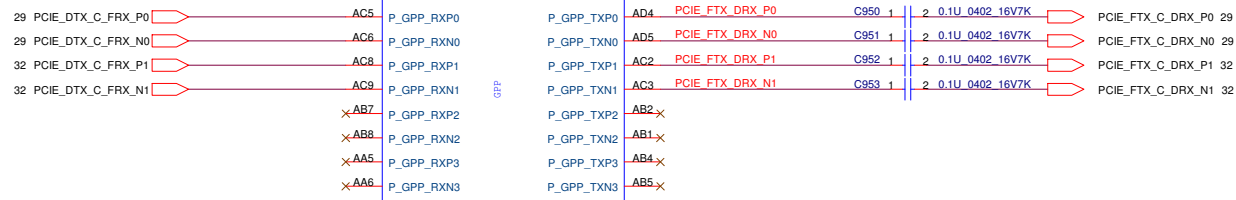


For UMA Mux.

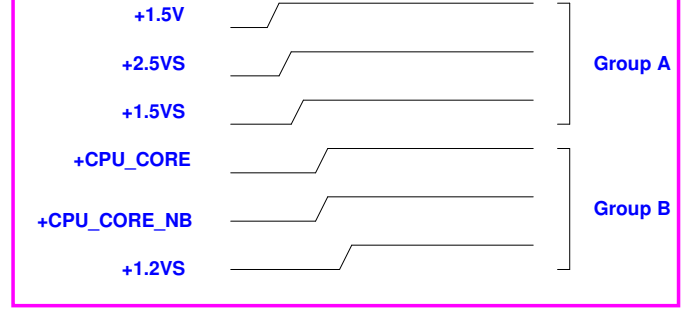
**CPU TSI interface level shift**



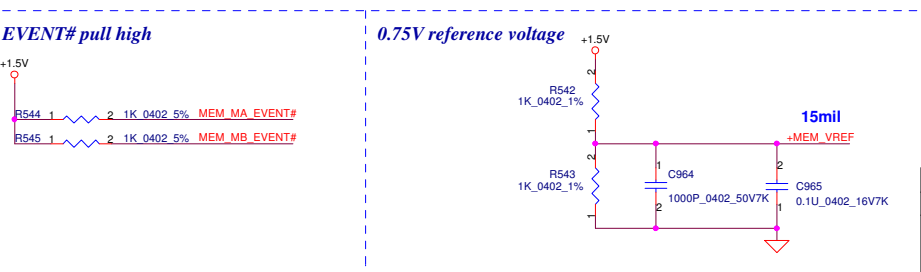
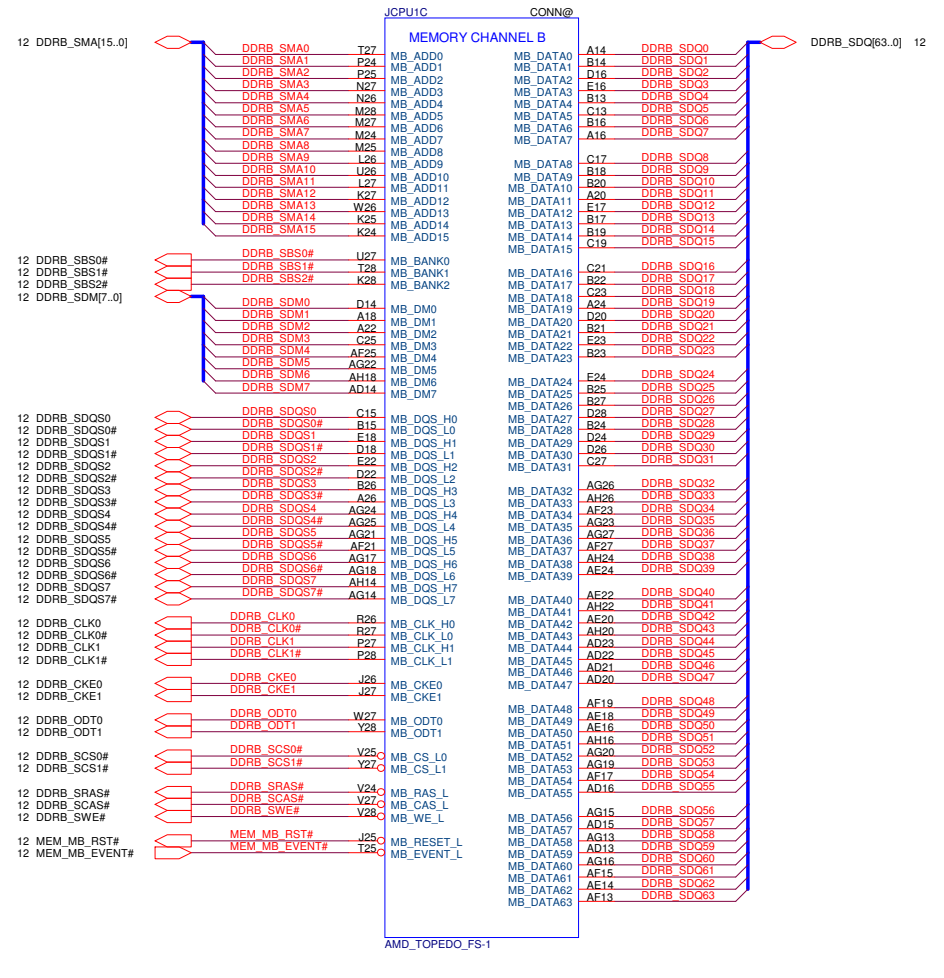
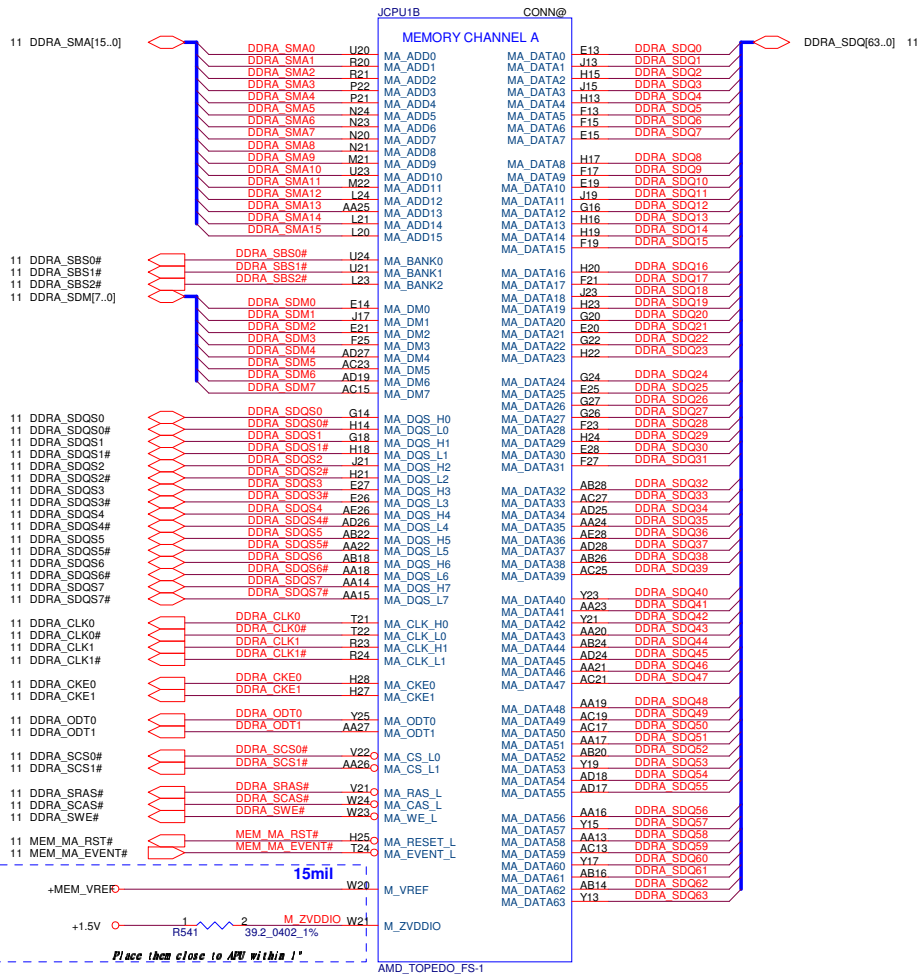
BSH111, the Vgs is:  
min = 0.4V  
Max = 1.3V



**Power Sequence of APU**

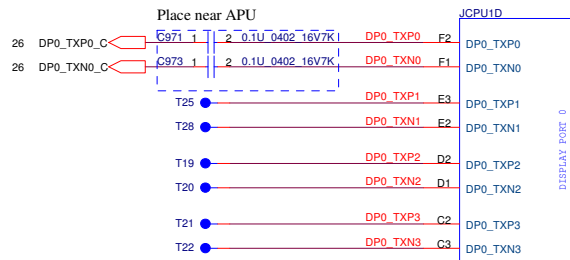


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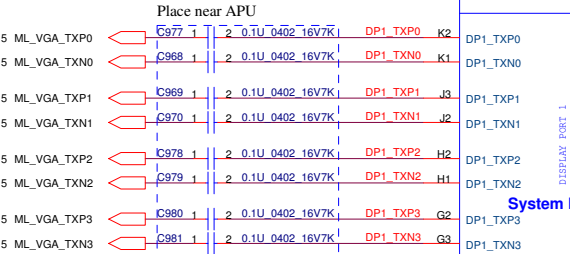


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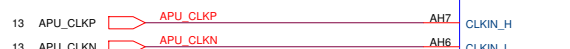
To LVDS Translator



To FCH VGA ML



100MHz



100MHz\_NSS



APU\_SVC



APU\_SID



APU\_RST#



APU\_SIC



APU\_TDI



APU\_TCK



APU\_TRST#



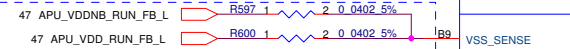
APU\_DBREQ#



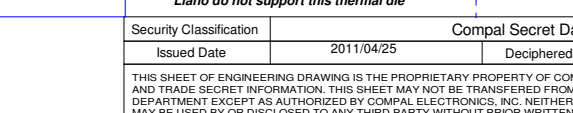
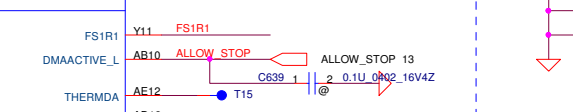
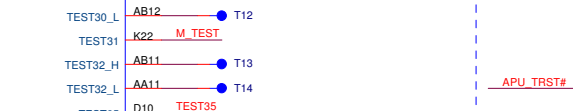
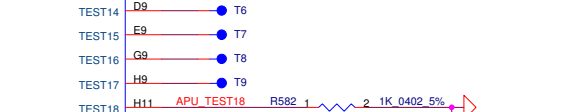
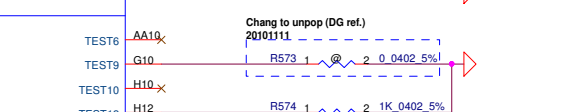
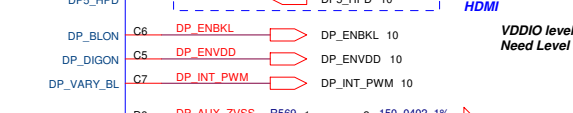
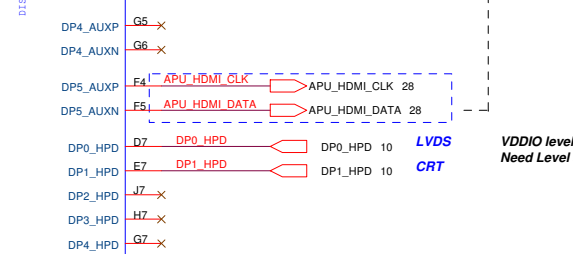
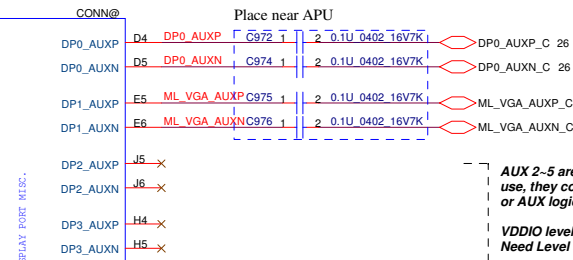
APU\_VDDNB\_RUN\_FB\_L



APU\_VDD\_RUN\_FB\_L



APU\_VDD\_SEN



To LVDS Translator

To FCH

AUX 2-5 are for GFX interface use, they could be selected to I2C or AUX logic

VDDIO level Need Level shift

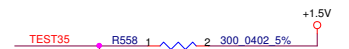
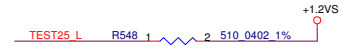
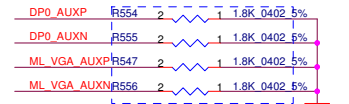
VDDIO level Need Level shift

HDMI

VDDIO level Need Level shift

If not used, pins are left unconnected (DG ref.)

20101111

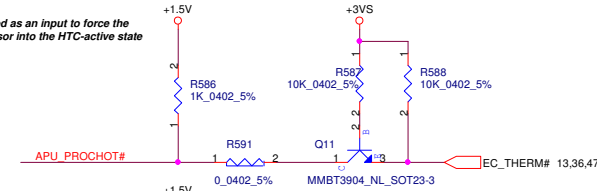


FS1R1 : Control S5 Dual PWR plane in laptop, seems no use



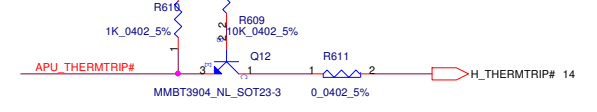
MISC

Asserted as an input to force the processor into the HTC-active state

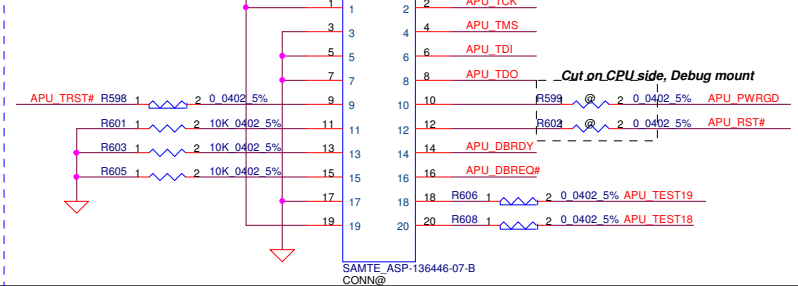


THERMTRIP shutdown temperature: 125 degree

Indicates to the FCH that a thermal trip has occurred. Its assertion will cause the FCH to transition the system to S5 immediately



HDT Debug conn



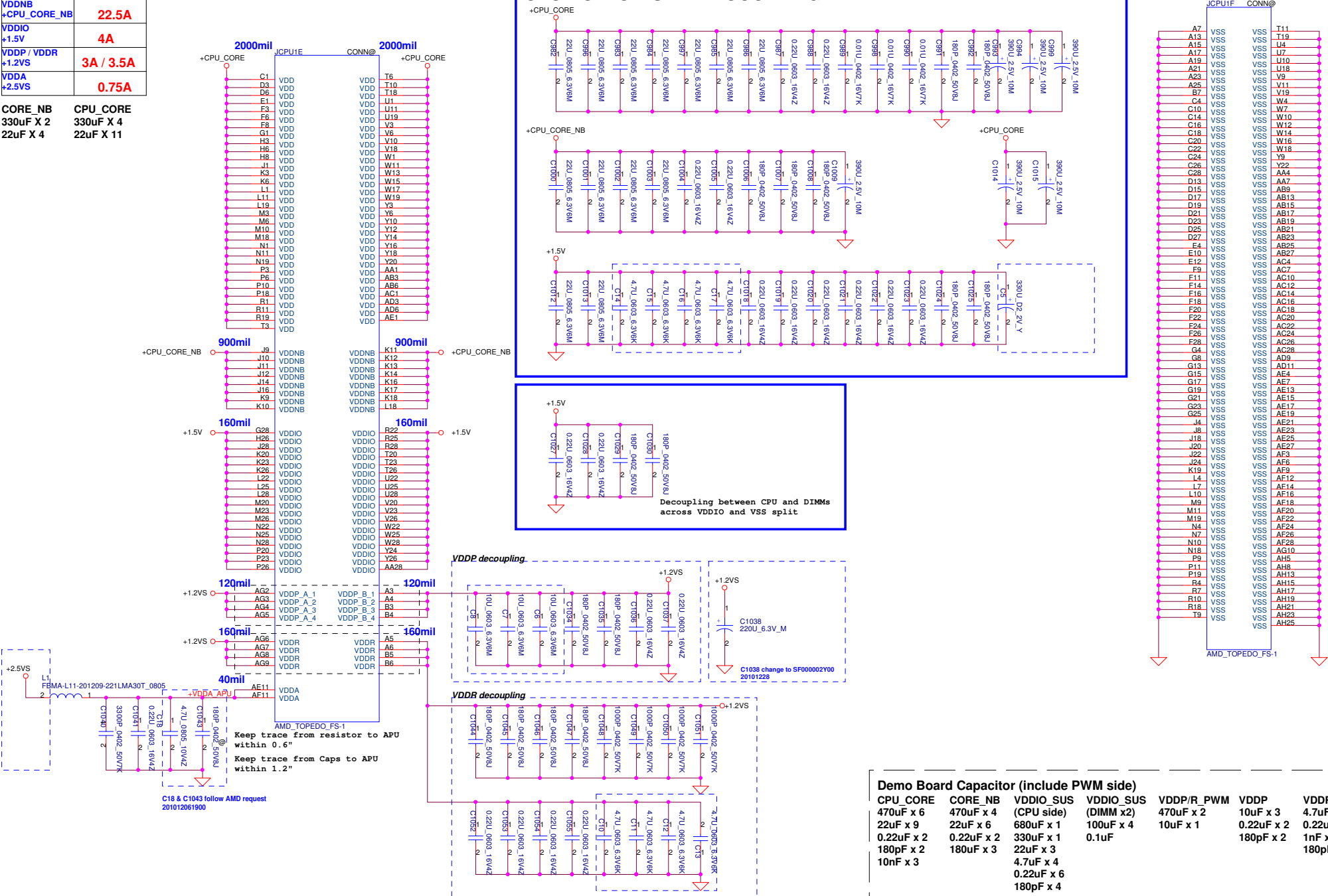
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Power Name	Consumption
VDD	
+CPU_CORE	<b>50A</b>
VDDNB	
+CPU_CORE_NB	<b>22.5A</b>
VDDIO	
+1.5V	<b>4A</b>
VDDP / VDDR	
+1.2VS	<b>3A / 3.5A</b>
VDDA	
+2.5VS	<b>0.75A</b>

CORE_NB	CPU_CORE
330uF X 2	330uF X 4
22uF X 4	22uF X 11

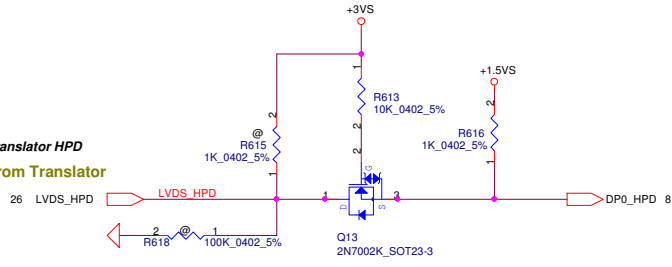
### CPU BOTTOM SIDE DECOUPLING



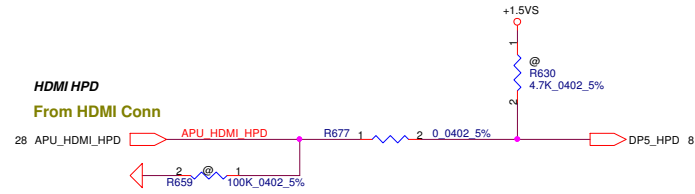
JCPU1F	CONN@
A7	T11
A13	T19
A15	T14
A17	U7
A19	U10
A21	U18
A23	V9
A25	V11
B7	V19
C4	W4
C10	W7
C14	W10
C16	W12
C18	W14
C20	W16
C22	W18
C24	Y9
C26	Y22
C28	AA4
D13	AA7
D15	AB9
D17	AB13
D19	AB15
D21	AB17
D23	AB19
D25	AB21
D27	AB23
E4	AB25
E10	AB27
E12	AC4
F3	AC7
F11	AC10
F14	AC12
F16	AC14
F18	AC16
F20	AC18
F22	AC20
F24	AC22
F26	AC24
F28	AC26
G4	AC28
G8	AD9
G12	AD11
G15	AE4
G17	AE7
G19	AE13
G21	AE15
G23	AE17
G25	AE19
J4	AE21
J8	AE23
J12	AE25
J20	AE27
J22	AF3
J24	AF6
K18	AF9
L4	AF12
L7	AF14
L10	AF16
M9	AF18
M11	AF20
M19	AF22
N4	AF24
N7	AF26
N10	AF28
N18	AG10
P9	AH5
P11	AH8
P19	AH13
R4	AH15
R7	AH17
R10	AH19
R18	AH21
T9	AH23
	AH25

# HPD

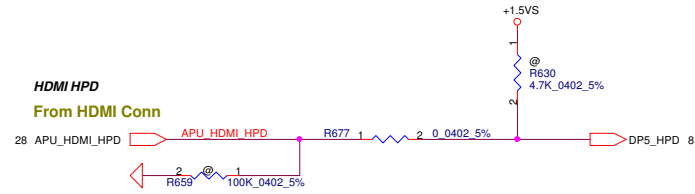
## Translator HPD From Translator



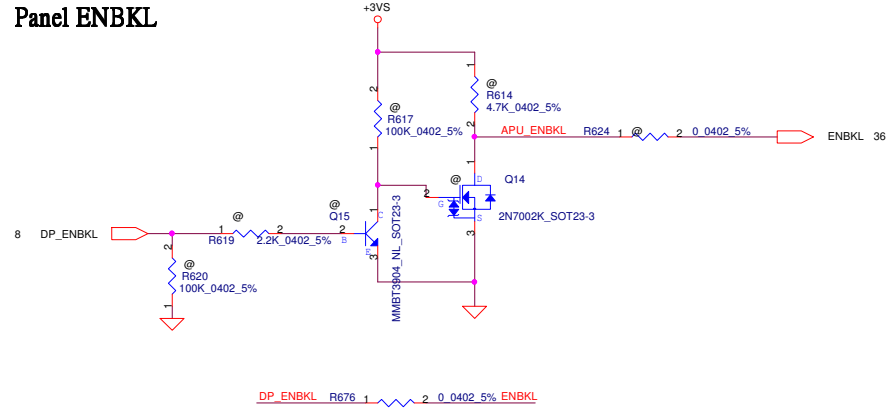
## CRT HPD From FCH



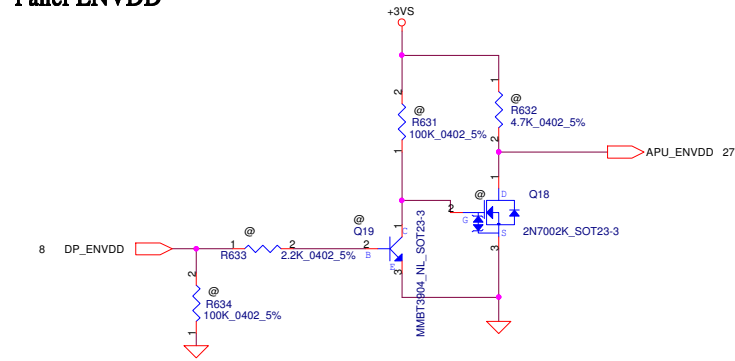
## HDMI HPD From HDMI Conn



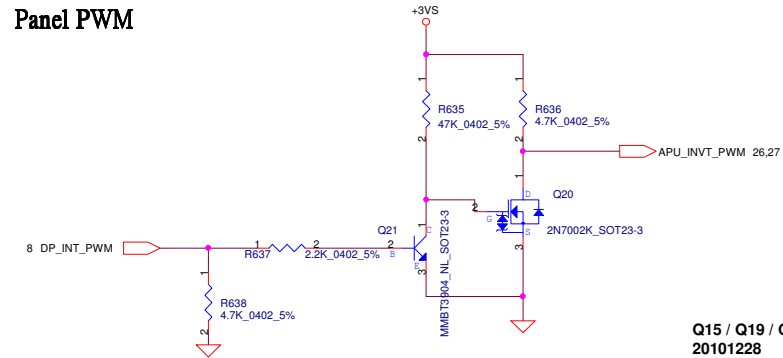
# Panel ENBKL



# Panel ENVDD

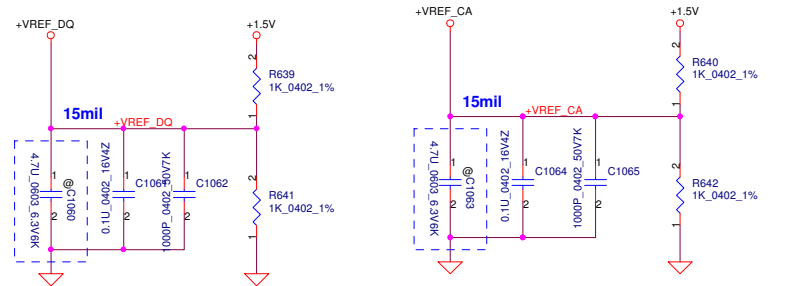
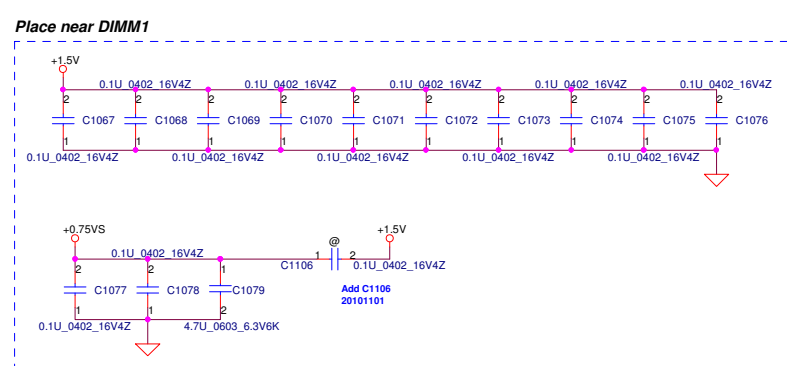
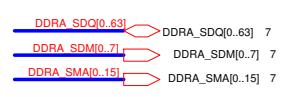
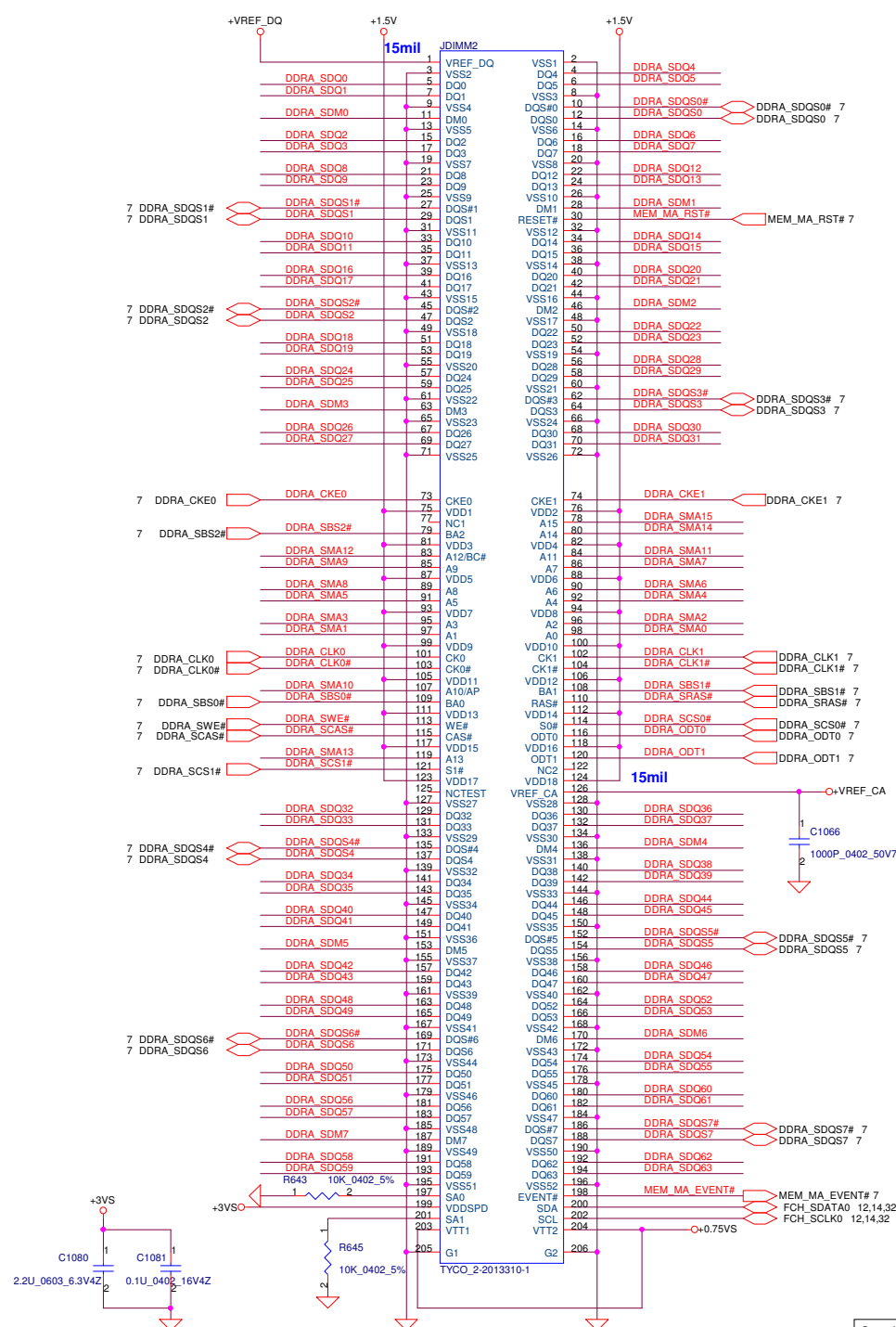


# Panel PWM



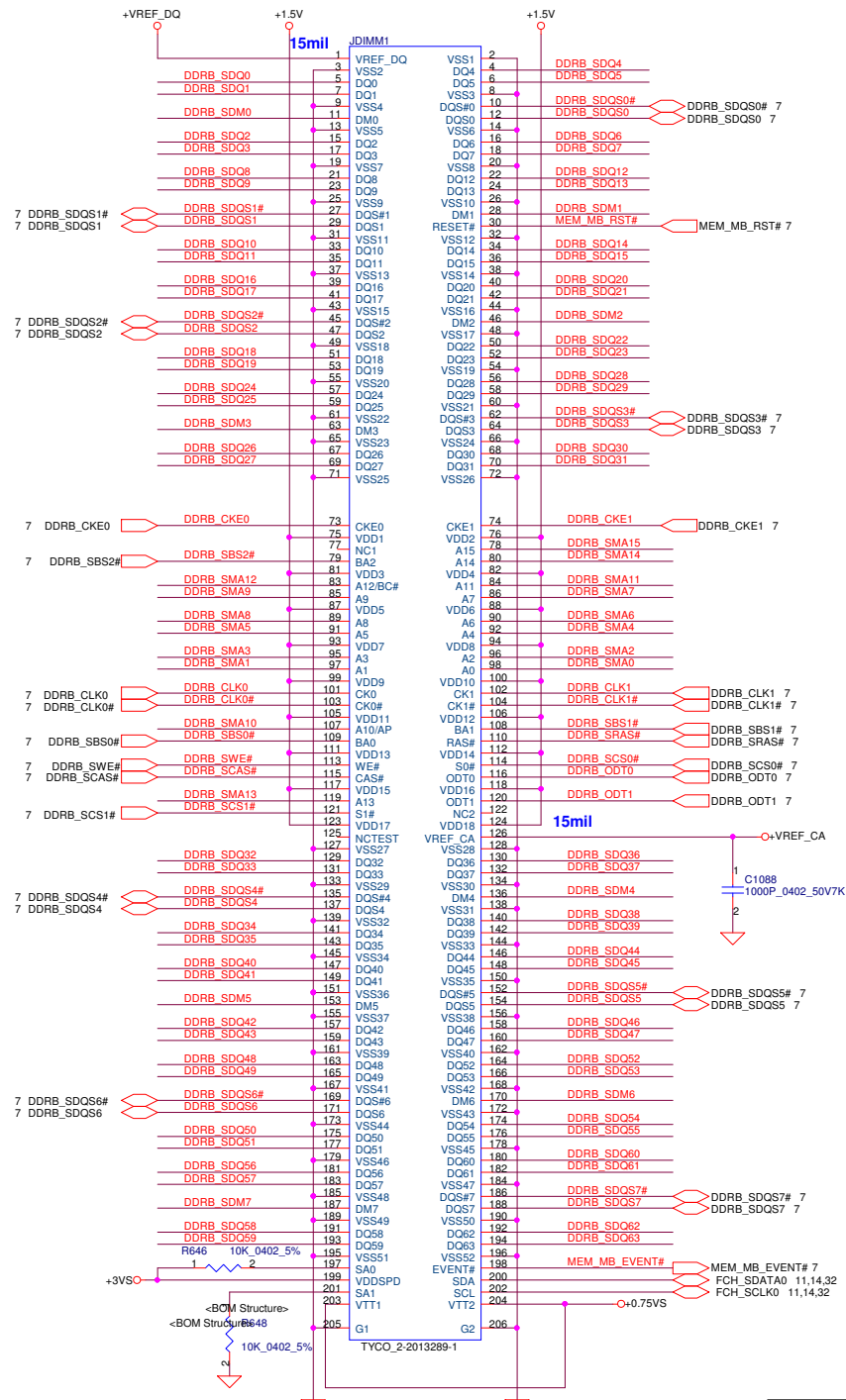
Q15 / Q19 / Q21 change to SB000006A00  
20101228

Security Classification	Compal Secret Data			Title	AMD FS1 Singal Level Shifter
Issued Date	2011/04/25	Deciphered Date	2012/04/25	Document Number	QBL60 LA-7552P
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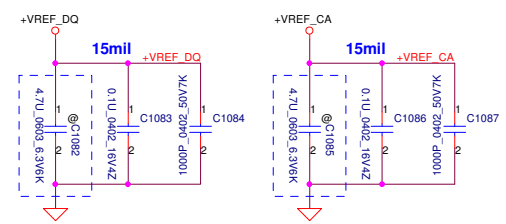
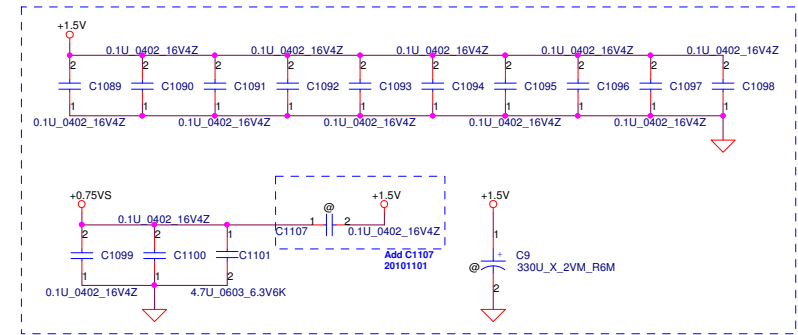
**DIMM\_A STD H:9.2mm**  
 <Address: 00>

Security Classification		Compal Secret Data		Cmpal Electronics, Inc.	
Issued Date	2011/04/25	Deciphered Date	2012/04/25	Title	
				DDRIII SO-DIMM 1	
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- DDRB\_SDO[0..63] — DDRB\_SDOQ[0..63] 7
- DDRB\_SDM[0..7] — DDRB\_SDMQ[0..7] 7
- DDRB\_SMA[0..15] — DDRB\_SMAQ[0..15] 7

Place near DIMM2

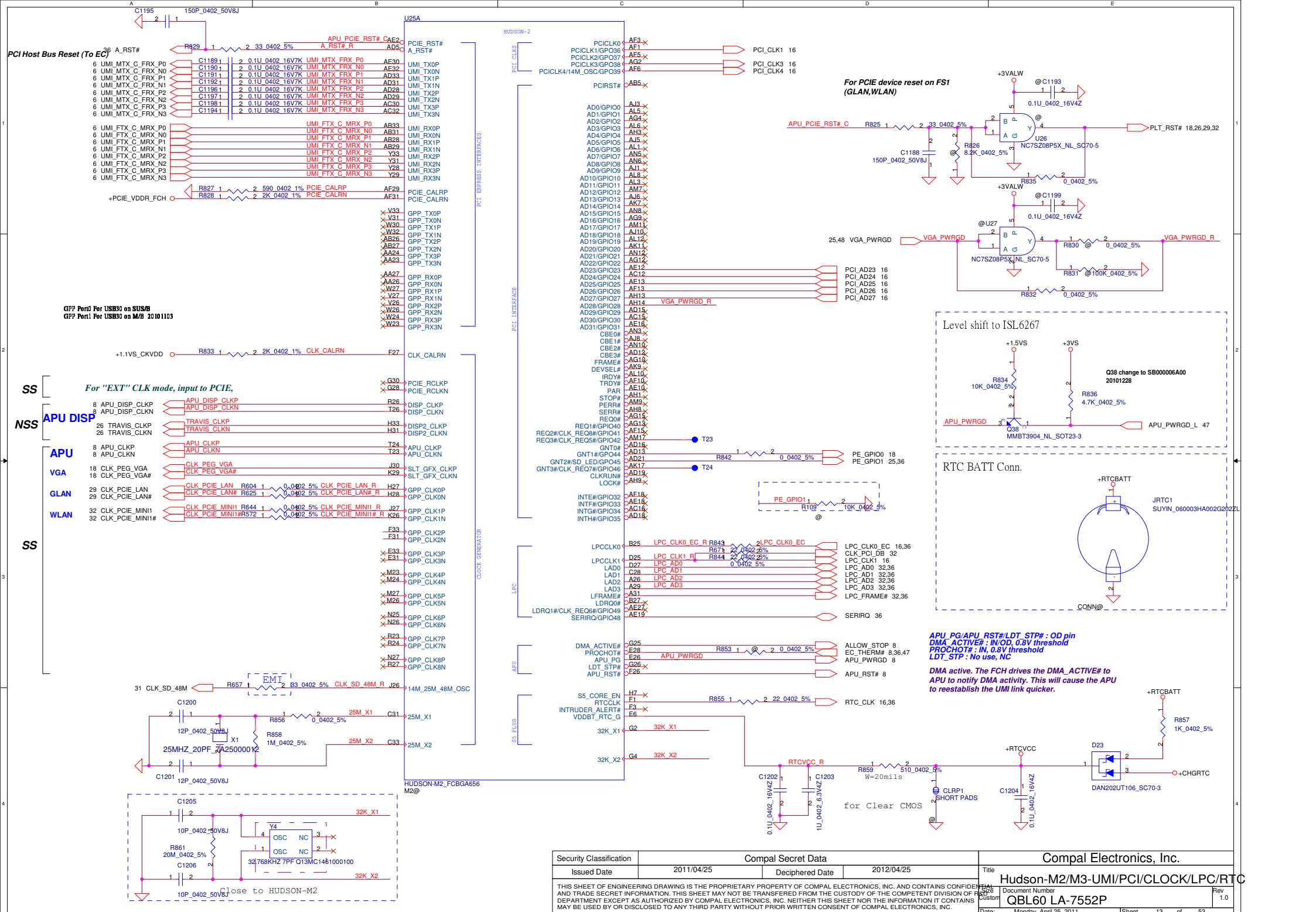


**DIMM\_B STD H:5.2mm**  
 <Address: 01>

Security Classification	Compal Secret Data	
Issued Date	2011/04/25	Deciphered Date
		2012/04/25

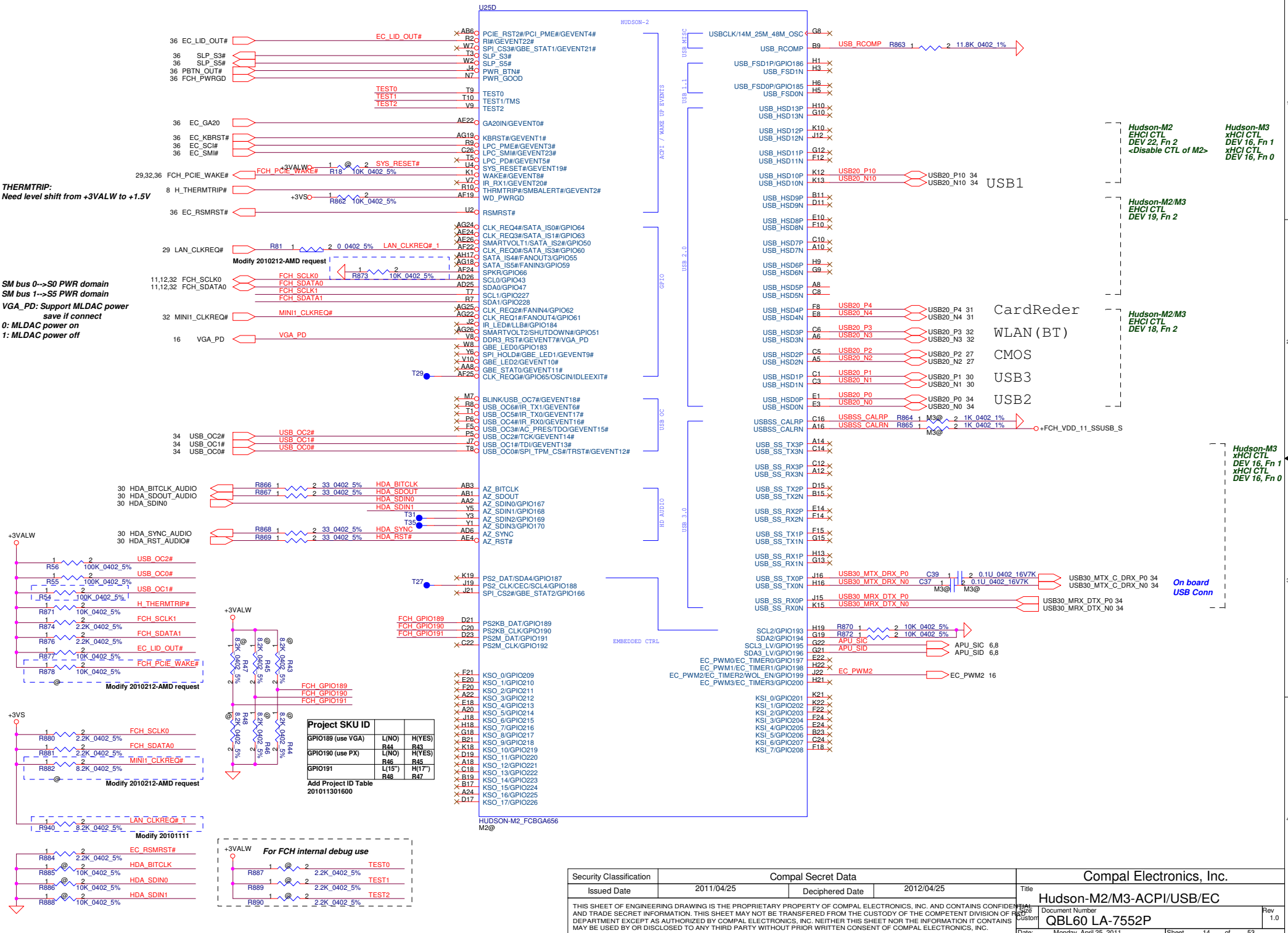
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Compal Electronics, Inc.		
DDRIII SO-DIMM 2		
File No	Document Number	Rev
Custom	<b>QBL60 LA-7552P</b>	1.0
Date	Monday, April 25, 2011	Sheet 12 of 53

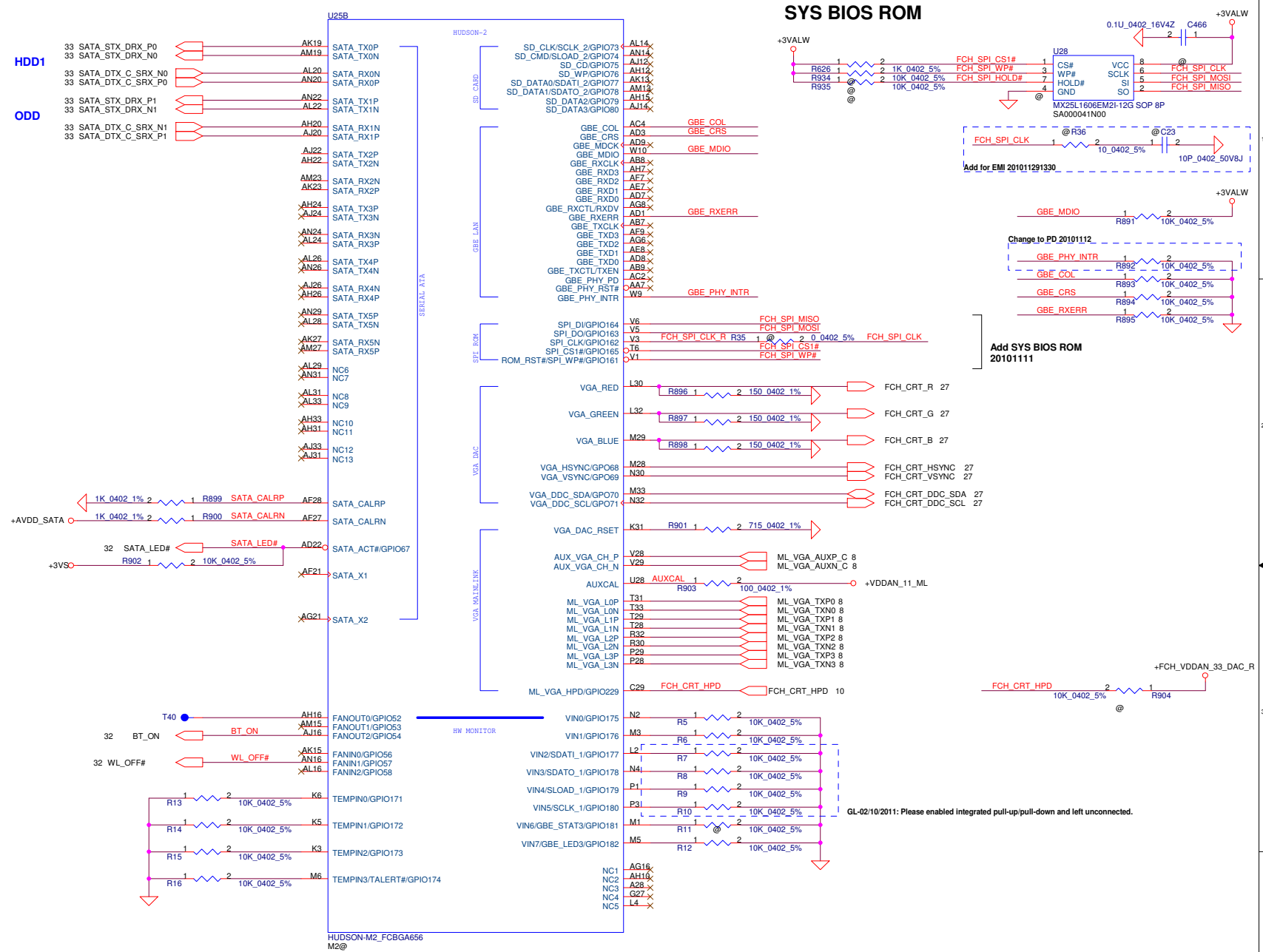


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/04/25	Deciphered Date	2012/04/25	Title	Hudson-M2/M3-UMI/PCI/CLOCK/LPC/RTC
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				Customer	QBL60 LA-7552P
Date:	Monday, April 25, 2011	Sheet	13 of 53	Rev	1.0

PCIE\_RST2 : Reset PCIE device on Hudson2



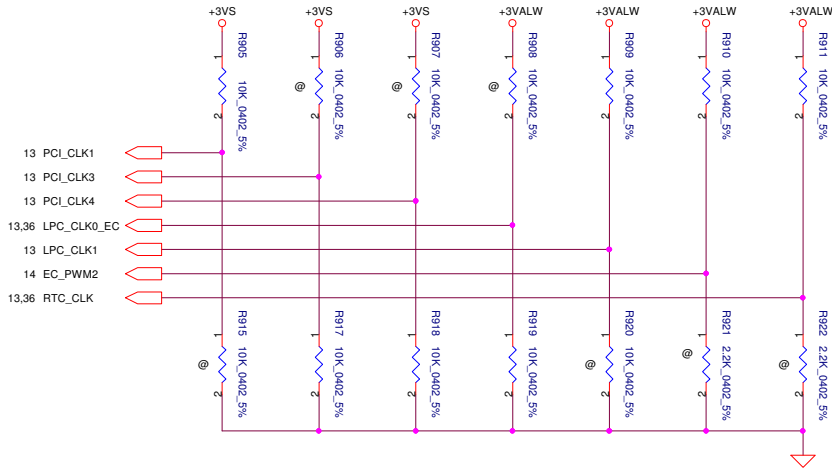
Security Classification	Compal Secret Data		Title	
Issued Date	2011/04/25	Deciphered Date	2012/04/25	Hudson-M2/M3-ACPI/USB/EC
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Security Classification	Compal Secret Data		Title	
Issued Date	2011/04/25	Deciphered Date	2012/04/25	Hudson-M2/M3-SATA/GBE/HWM
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				Rev 1.0 Sheet 15 of 53

# STRAP PINS

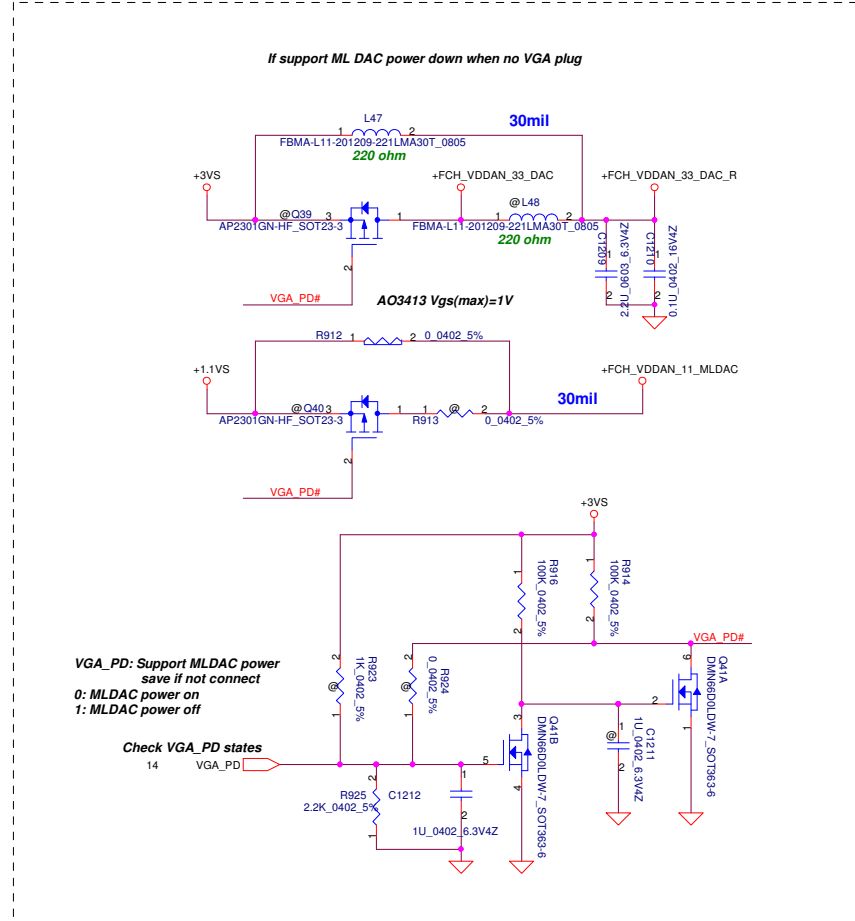
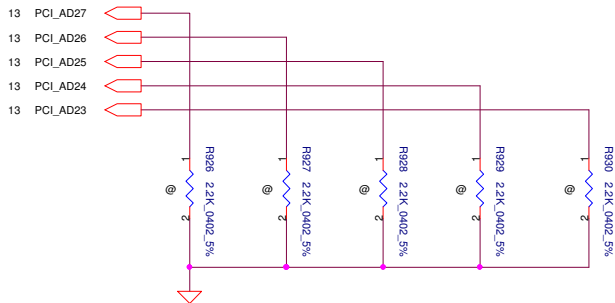
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
<b>PULL HIGH</b>	ALLOW PCIE GEN2 <b>DEFAULT</b>	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED <b>DEFAULT</b>	LPC ROM <b>DEFAULT</b>	S5 PLUS MODE DISABLED <b>DEFAULT</b>
<b>PULL LOW</b>	FORCE PCIE GEN1	IGNORE DEBUG STRAP <b>DEFAULT</b>	FUSION CLOCK MODE <b>DEFAULT</b>	EC DISABLED	CLKGEN DISABLE	SPI ROM	S5 PLUS MODE ENABLED



# DEBUG STRAPS

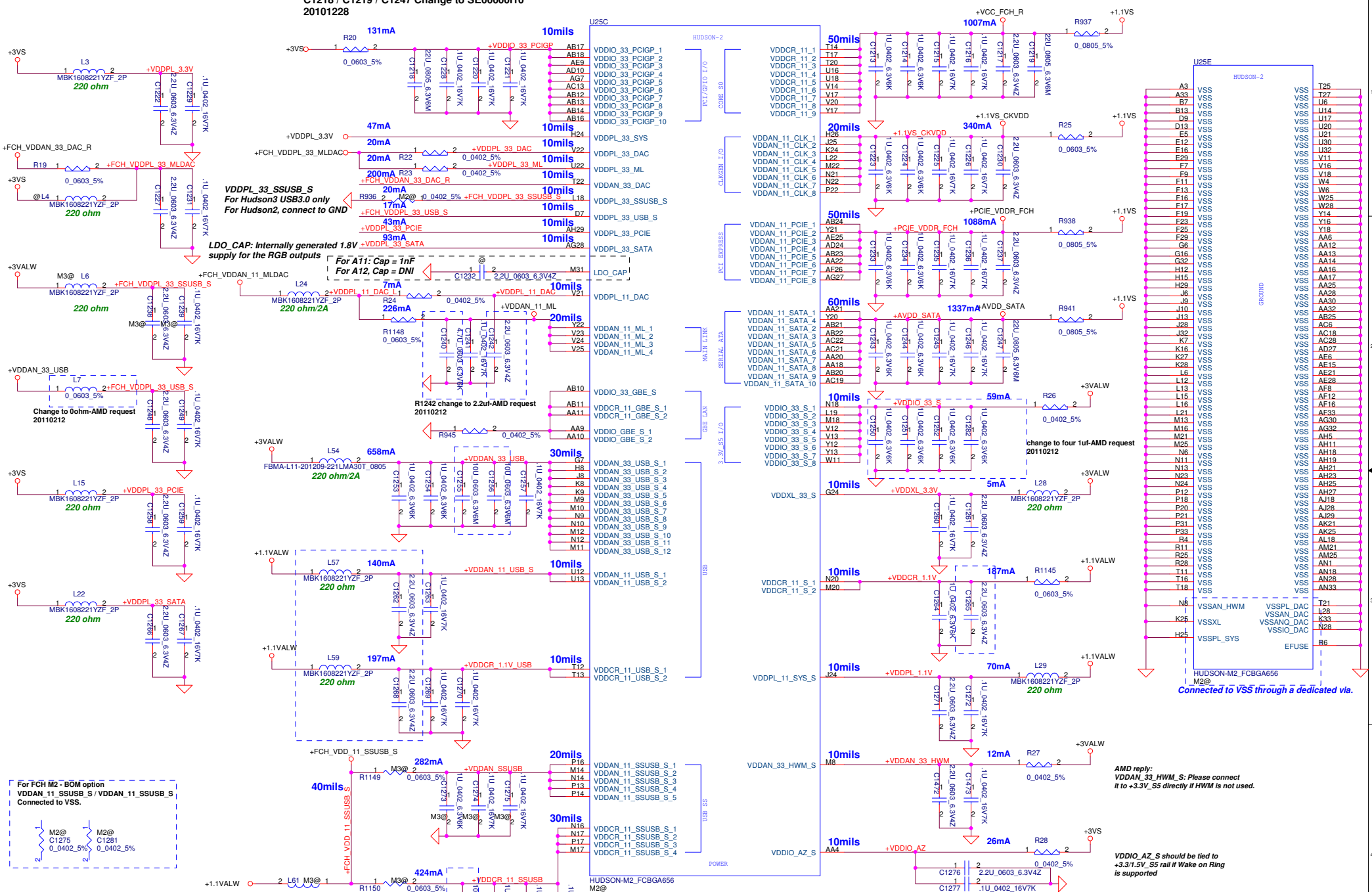
FCH HAS 15K INTERNAL PU FOR PCI\_AD[27:23]

PCI_AD26	PCI_AD27	PCI_AD25	PCI_AD24	PCI_AD23	
<b>PULL HIGH</b>	USE PCI PLL <b>DEFAULT</b>	DISABLE ILA AUTORUN <b>DEFAULT</b>	USE FC PLL <b>DEFAULT</b>	USE DEFAULT PCIE STRAPS <b>DEFAULT</b>	DISABLE PCI MEM BOOT <b>DEFAULT</b>
<b>PULL LOW</b>	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCI STRAPS	ENABLE PCI MEM BOOT





**C1218 / C1219 / C1247 Change to SE00000110  
20101228**



For FCH M2 - BOM option  
VDDAN\_11\_SSUSB\_S / VDDAN\_11\_SSUSB\_S  
Connected to VSS.

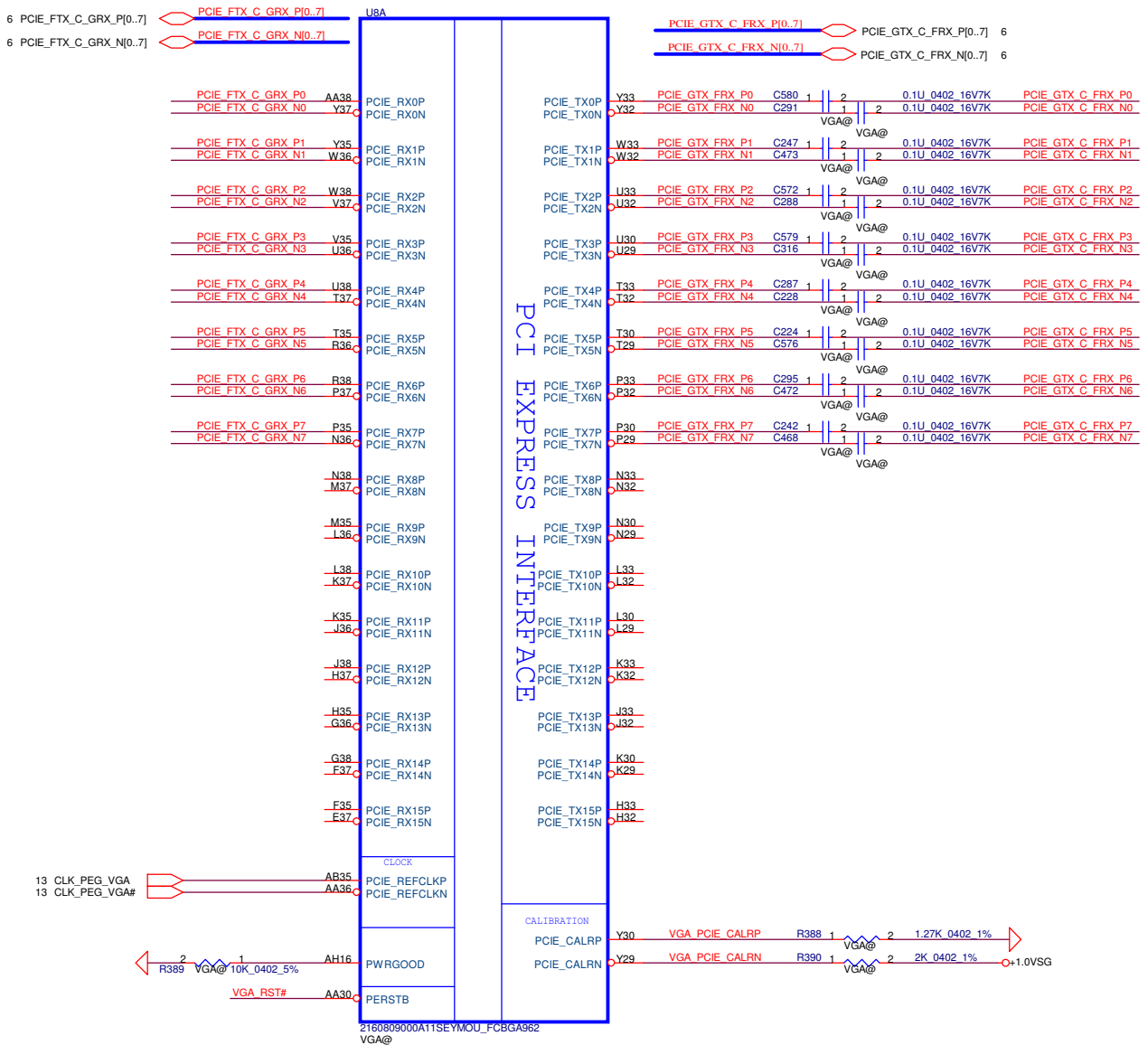
AMD reply:  
VDDAN\_33\_HWM\_S: Please connect  
it to +3.3V\_S5 directly if HWM is not used.

VDDIO\_AZ\_S should be tied to  
+3.3/1.5V\_S5 rail if Wake on Ring  
is supported

Connected to VSS through a dedicated via.

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Document Number	QBL60 LA-7552P			Rev 1.0
Date	Monday, April 25, 2011	Sheet	17	of 53

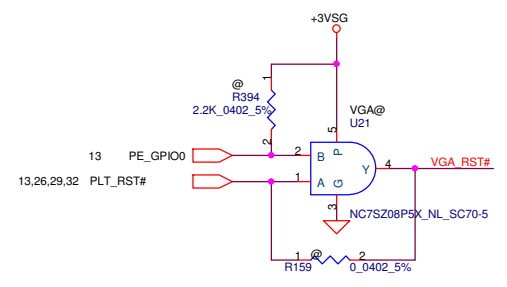
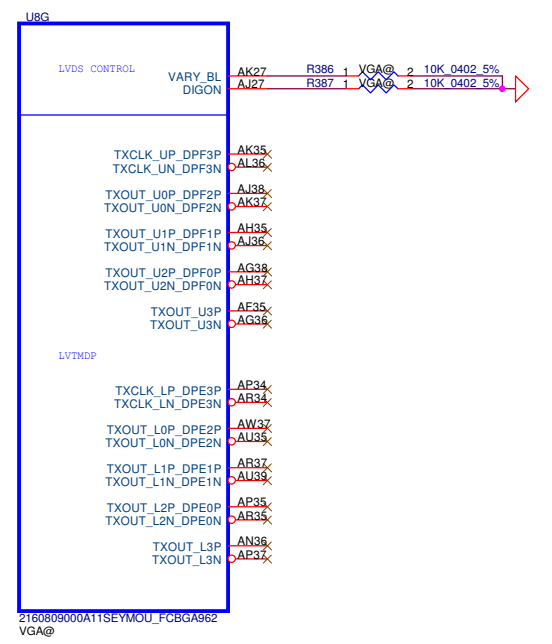
# GFX PCIE LANE REVERSAL



For UMA Mux.

**<DIGON>**  
Controls panel digital power on/off.  
Active High ,external PD need

**<VARY\_BL>**  
LCD PWM (pulse width modulated)  
output to adjust LCD brightness  
Active High ,external PD need



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Issued Date	2011/04/25	Deciphered Date	2012/04/25	Title	Vancouver_PCIE / LVDS
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				Date	Monday, April 25, 2011
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				Part Number	QB160 LA-7552P

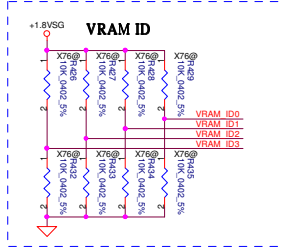
Strap Name	Pin Straps description <all Internal PD>	Setting
VIP_DEVICE_EN (GENLK_VSYNC)	VIP Device Strap Enable indicates to the software driver (Internal PD) 0: Driver would ignore the value sampled on VHAD_0 during reset 1: VHAD_0 to determine whether or not a VIP slave device	0
VGA_DIS	VGA Disable determines (Internal PD) 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENB	Transmitter Power Saving Enable (Internal PD) 0: 50% Tx output swing 1: Full Tx output swing	1
TX_DEEMPH_EN	PCI Express Transmitter De-emphasis Enable (Internal PD) 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	1
CONFIG[2]	GPIO13,12,11 (config 2,1,0) : (Internal PD) memory apertures a) If BIOS_ROM_EN = 1, then Config[2:0] defines CONFIG[3:0] 128 MB 000 the ROM type b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. 64 MB 010	001
CONFIG[1]		
CONFIG[0]		
BIOS_ROM_EN	GPIO22 Enable external BIOS ROM device (Internal PD) 0: Disable, 1: Enable	0
AUD[1]	HSYNC 00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	00
AUD[0]	VSYNC	
BIF_GEN2_EN	GPIO2 0: Advertises the PCIe device as 5.0 GT/s capable at power-on 1= Advertises the PCIe device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	1
RESERVED	H2SYNC GENLK_CLK GPIO8 GPIO21 Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	DNI

Don't have this strap on Whistler and Seymour

NC on Park, Robson and Seymour  
NC on Park, Robson

NC on Park, Robson and Seymour

Global Swap Lock on Multiple GPUs



GPIO5 fast-power reduction: HW control will cause display disturb should use SW method control  
GPIO6 voltage control signal, No use can NC!

Move to DDCCCLK\_AUX3P,DDCDATA\_AUX3N

GPIO7 Controls backlight on/off. Active High, need external PD  
If GPIO22 High, GPIO 11-13--CFG[0:2] Config ROM type, GPU has internal PD

GPIO6,15,16,20  
Voltage control signal  
GPIO6,15 no use can NC  
Thermal monitor interrupt  
Critical temperature fault

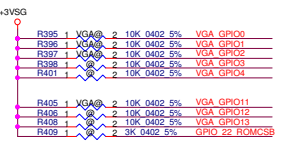
Reserved

External BIOS device  
DN(1)/OFF(0) Inter PD

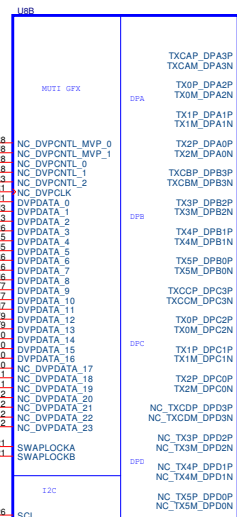
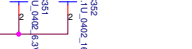
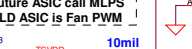
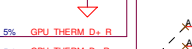
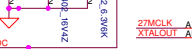
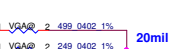
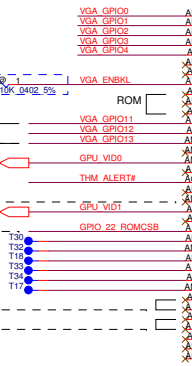
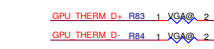
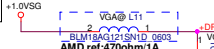
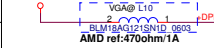
Internal Debug  
no use can floating  
ON(1)/OFF(0)

Stereo Sync  
no use can NC

For ATI Cross fire  
no use can NC



VRAM	Location	VRAM_ID3	VRAM_ID2	VRAM_ID1	VRAM_ID0
Samsung	BA10004530 64M16x8 K4W1G1646G-BC11	0	0	0	0
Samsung	BA0000470A0 128M16x8 K4W2G1646G-BC11	0	0	0	1
Hynix	BA000041S60 64M16x8 H5TQ16630PFR-11C	0	1	0	0
Hynix	BA00003Y030 128M16x8 H5TQ26638PFR-11C	0	1	0	1



NC on Park, Robson and Seymour

Not share via for other GND

70mA  
100mA

10mil

AMD ref:120ohm/0.3A

SM010030010  
200ma 120ohm@100mhz DCR 0.2

Back compatibility (Manhattan)

100mA  
100mA  
2mA

10mil

125mA

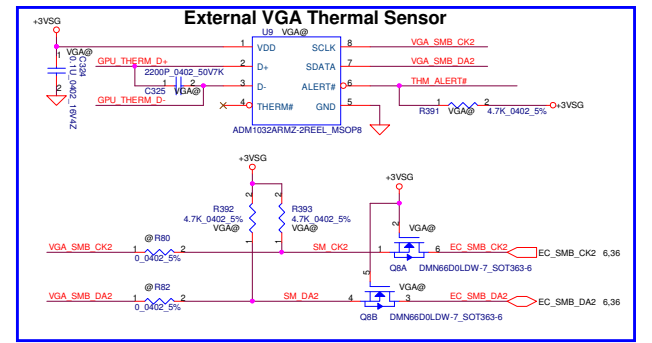
NC on Park, Robson and Seymour

NC on Park, Robson and Seymour

20mA

10mil

120ohm/0.3A



VGA SMB CK2 @ R80 1 VGA@ 2 0.0402 5% VGA GPIO4

VGA SMB DA2 @ R82 1 VGA@ 2 0.0402 5% VGA GPIO3

SM CK2 @ R78 1 VGA@ 2 0.0402 5% VGA GPIO4

SM DA2 @ R79 1 VGA@ 2 0.0402 5% VGA GPIO3

HSYNC:VSYNC  
11: Audio for both DisplayPort and HDMI

AUD Strap  
VSYNC  
HSYNC

NC on Whistler and Seymour

Whistler and Seymour  
Except A2VSSQ change to TSVSSQ,  
others are NC

10mil

100mA

10mil

10mil

10mil

10mil

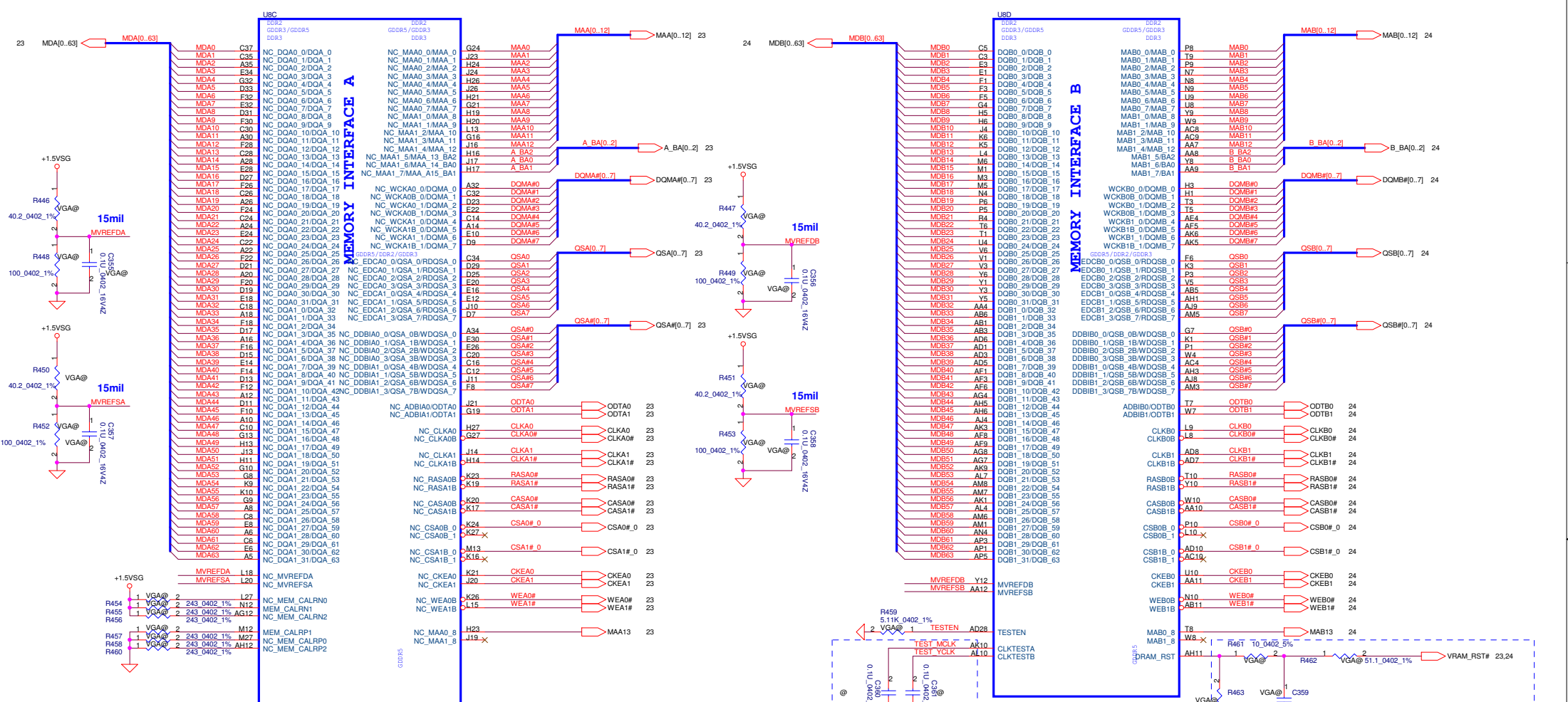
10mil

10mil

10mil

10mil

10mil



2160809000A11SEYMOU\_FCBGA962  
VGA@

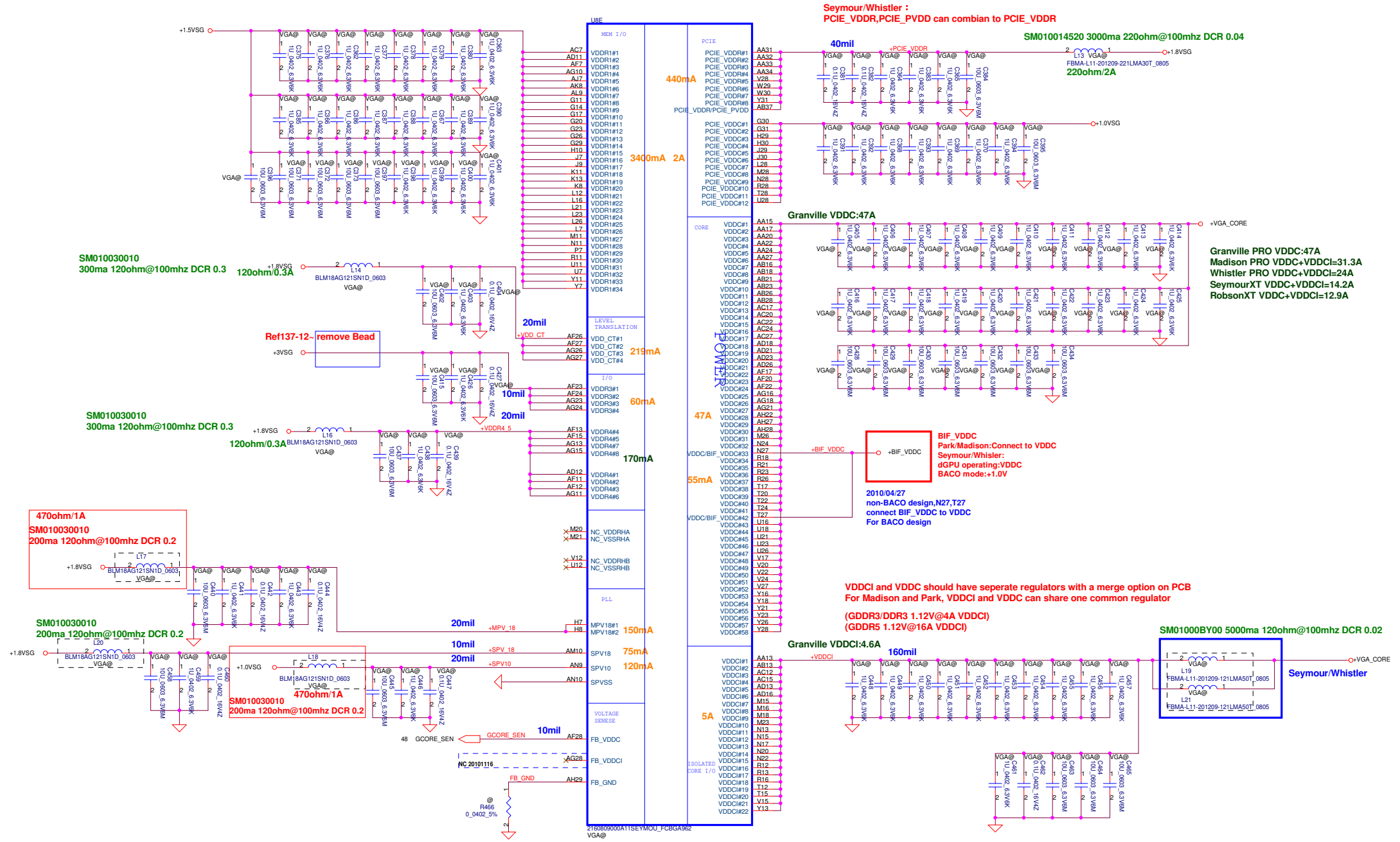
2160809000A11SEYMOU\_FCBGA962  
VGA@

Place all these components very close to GPU (Within 25mm) and keep all component close to each other (within 5mm) except Rser2

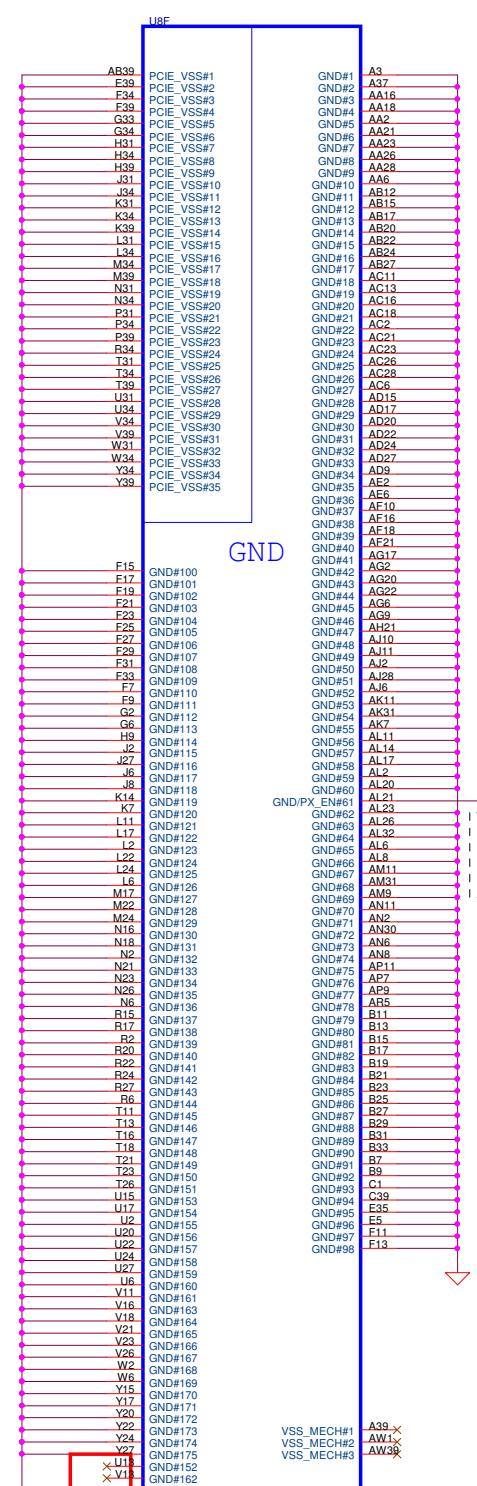
Note:  
route 50ohms single-ended  
and 100ohms diff  
and keep short  
REF137-03 suggest

**Park&Seymour is single channel for memory (channel B only)**

Security Classification	Compal Secret Data		Title	
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Part Number				Rev
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Security Classification	Compal Secret Data		Title	
Issued Date	2011/04/25	Deciphered Date	2012/04/25	Vancouver Power/GND
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Size	Document Number	Rev		
Custom	QBL60 LA-7552P	1.0		
Date:	Monday, April 25, 2011	Sheet	21	of 53

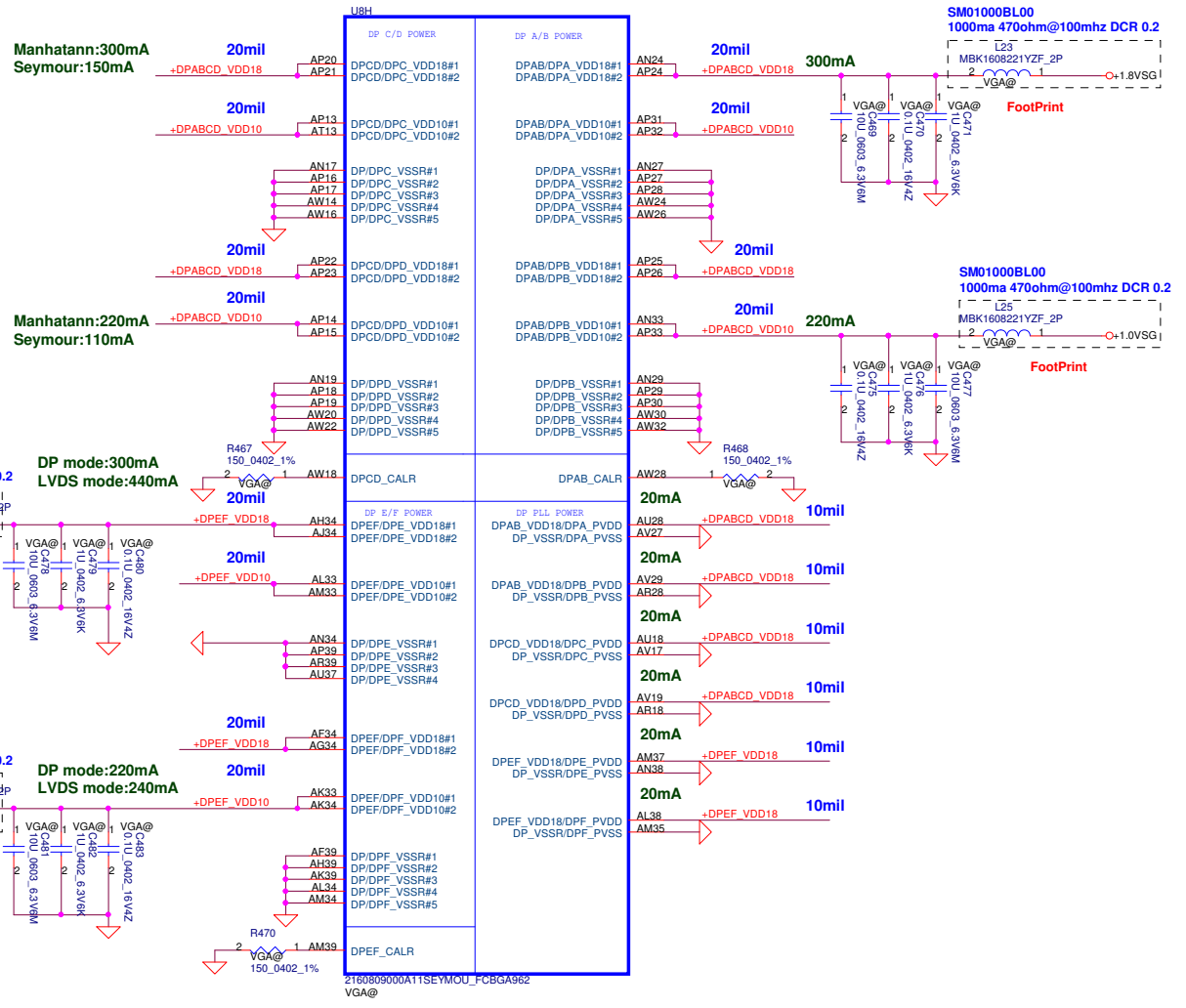


DPA\_VDD18,DPA\_PVDD,DPB\_VDD18,DPB\_PVDD can combian to DPAB\_VDD18  
 DPC\_VDD18,DPC\_PVDD,DPD\_VDD18,DPD\_PVDD can combian to DPCD\_VDD18  
 (DPD\_VDD18,DPD\_PVDD not applicable on Robson/Park)  
 DPE\_VDD18,DPE\_PVDD,DPF\_VDD18,DPF\_PVDD can combian to DPEF\_VDD18

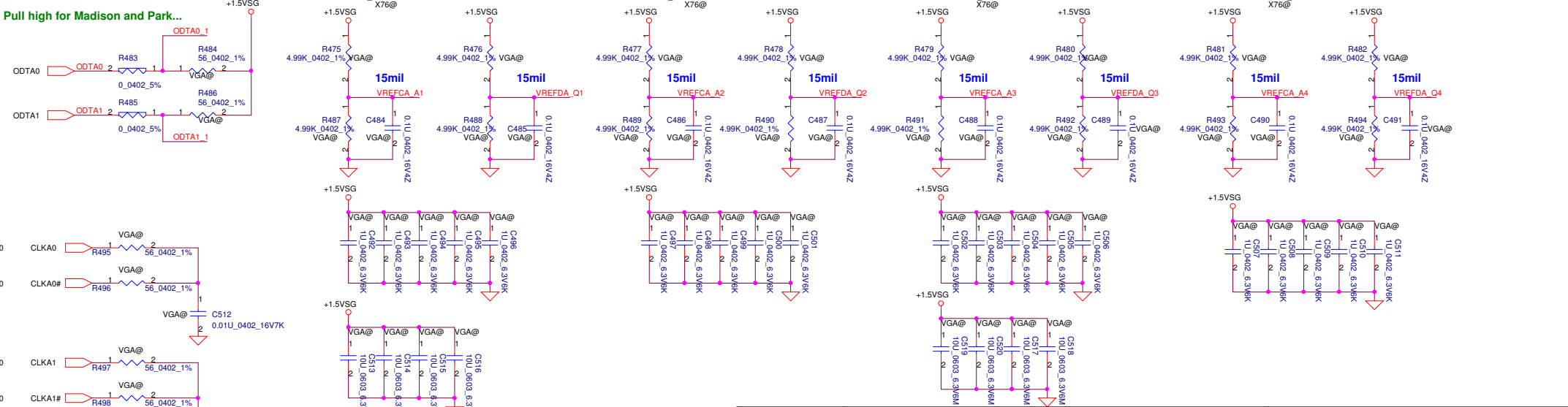
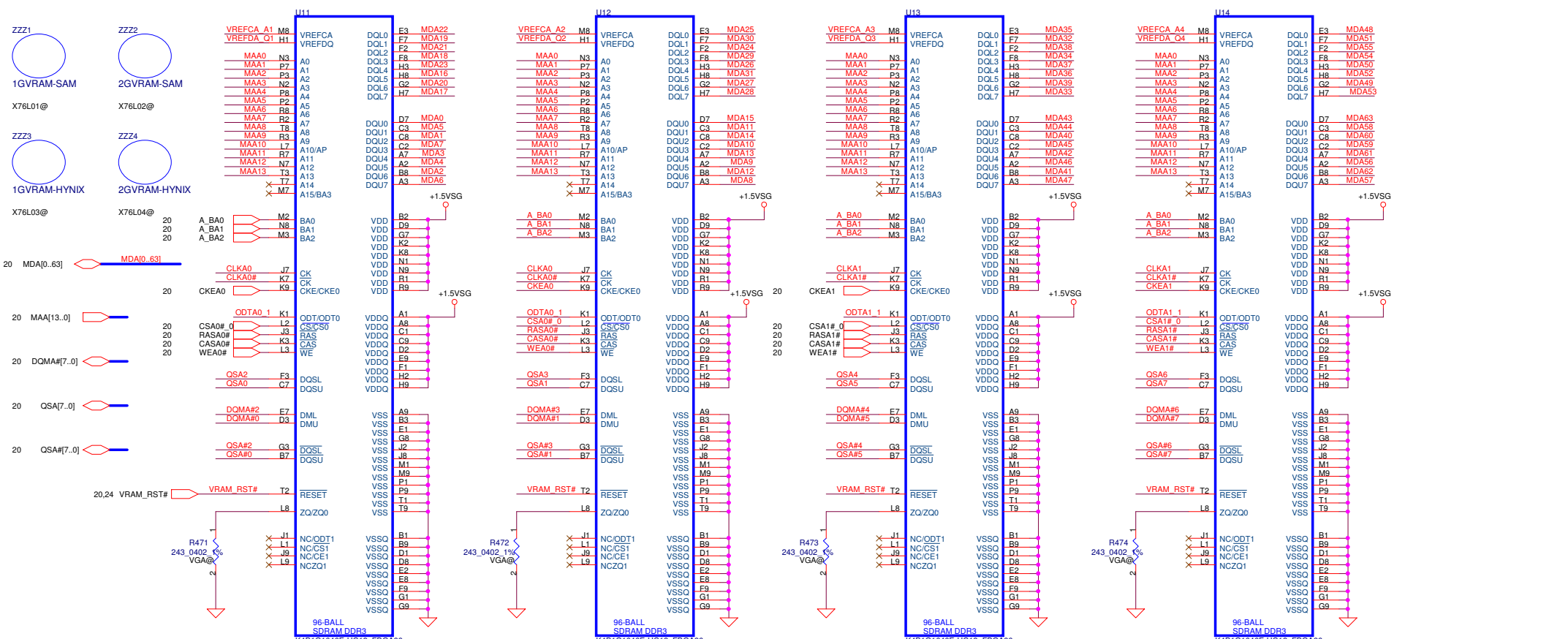
Seymour/Whistler :  
 DPA\_VDD10,DPB\_VDD10 can combian to DPAB\_VDD10  
 DPC\_VDD10,DPD\_VDD10 can combian to DPCD\_VDD10  
 DPE\_VDD10,DPD\_VDD10 can combian to DPEF\_VDD10

DPx-VSSR,DPx\_PVSS can combian to DP\_VSSR (Manhattan should have individual GND) where x is A,B,C,D,E,F

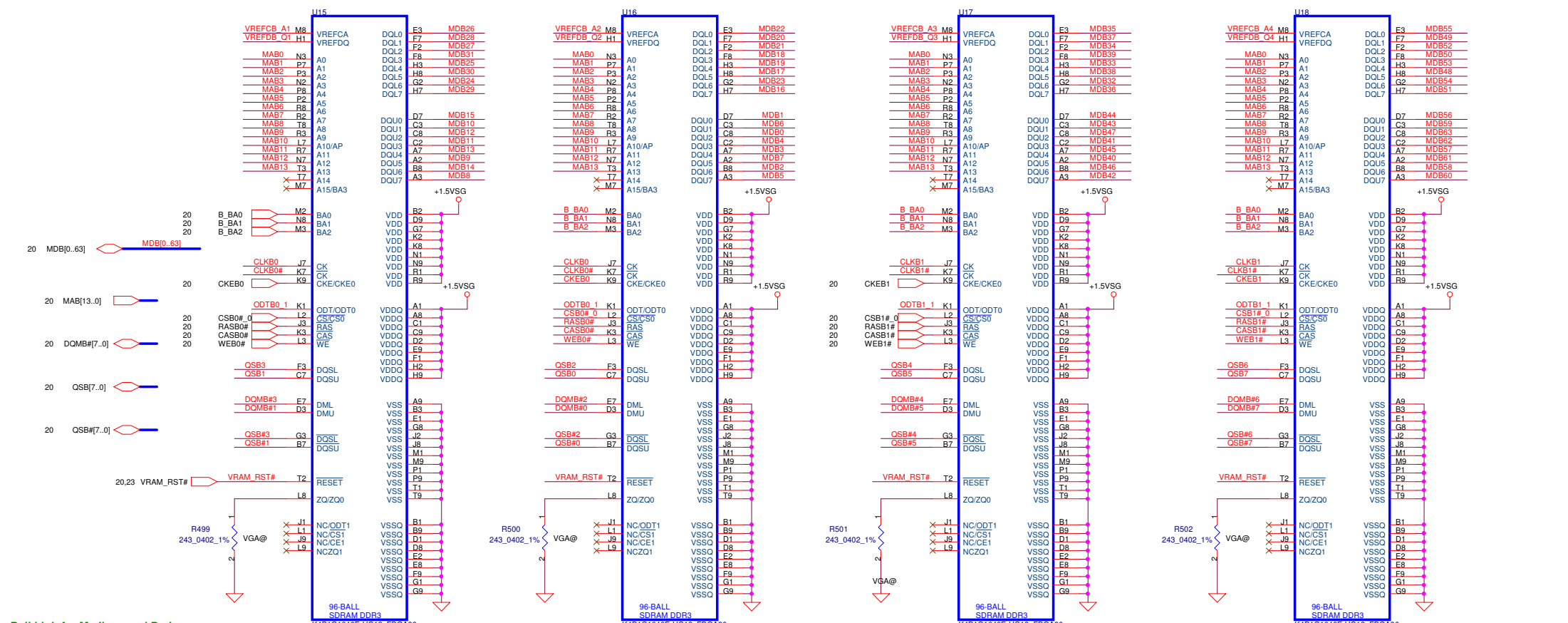
Park/Madison :AL21left NC  
 Seymour/Whistler:  
 AL21:PX\_EN use to control discreate GPU regulators for power express BACO mode  
 Support BACO:  
 output High3.3V:turn off regulators (BACO mode on)  
 output Low0V:turn on regulators (BACO mode off) need PD resistor  
 No support BACO:  
 left NC



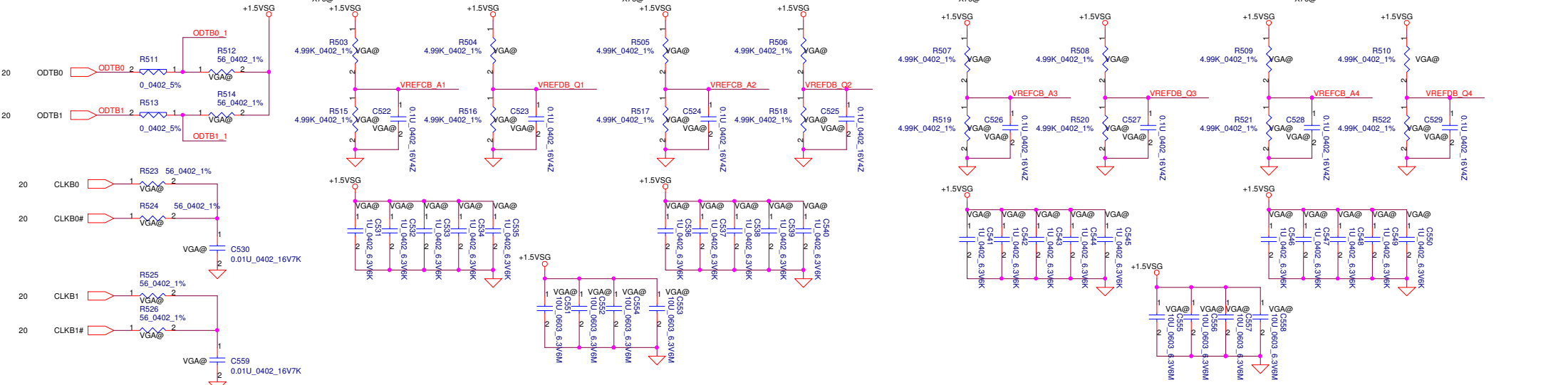
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Issued Date	2011/04/25	Deciphered Date	2012/04/25	Vancouver Power/GND	
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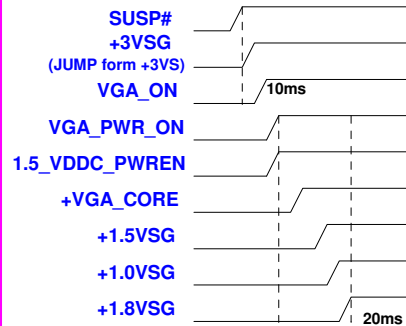
Pull high for Madison and Park...



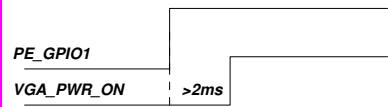
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**Power Sequence of Whistler and Seymour**



For PX sequence, >2mS delay is required between PE\_GPIO1 and VGA\_PWR\_ON

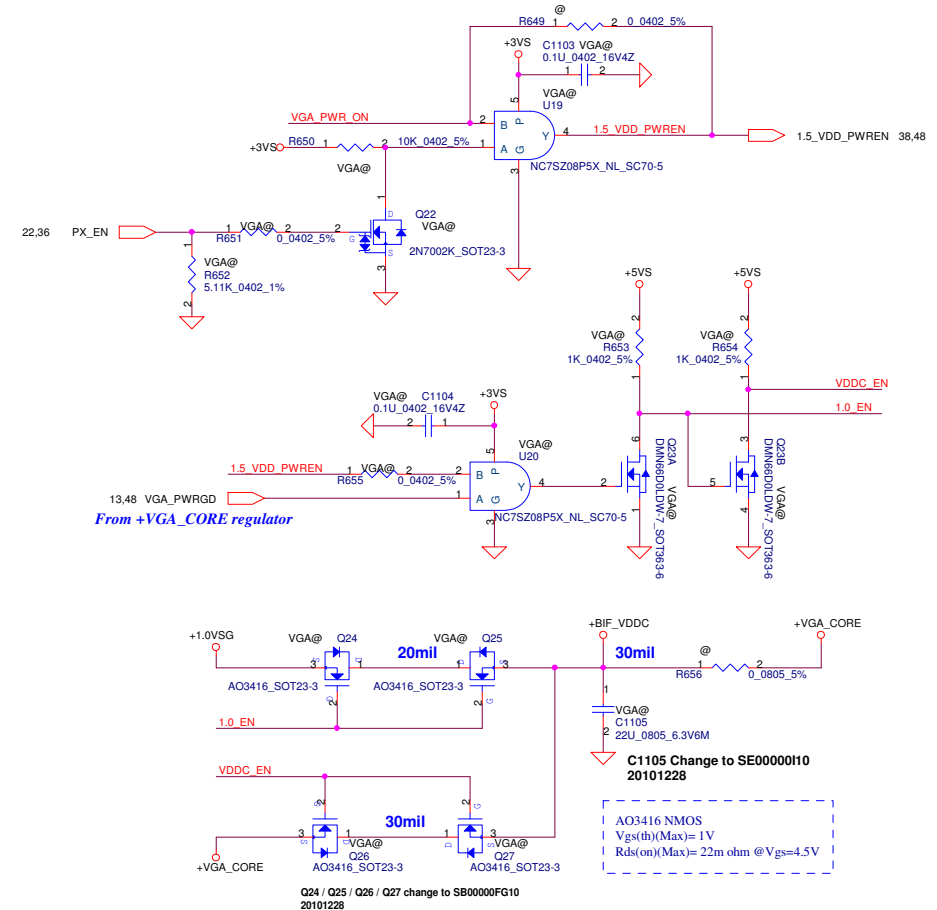
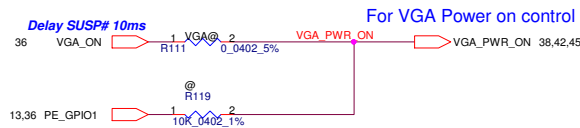


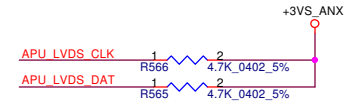
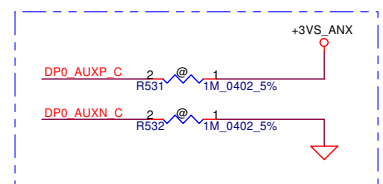
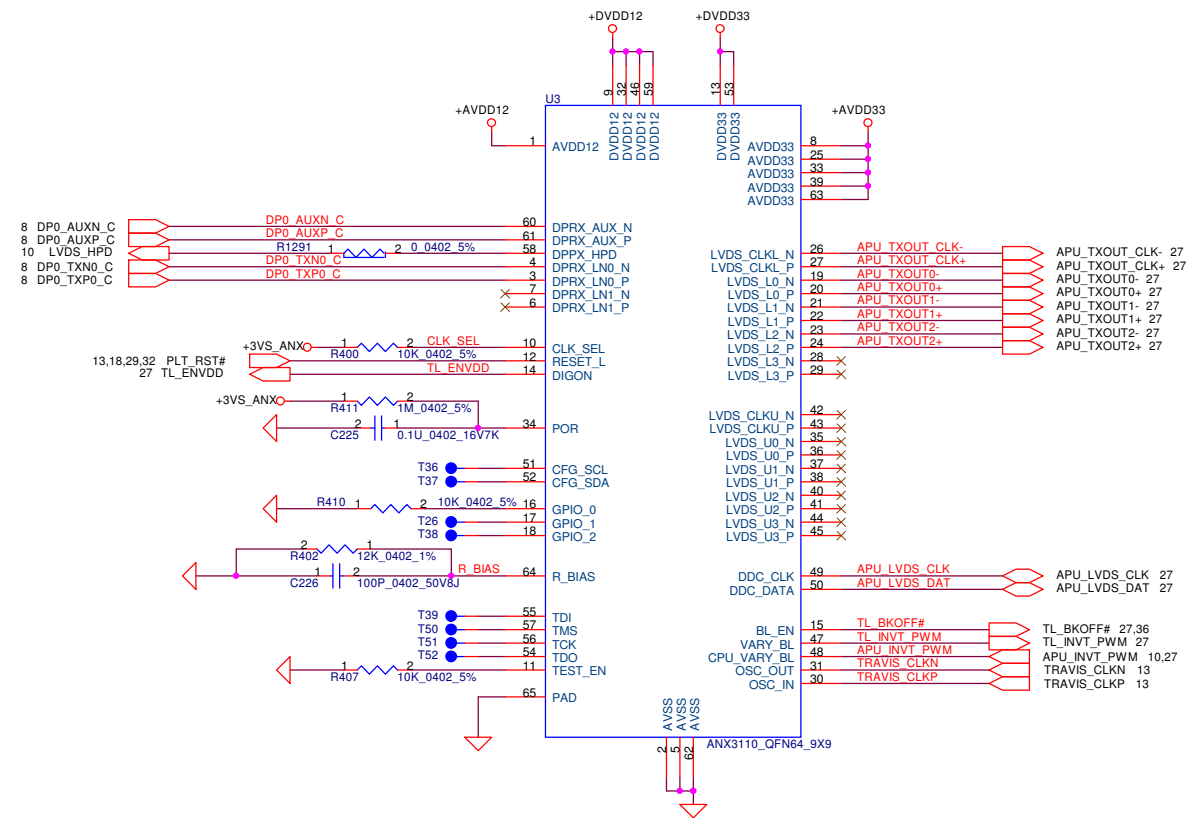
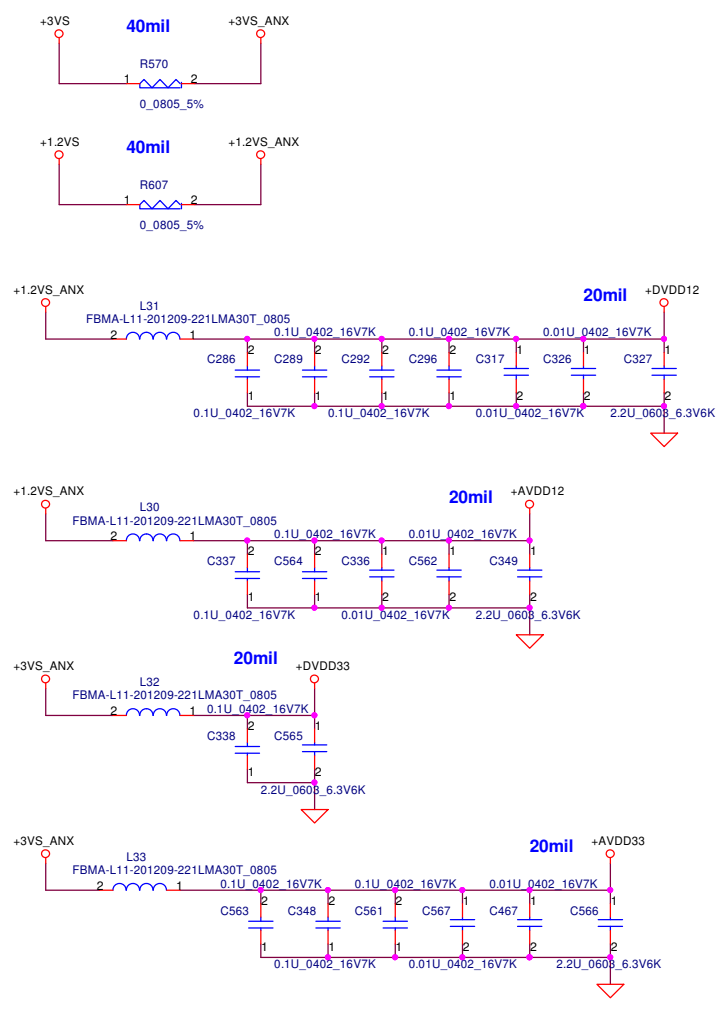
**VGA Muxless with BACO Status Mapping table**

	Normal mode	BACO mode
PX_EN	0	1
1.5_VDDC_PWREN	1	0
VDDC_EN	1	0
1.0_EN	0	1
+3.3VSG	ON	ON
+1.8VSG	ON	ON
+1.0VSG	ON	ON
+VGA_CORE	ON	OFF
+1.5VSG	ON	OFF
+BIF_VDDC	+VGA_CORE	+1.0VSG

**VGA Power Enable Signal Mapping table**

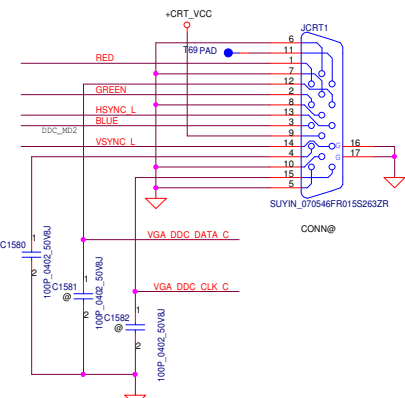
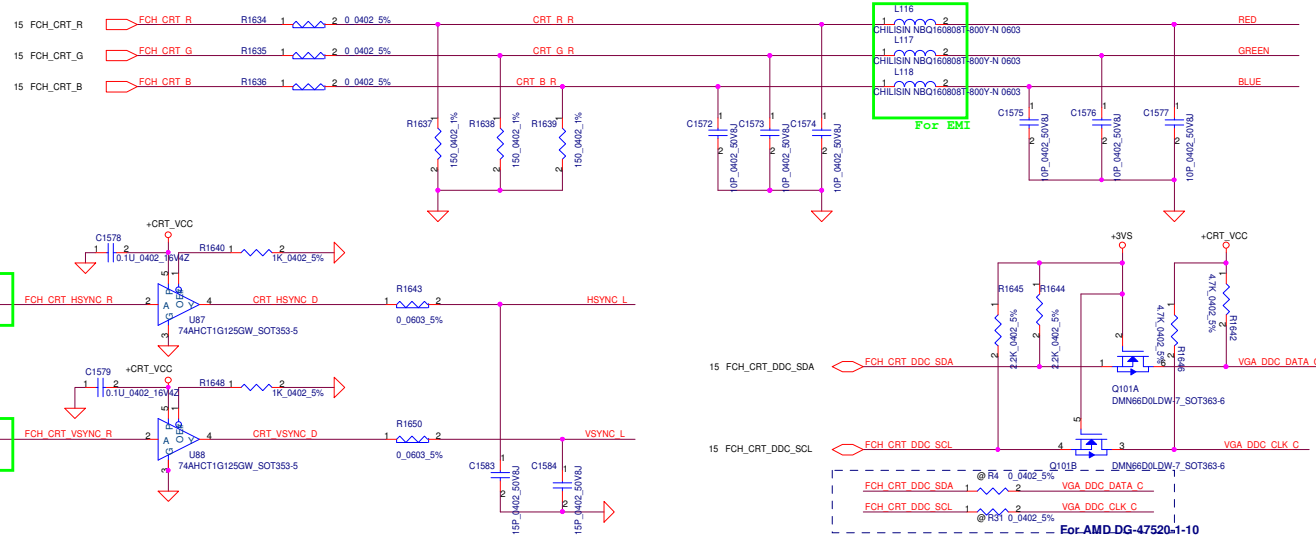
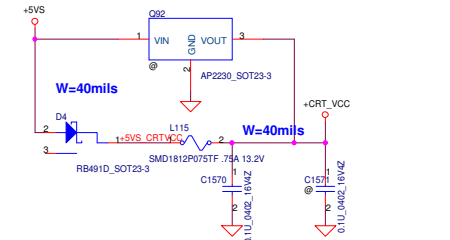
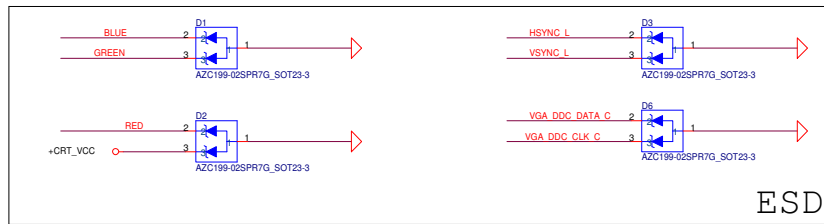
VGA_PWR_ON source signal	Whistler
+3.3VSG	VGA_ON
+1.8VSG	SUSP#
+1.0VSG	VGA_PWR_ON
+VDDCI	Combine with +VGA_CORE
+VGA_CORE	1.5_VDDC_PWREN
+1.5VSG	1.5_VDDC_PWREN





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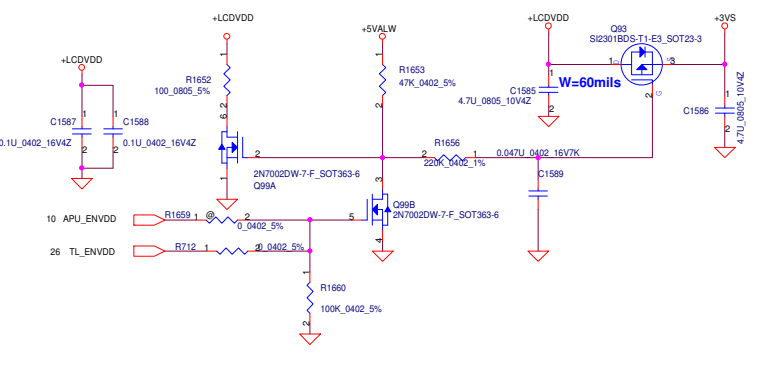
# CRT



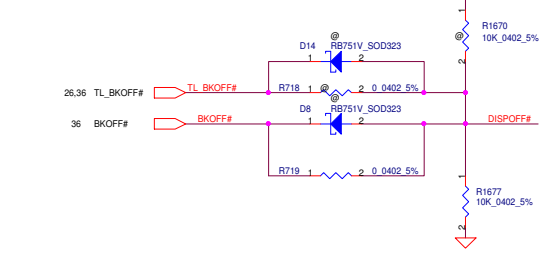
Close to APU

For AMD.DG-47520-1-10

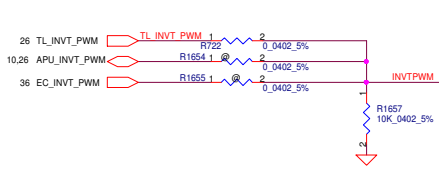
## Panel LCDVDD Control



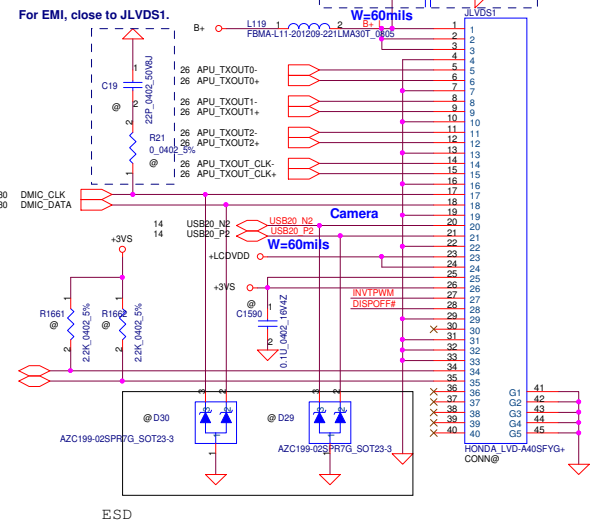
## Panel Backlight Control



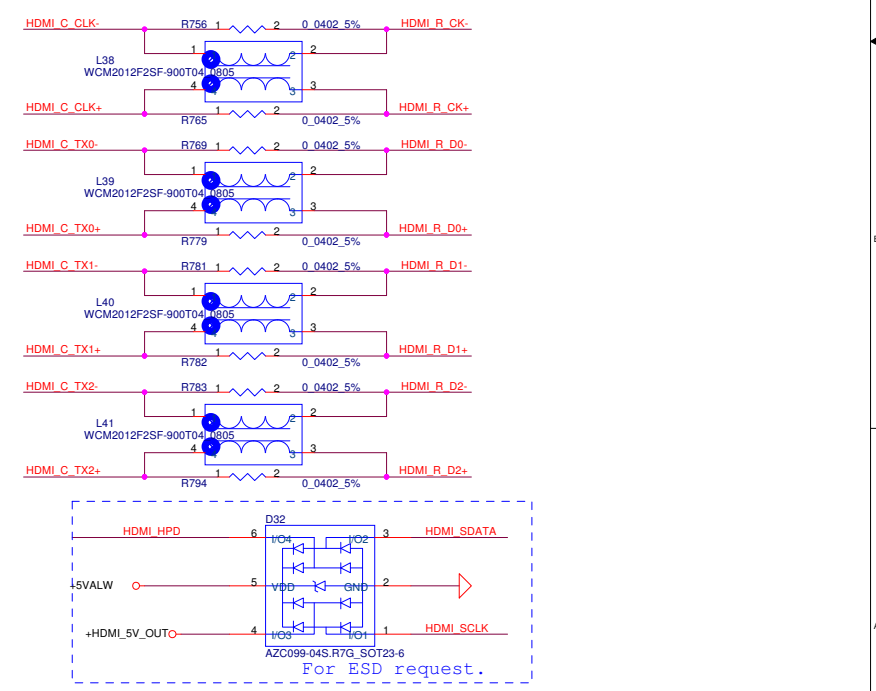
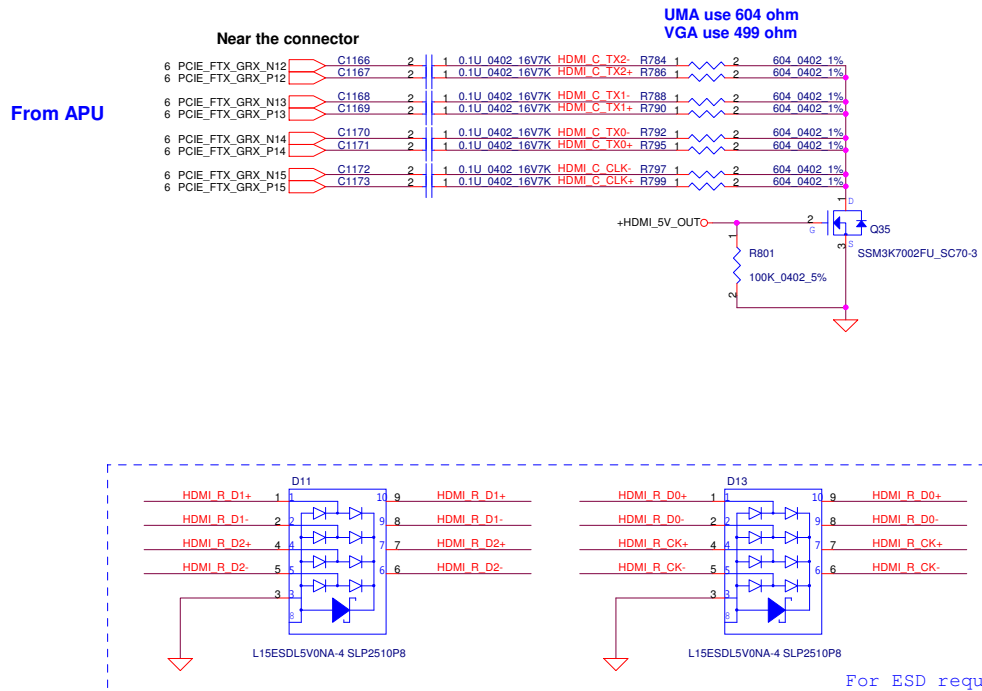
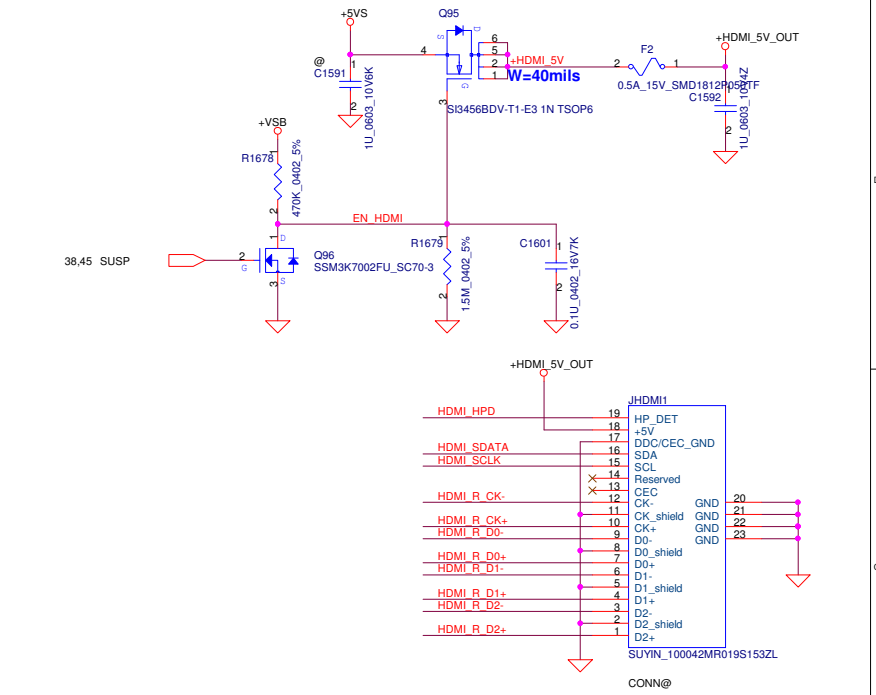
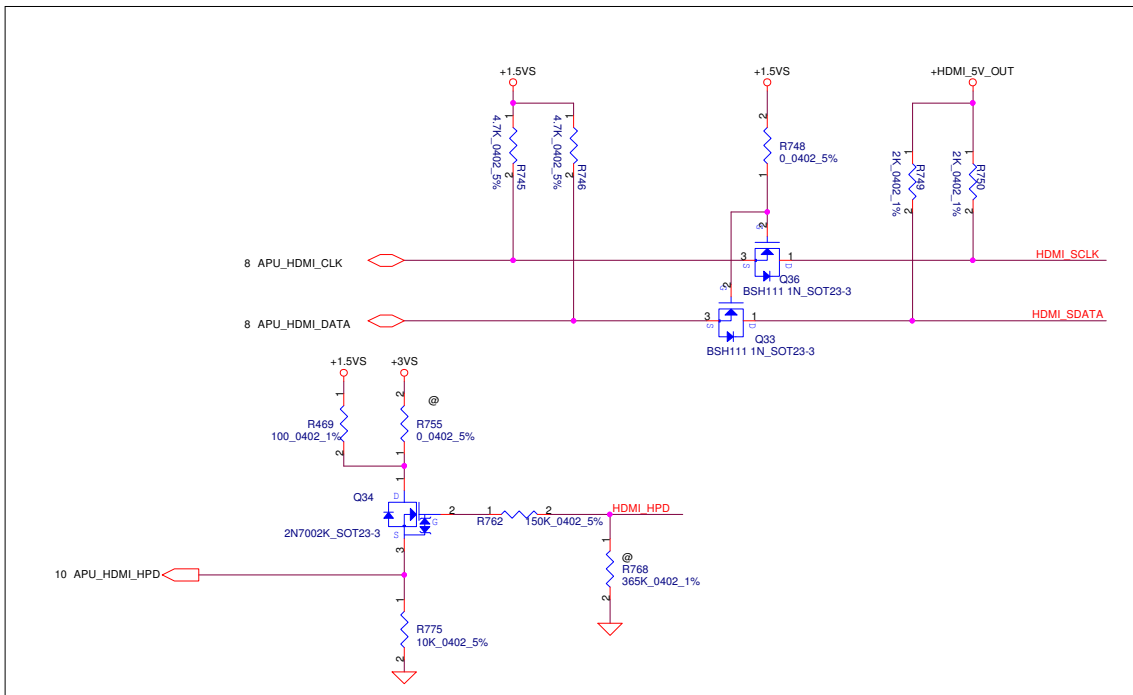
## Panel PWM Control



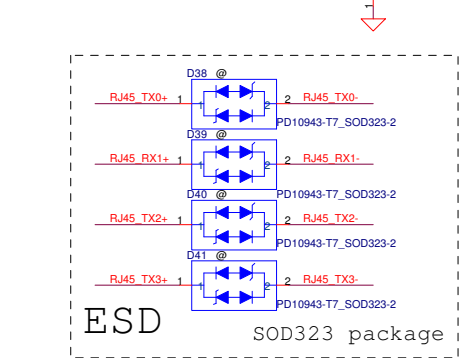
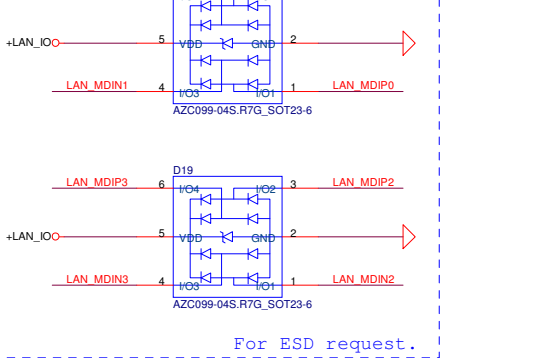
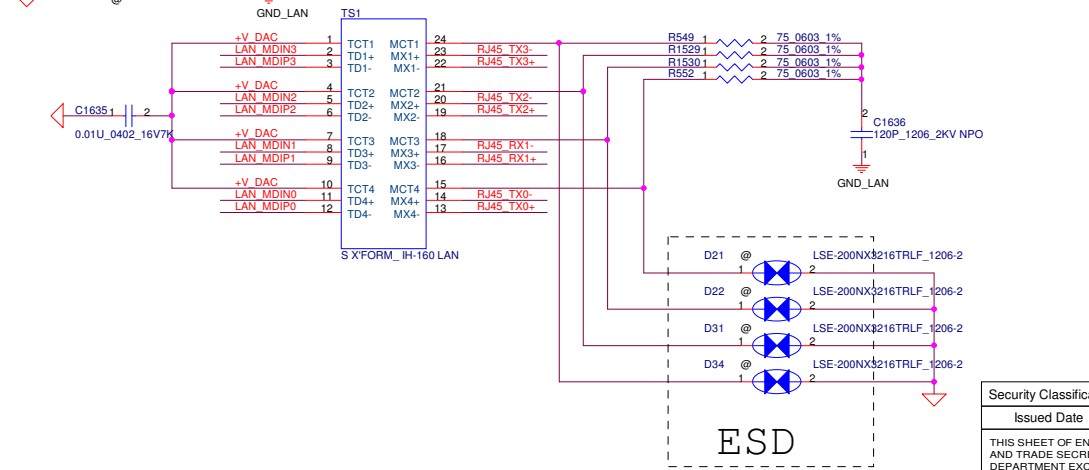
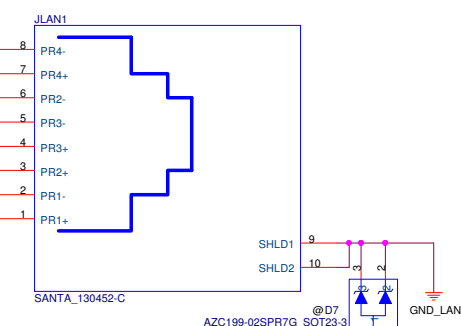
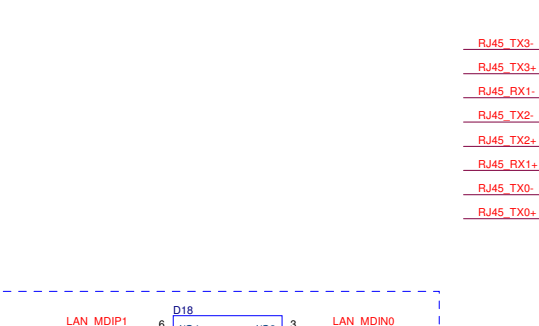
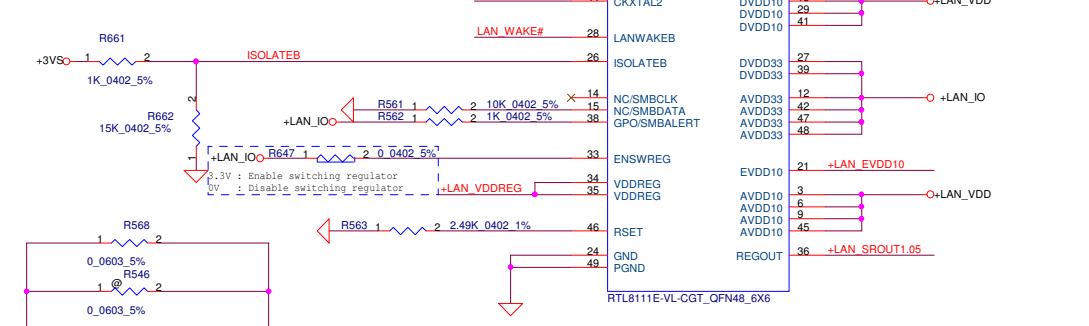
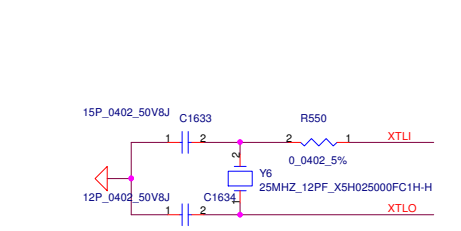
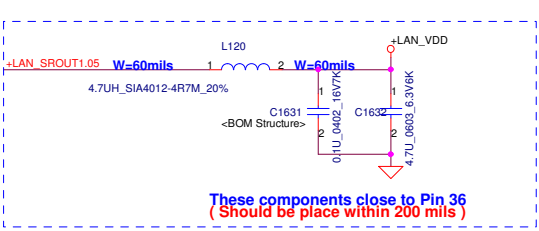
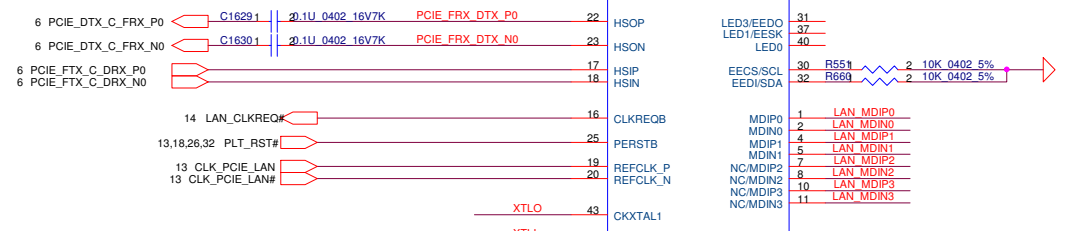
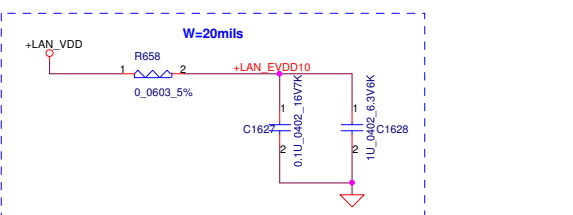
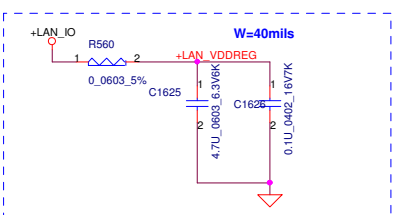
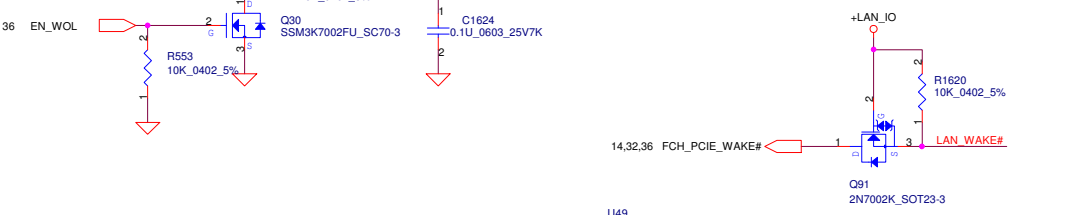
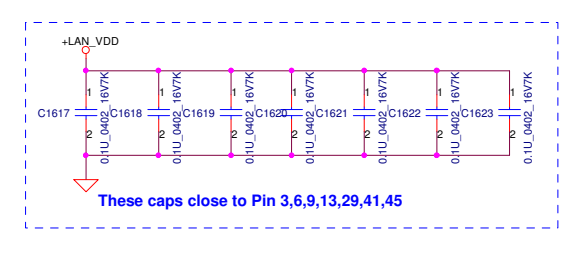
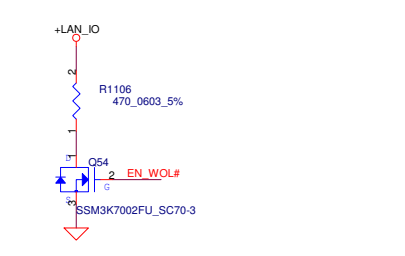
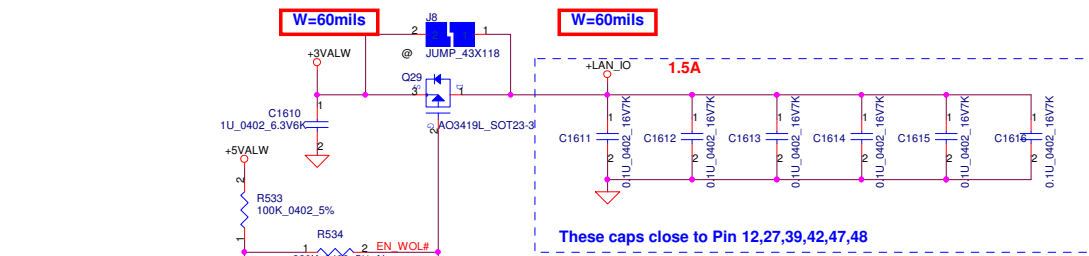
For EMI, close to JLVDS1.



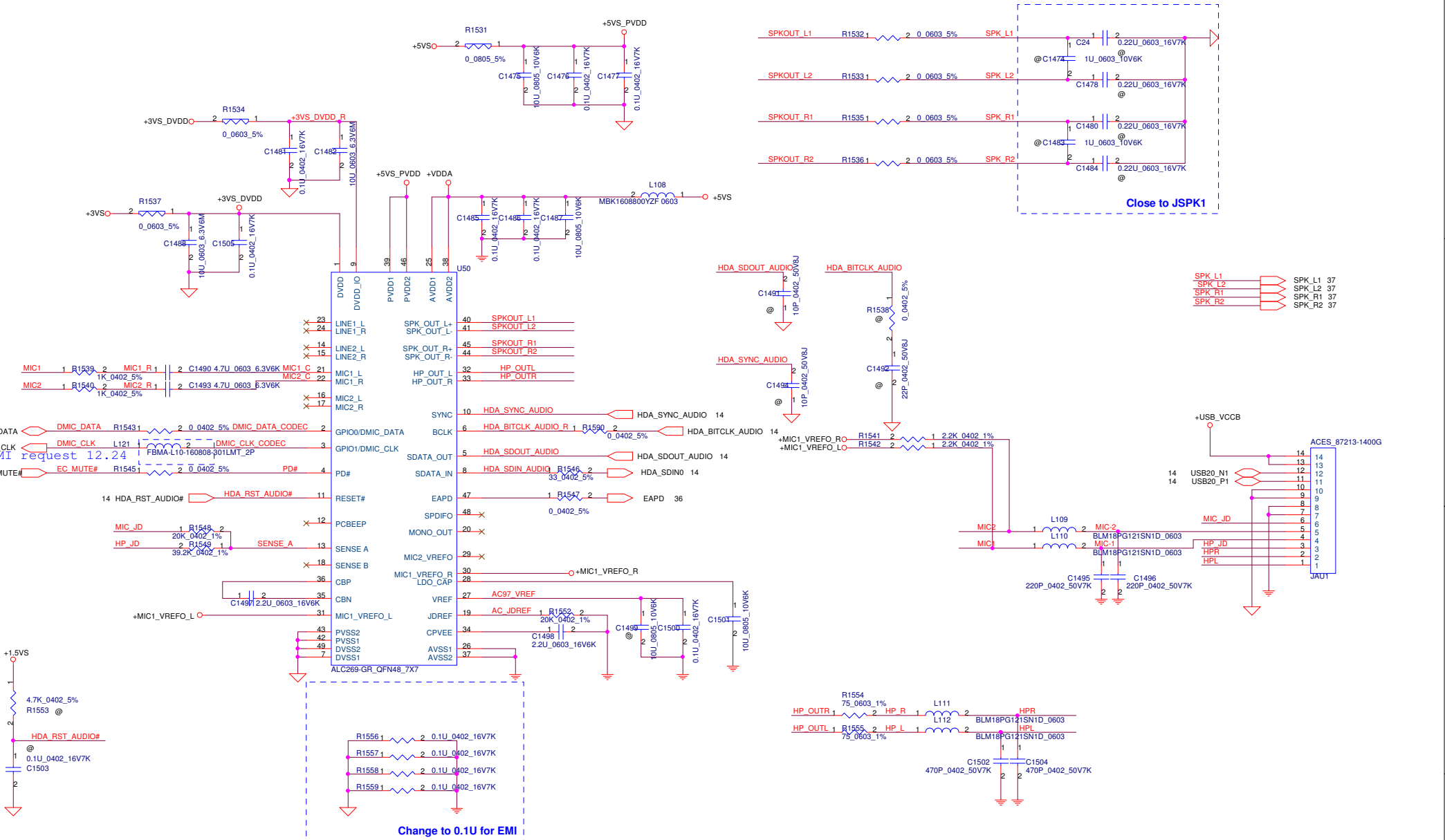
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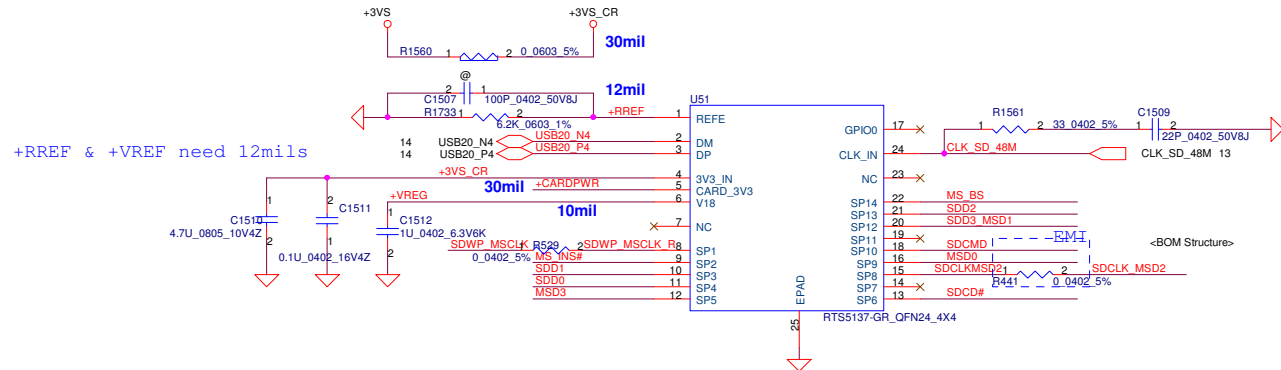


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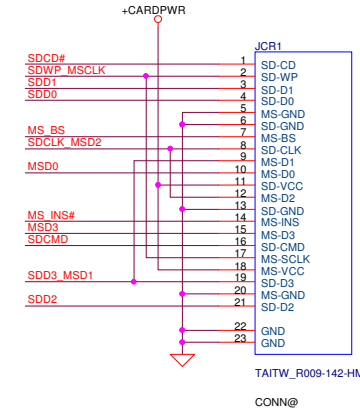
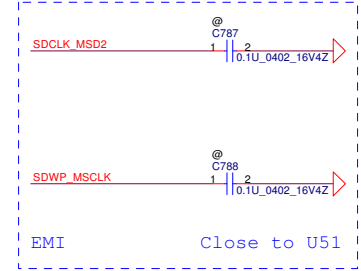
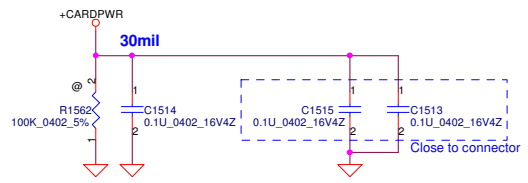


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# Card Reader RTS5137 (only SD/MMC/MS function)



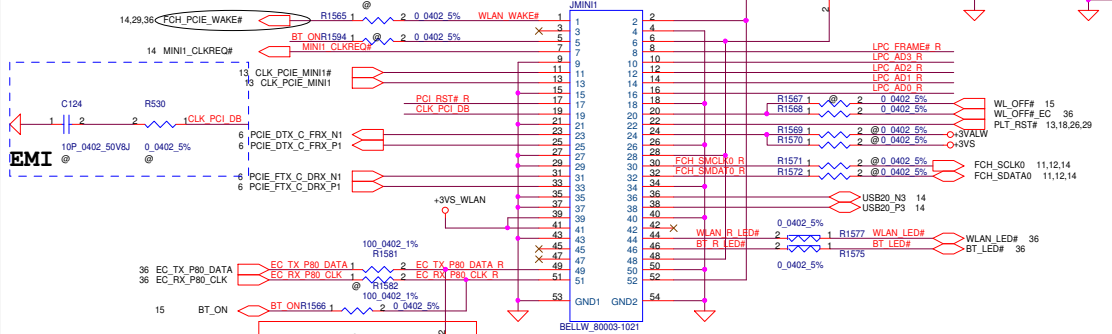
# Card Reader Connector



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# Mini-Express Card for WLAN/WiMAX(Half)

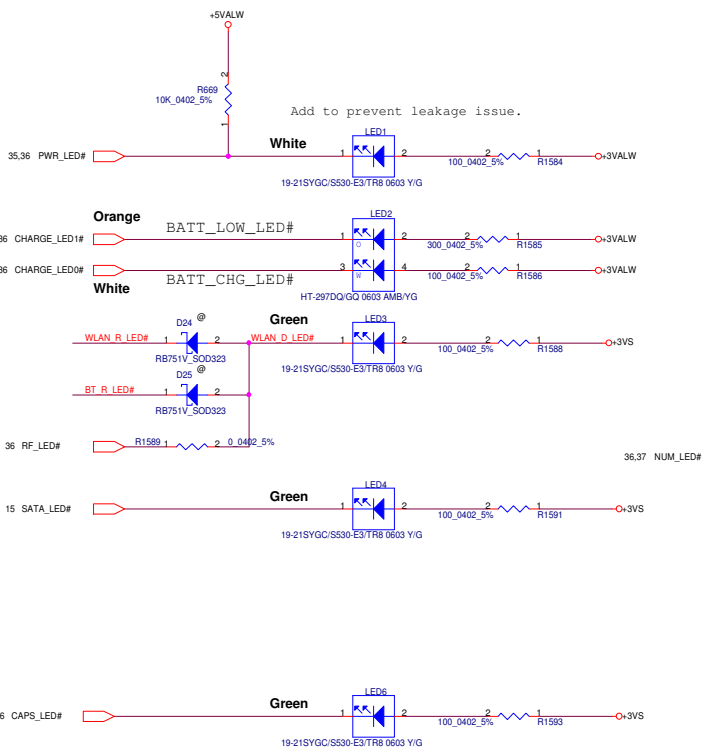
## Mini-Express Card(WLAN/WiMAX)



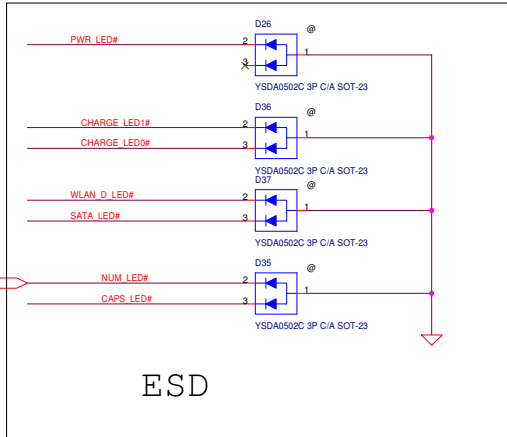
**Reserve for SW mini-pcie debug card.**  
**Series resistors closed to KBC side.**

LPC_FRAME# R	R1573	1	2 @ 0.0402 5%	LPC_FRAME#	LPC_FRAME#	13,36
LPC_AD3 R	R1574	1	2 @ 0.0402 5%	LPC_AD3	LPC_AD3	13,36
LPC_AD2 R	R1576	1	2 @ 0.0402 5%	LPC_AD2	LPC_AD2	13,36
LPC_AD1 R	R1578	1	2 @ 0.0402 5%	LPC_AD1	LPC_AD1	13,36
LPC_AD0 R	R1579	1	2 @ 0.0402 5%	LPC_AD0	LPC_AD0	13,36
PCI_RST# R	R1580	1	2 @ 0.0402 5%	PLT_RST#	LPC_AD0	13,36
CLK_PCIE_DB				CLK_PCIE_DB		13

## LED

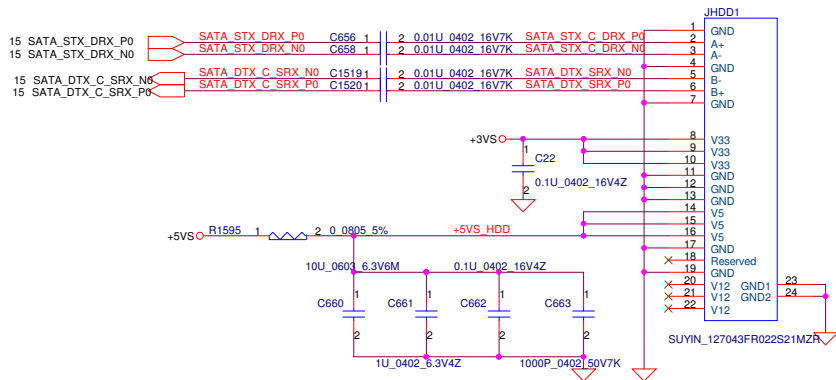


## ESD

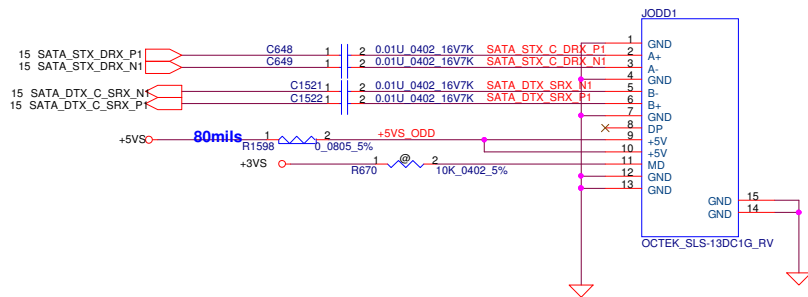




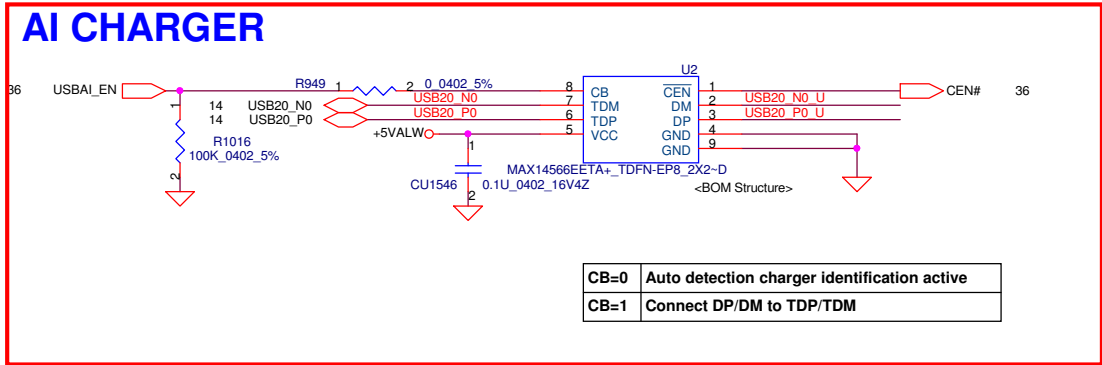
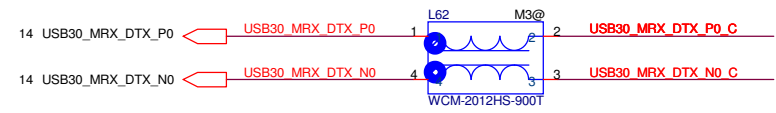
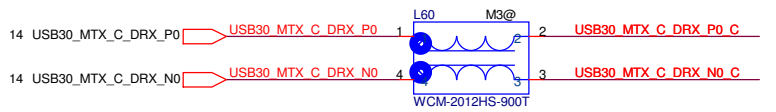
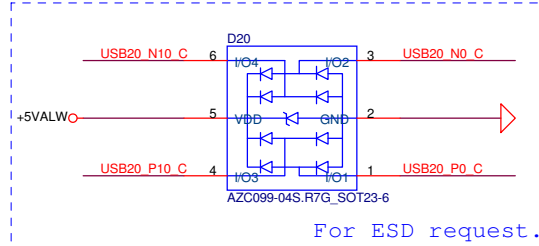
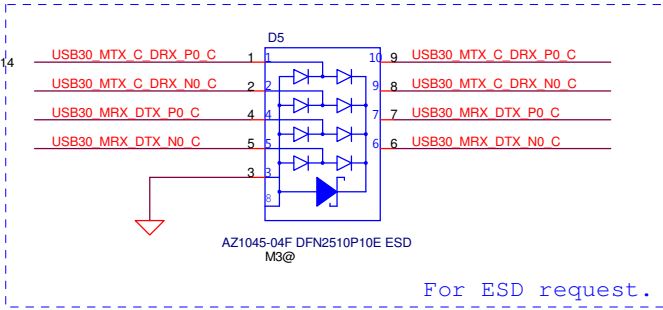
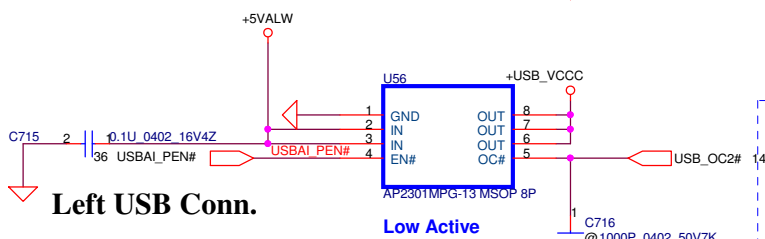
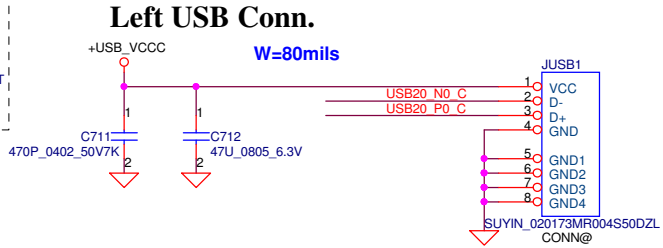
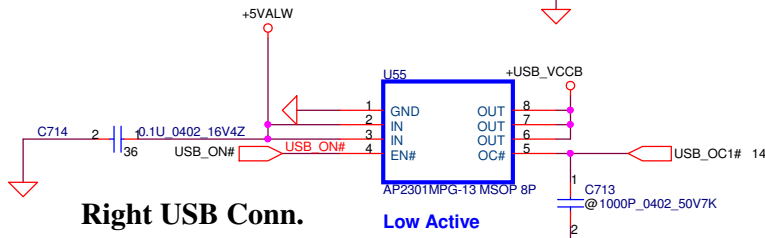
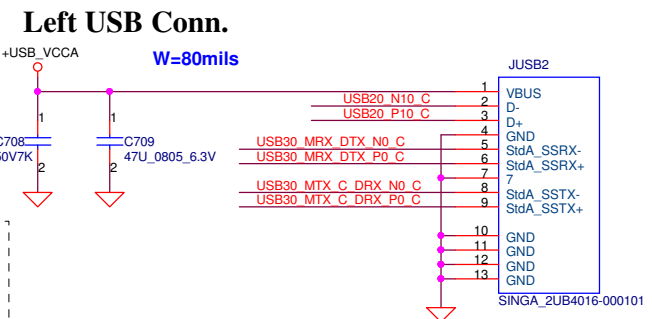
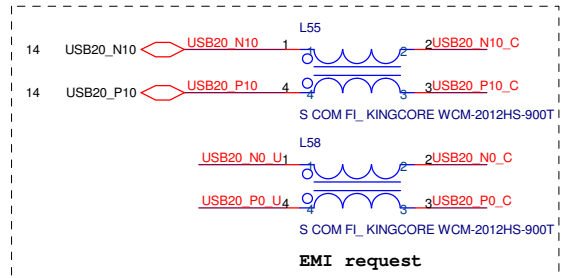
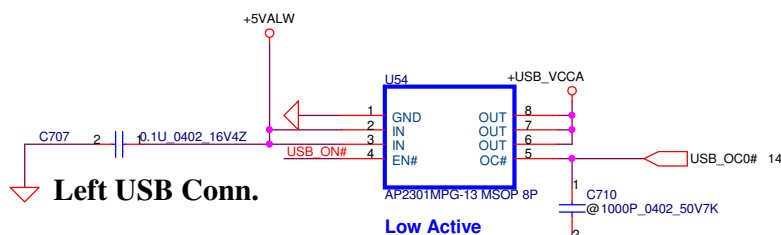
### SATA HDD Conn.



### SATA ODD FFC Conn.



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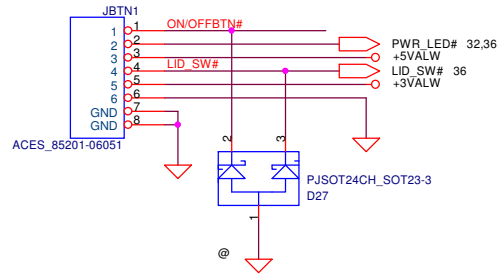
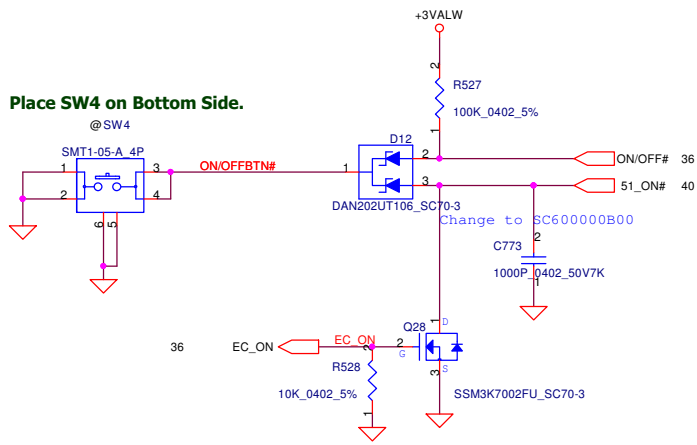


CB=0	Auto detection charger identification active
CB=1	Connect DP/DM to TDP/TDM

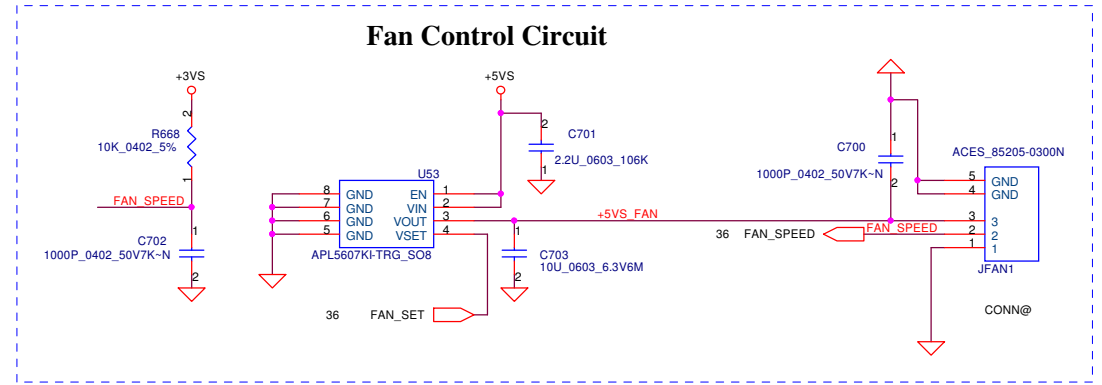
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Issued Date	2011/04/25	Deciphered Date	2012/04/25	Title	P32-USB/BT/USBsub
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File Name	Document Number	Rev			
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# ON/OFF switch Power Button

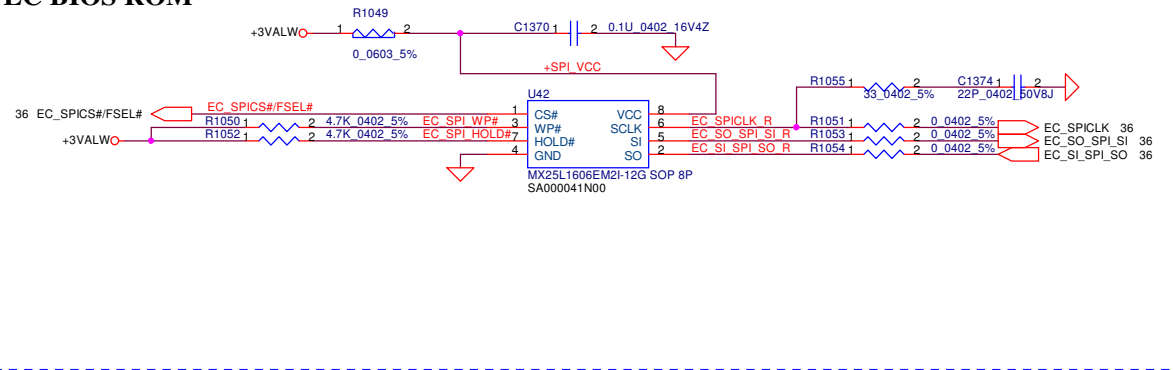
Place SW4 on Bottom Side.  
@ SW4



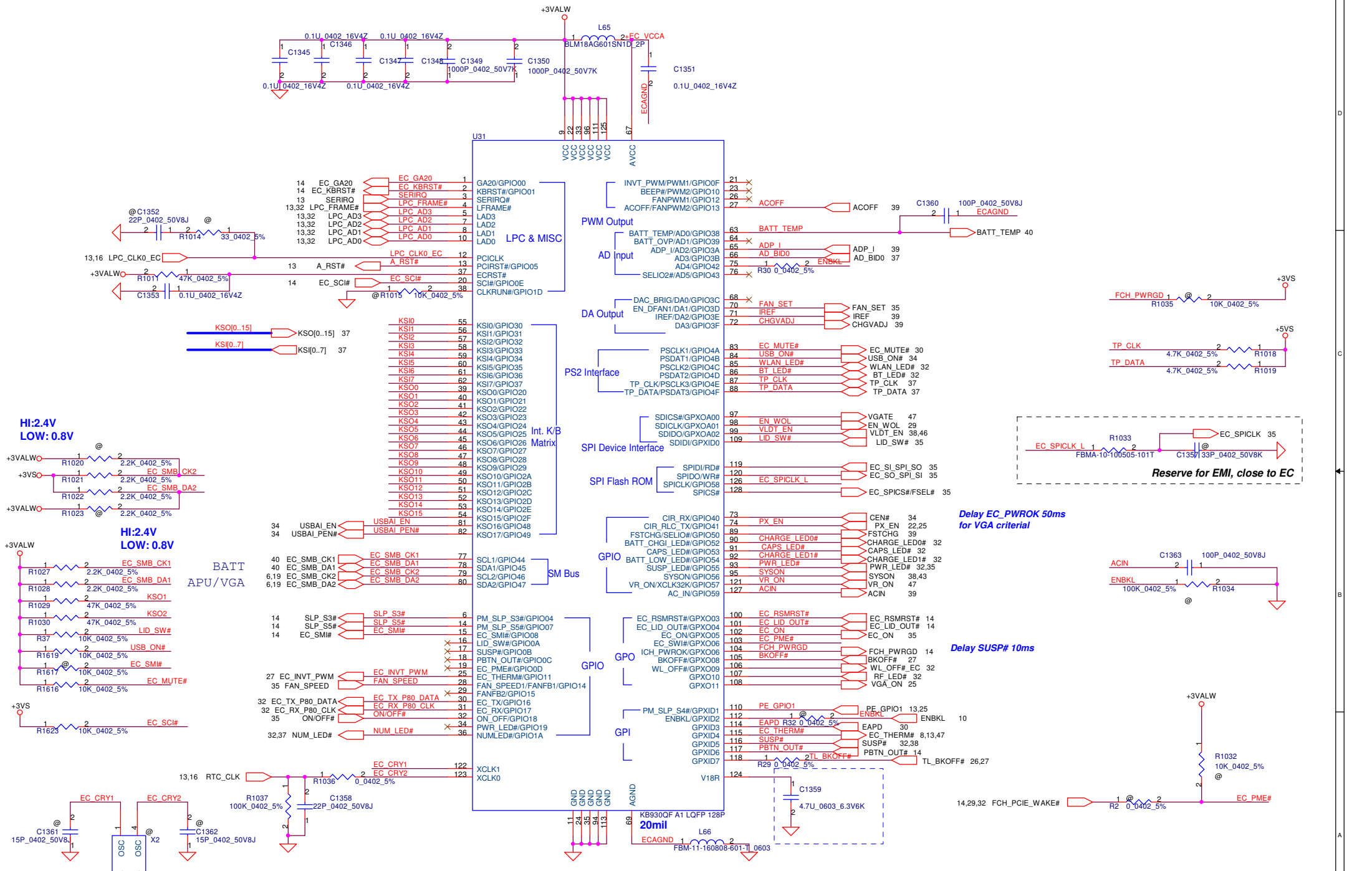
# Fan Control Circuit



# EC BIOS ROM



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Issued Date	2011/04/25	Deciphered Date	2012/04/25	P31-KB /SW/TP/Lid	
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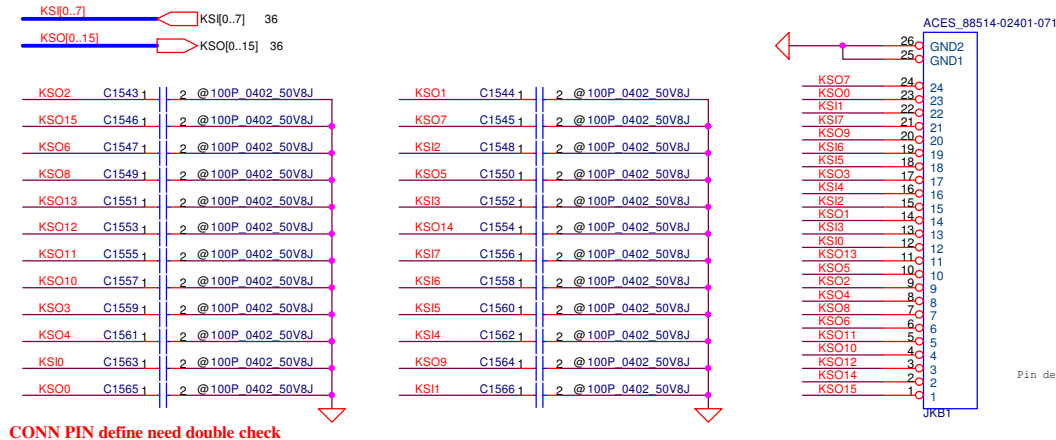
Reserve for EMI, close to EC

Delay EC\_PWROK 50ms for VGA criteria

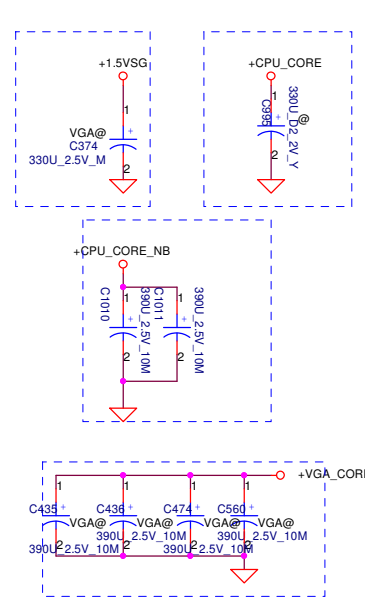
Delay SUSP# 10ms

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Size	Document Number			Rev		
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### INT\_KBD Conn.

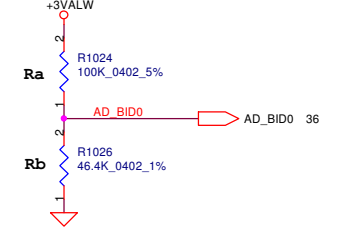


CONN PIN define need double check

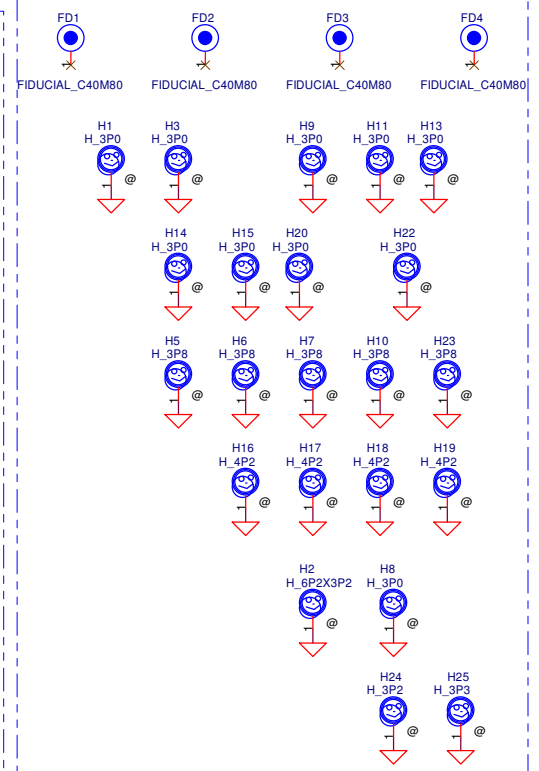
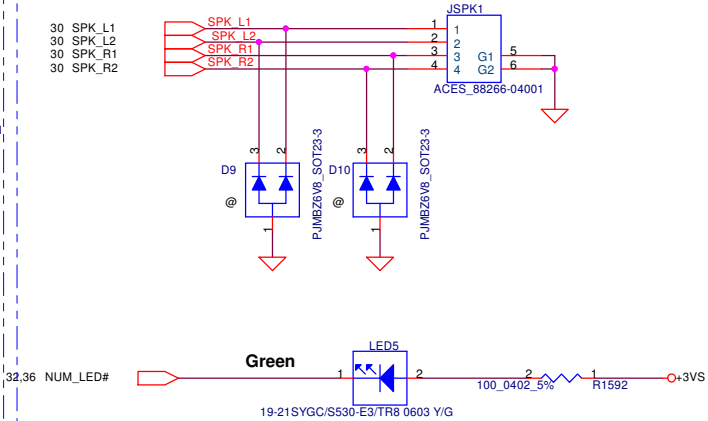
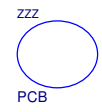
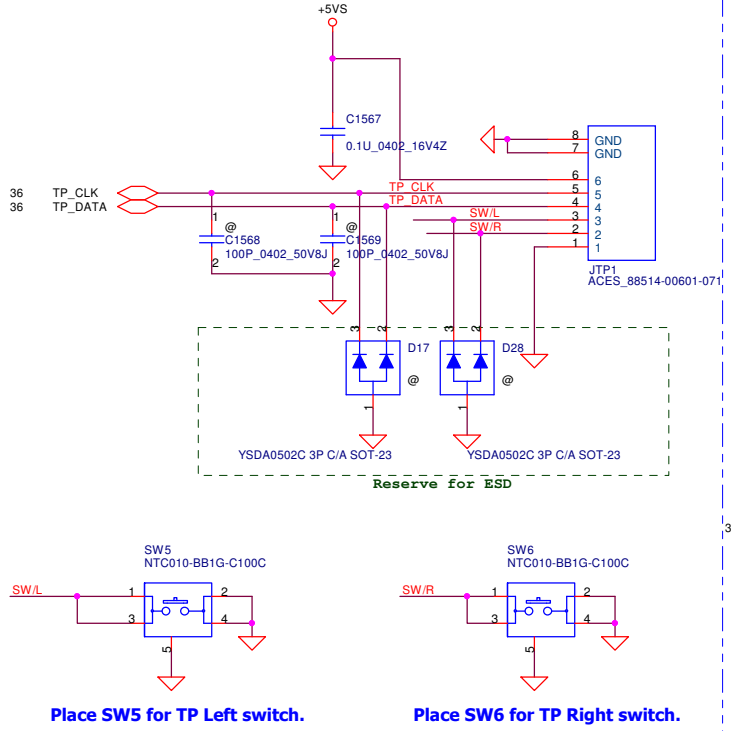


ID	BRD ID	Ra	Rb	Vab
0	R01 SR	100K	26.1K	0.683V
1	R02 ER	100K	34.8K	0.851V
2	R10 PR	100K	46.4K	1.045V
3	Reserve	100K	56.2K	1.187V

### Analog Board ID definition

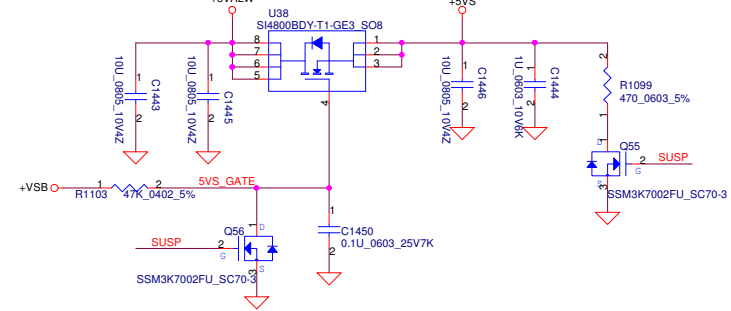


### To TP/B Conn.

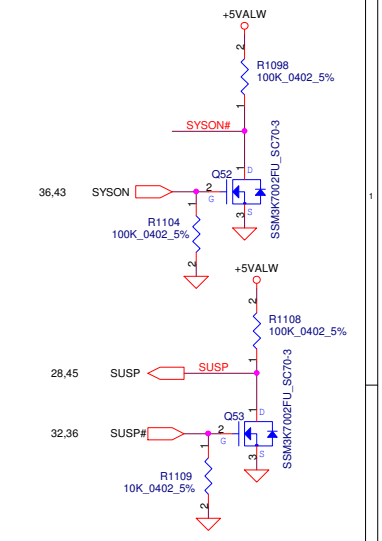
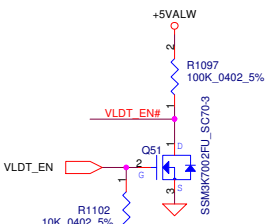
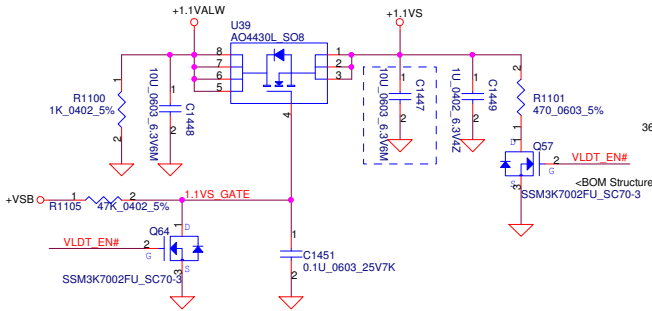


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			P33-Other IO/USB (right)	
Size Custom	Document Number	Date: Monday, April 25, 2011		Rev 1.0
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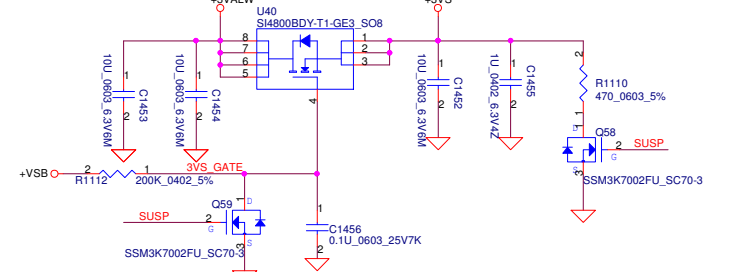
**+5VALW TO +5VS (5A)**



**+1.1VALW TO +1.1VS (1.1A)**

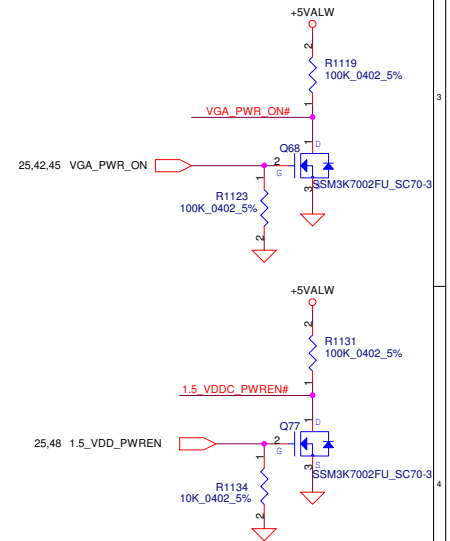
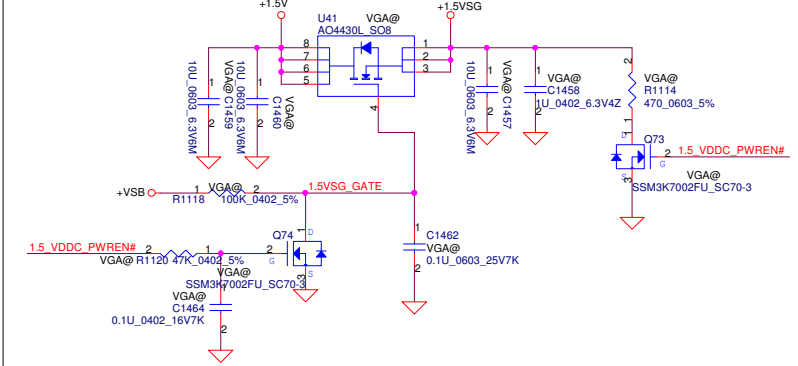


**+3VALW TO +3VS (3.3A)**

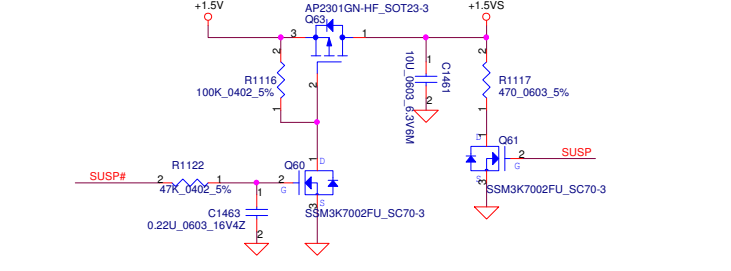


**VGA Power**

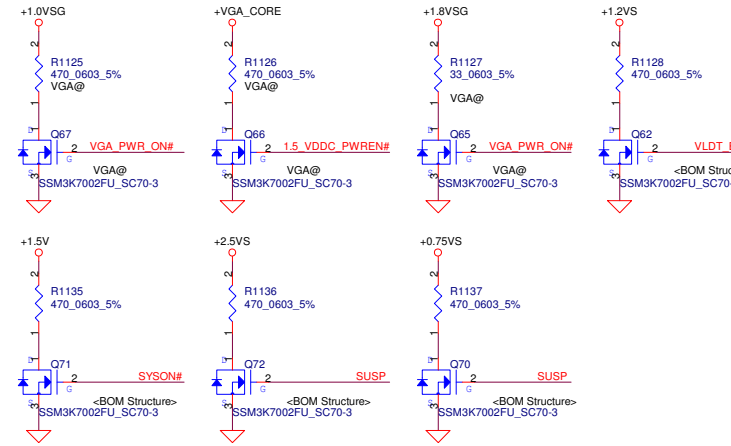
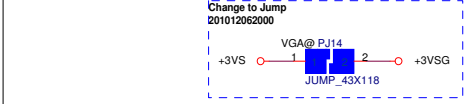
**+1.5V to +1.5VSG (1.5A)**



**+1.5V TO +1.5VS (1.5A)**



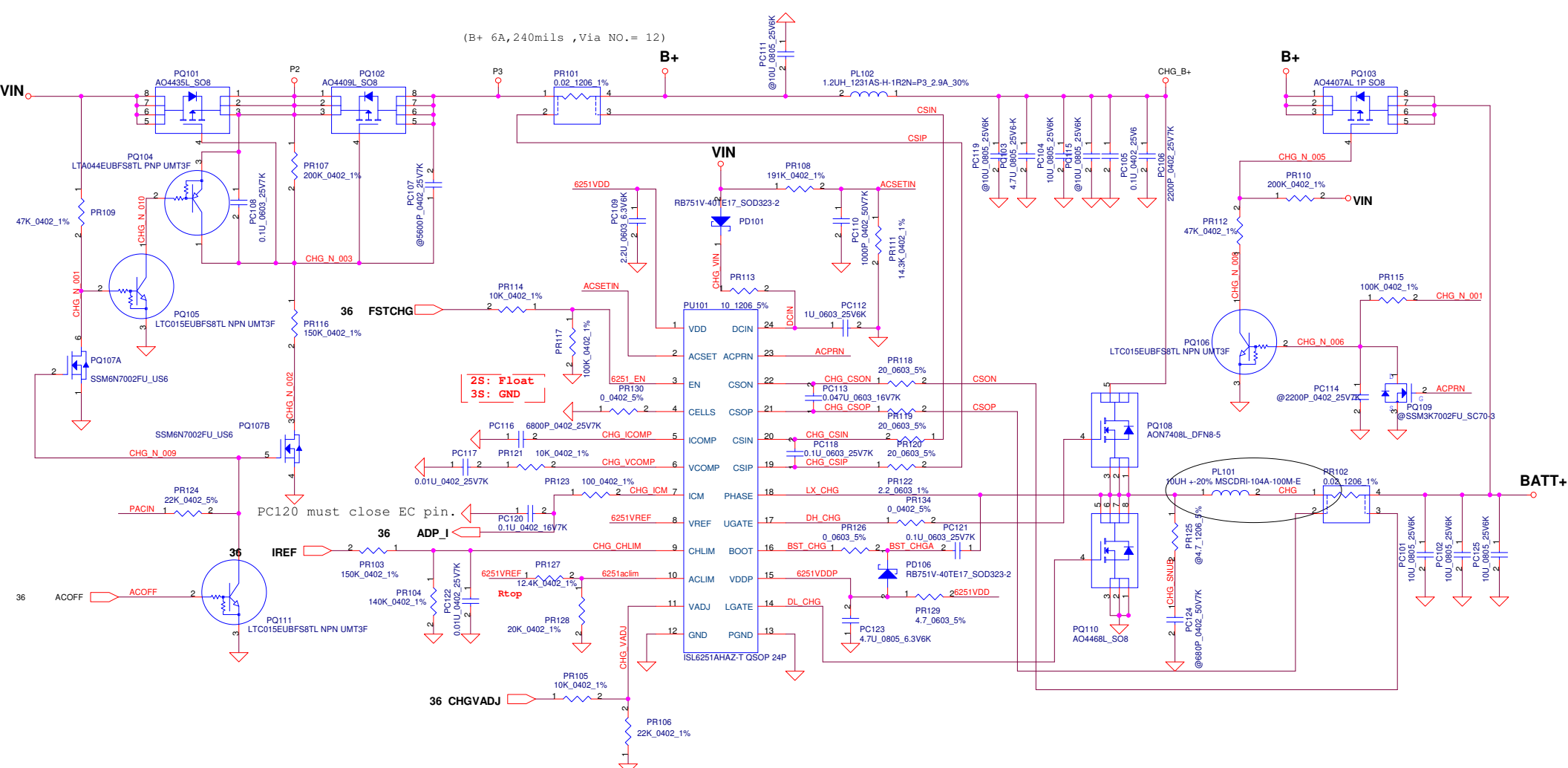
**+3VS to +3VSG (3.3A)**



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Compal Electronics, Inc.	
DC Interface	
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(B+ 6A,240mils ,Via NO.= 12)



2S: Float  
3S: GND

36 ACOFF

36 IREF

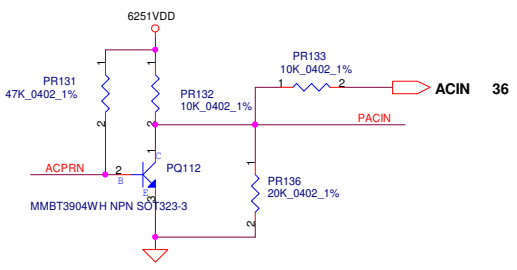
36 CHGVADJ

CP= 85%\*I<sub>ada</sub>;  
I<sub>ada</sub>=0~4.737A (90W); CP=4.03A; where R<sub>acdet</sub>=0.020ohm, where R<sub>top</sub>=12.4K  
90W for Dis: R<sub>top</sub>:SD00000AJ80  
I<sub>ada</sub>=0~3.421A (65W); CP=2.91A; where R<sub>acdet</sub>=0.020ohm, where R<sub>top</sub>=226K  
65W for UMA: R<sub>top</sub>:SD034226380  
Astro2010\_01\_15 need confirm P/N

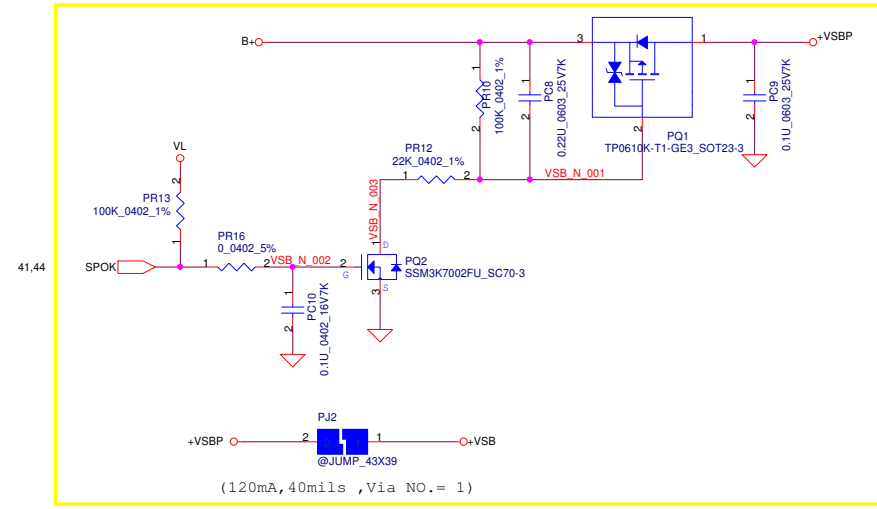
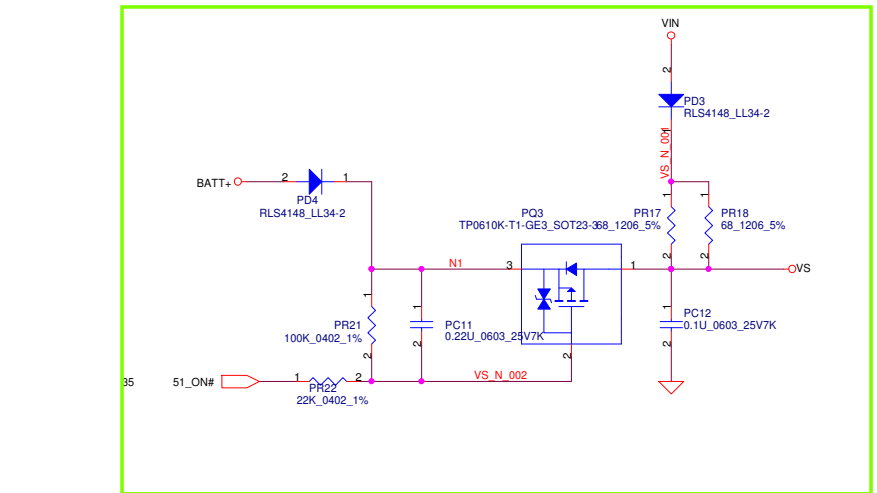
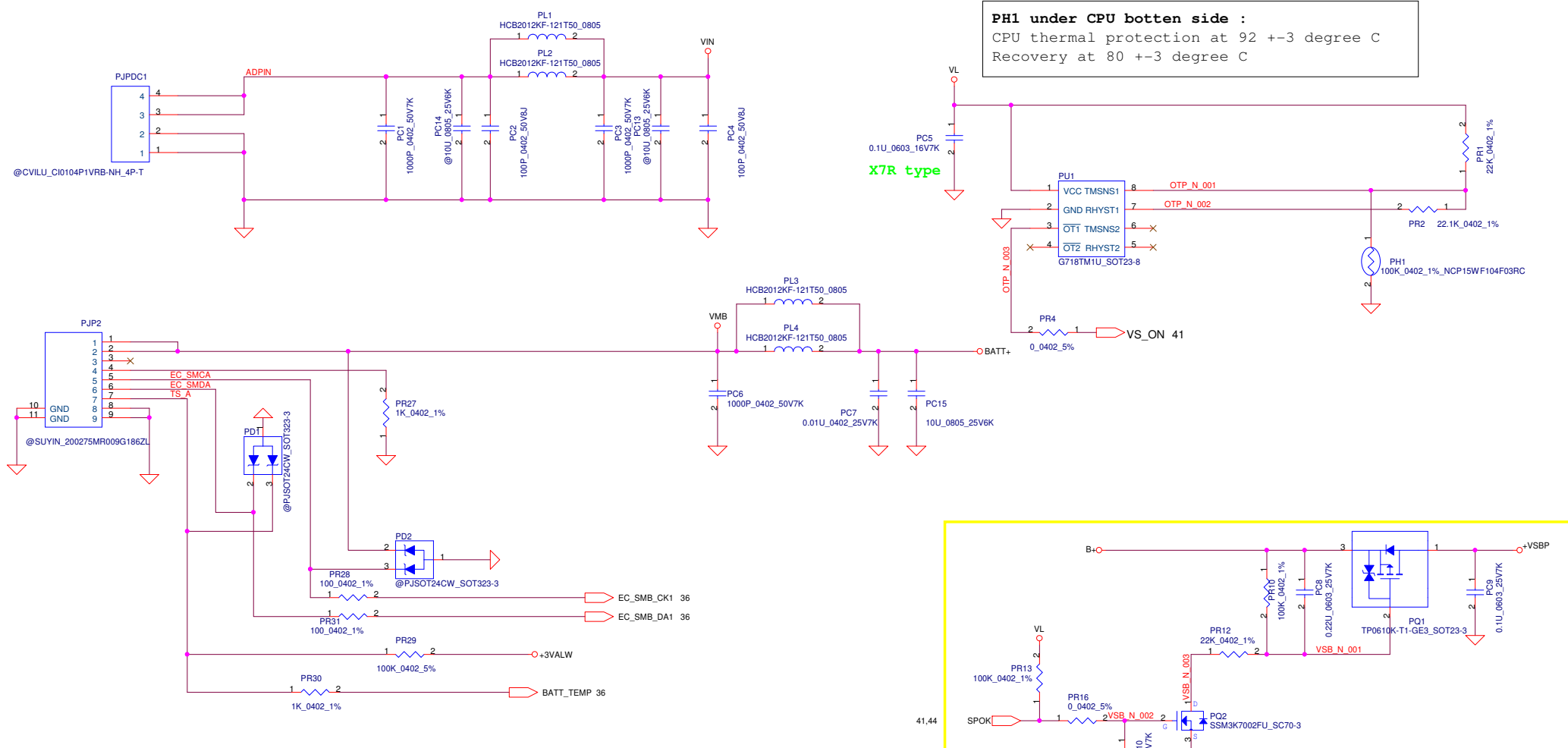
CP mode  
V<sub>acLim</sub>=VREF\*(R<sub>bot</sub>//R<sub>internal</sub>/(R<sub>top</sub>//R<sub>internal</sub>+R<sub>bot</sub>//R<sub>internal</sub>))  
when 90W V<sub>acLim</sub>=2.39\*(20K//152K/(20K//152K+12.4K//152K))=1.44966V  
when 65W V<sub>acLim</sub>=2.39\*(20K//152K/(20K//152K+226K//152K))=0.38914V  
I<sub>input</sub>=(1/R<sub>acdet</sub>)\*(0.05\*V<sub>acLim</sub>/VREF+0.05)  
when 90W, I<sub>input</sub>=(1/0.02)\*(0.05\*1.44966/2.39+0.05)=4.02A  
when 65W, I<sub>input</sub>=(1/0.02)\*(0.05\*0.38914/2.39+0.05)=2.92A

CC=0.25A-3A  
IREF=1.016\*I<sub>charge</sub>  
IREF=0.254V-3.048V  
VCHLIM need over 95mV

CHGVADJ=(V <sub>cell</sub> -4)/0.10627	
V <sub>cell</sub>	CHGVADJ
4V	0V
4.2V	1.882V

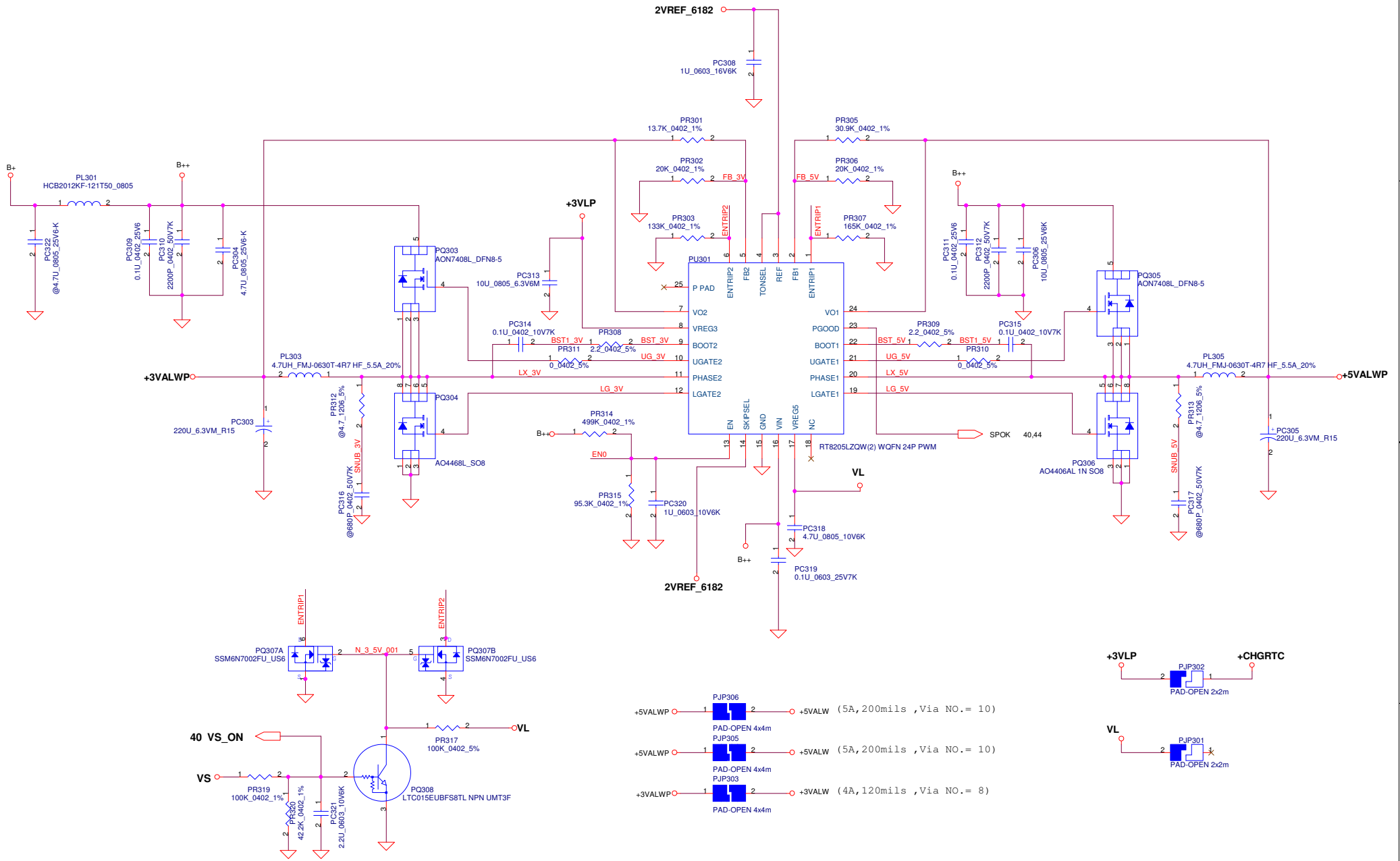


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				CHARGER	
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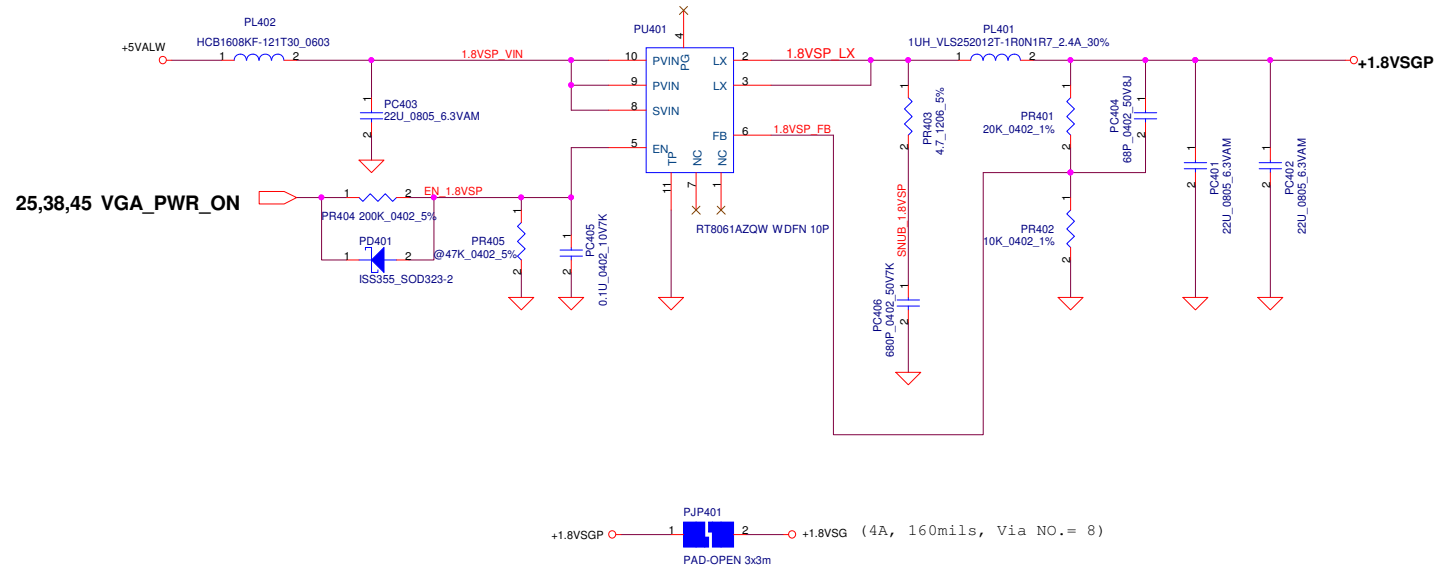
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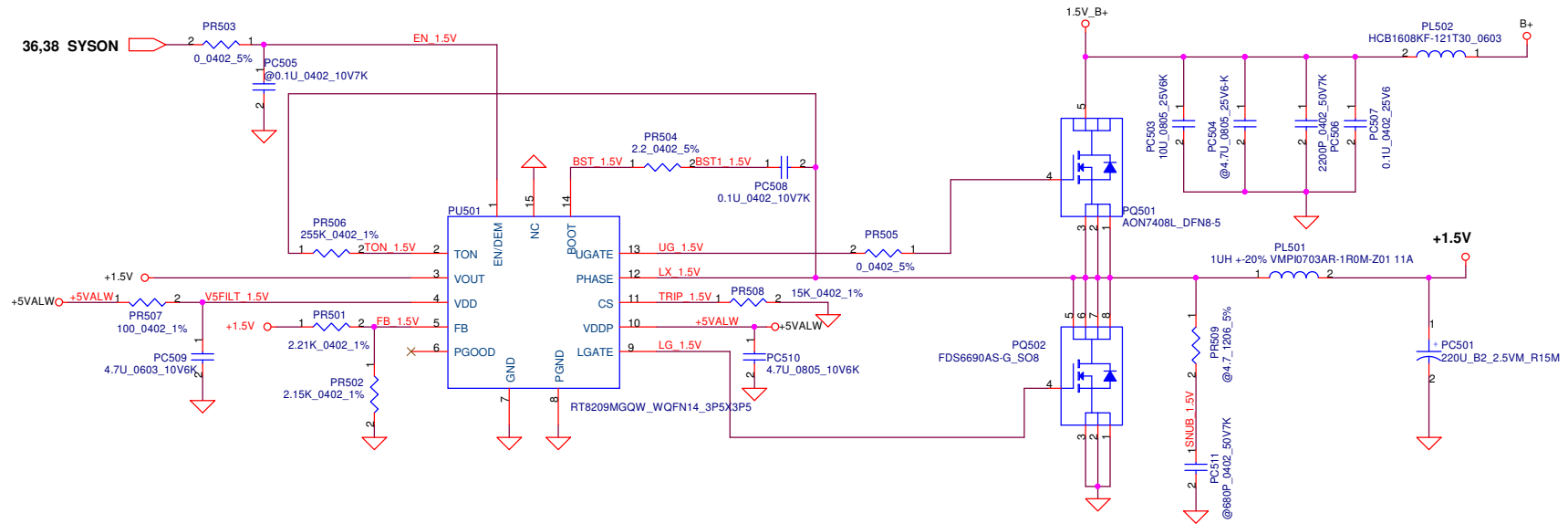
EC:+3VL, reserve PR319, install PR318, PR320 100K  
 EC:+3VALW, reserve PR318, install PR319, PR320 42.2K

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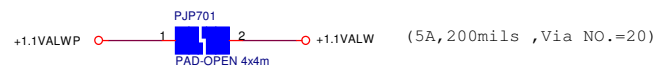
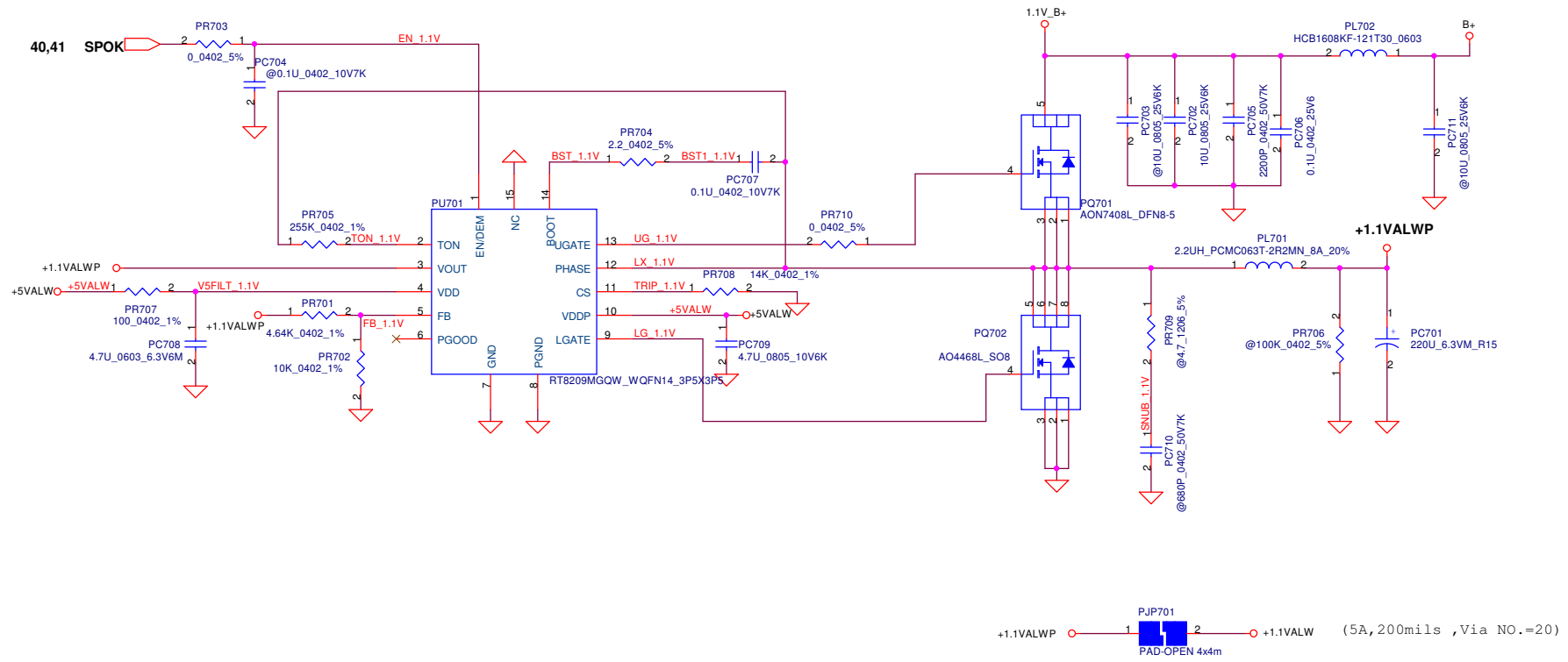
$\langle V_o = 1.8V \rangle \quad V_{FB} = 0.6V$   
 $V_o = V_{FB} * (1 + PR401/PR402) = 0.6 * (1 + 20K/10K) = 1.8V$

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				Document Number	Rev
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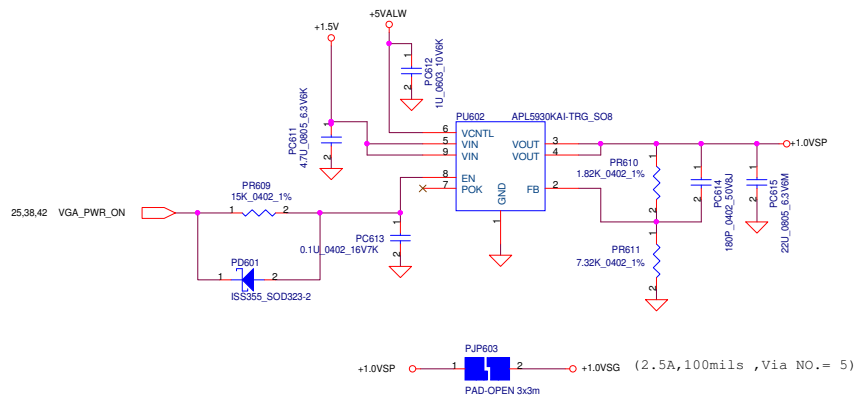
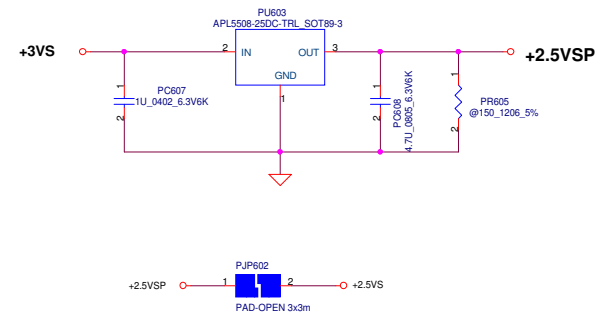
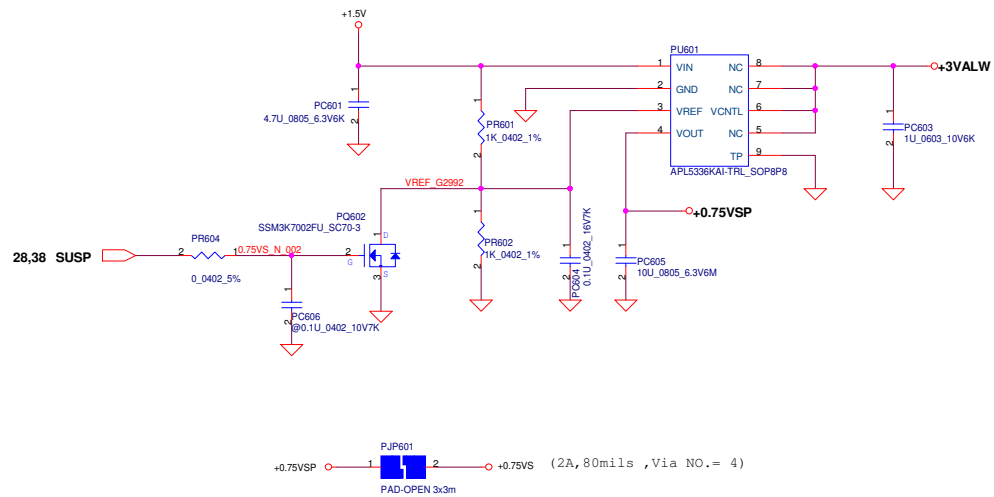


(8A,320mils ,Via NO.= 16)

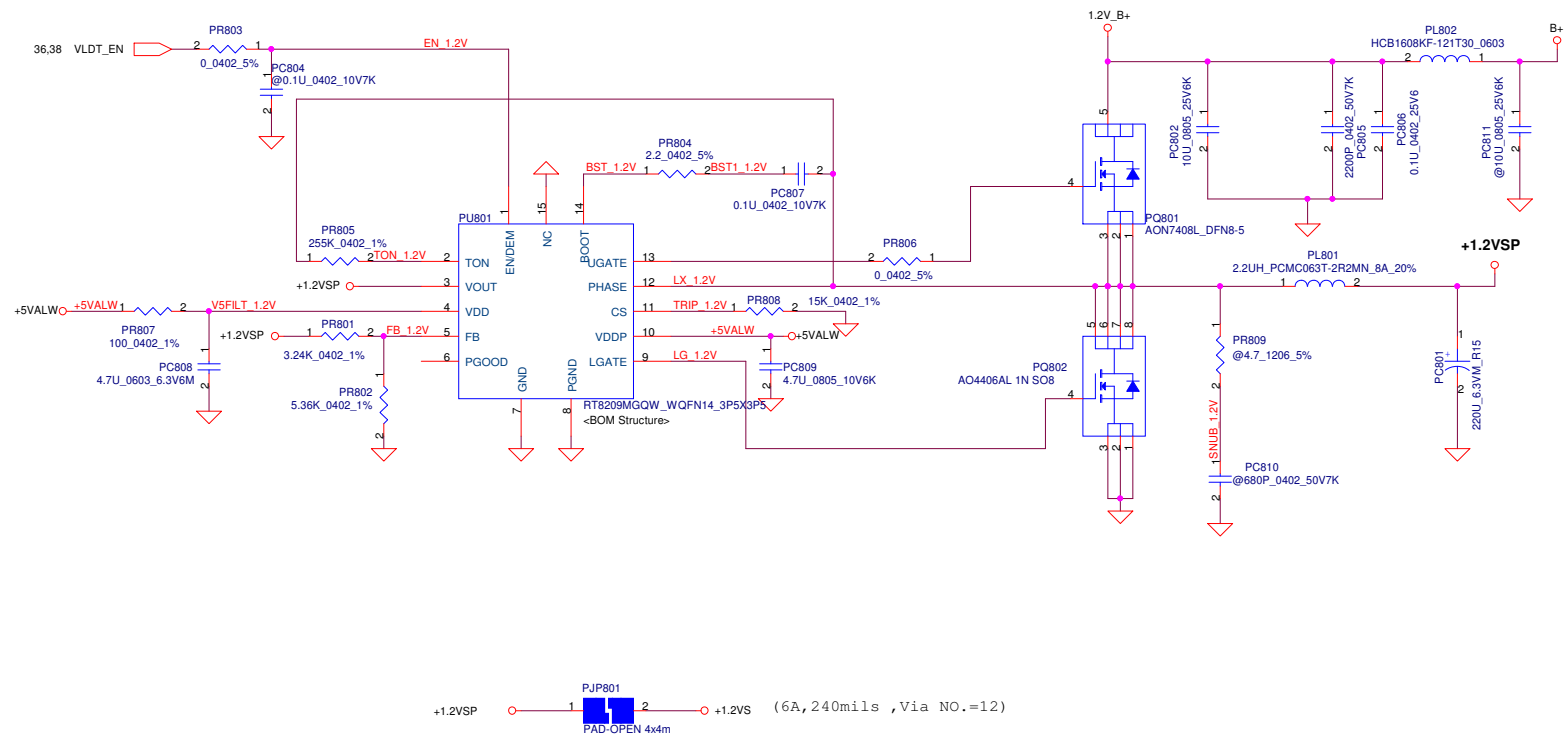
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Issued Date	2011/04/25	Deciphered Date	2012/04/25		
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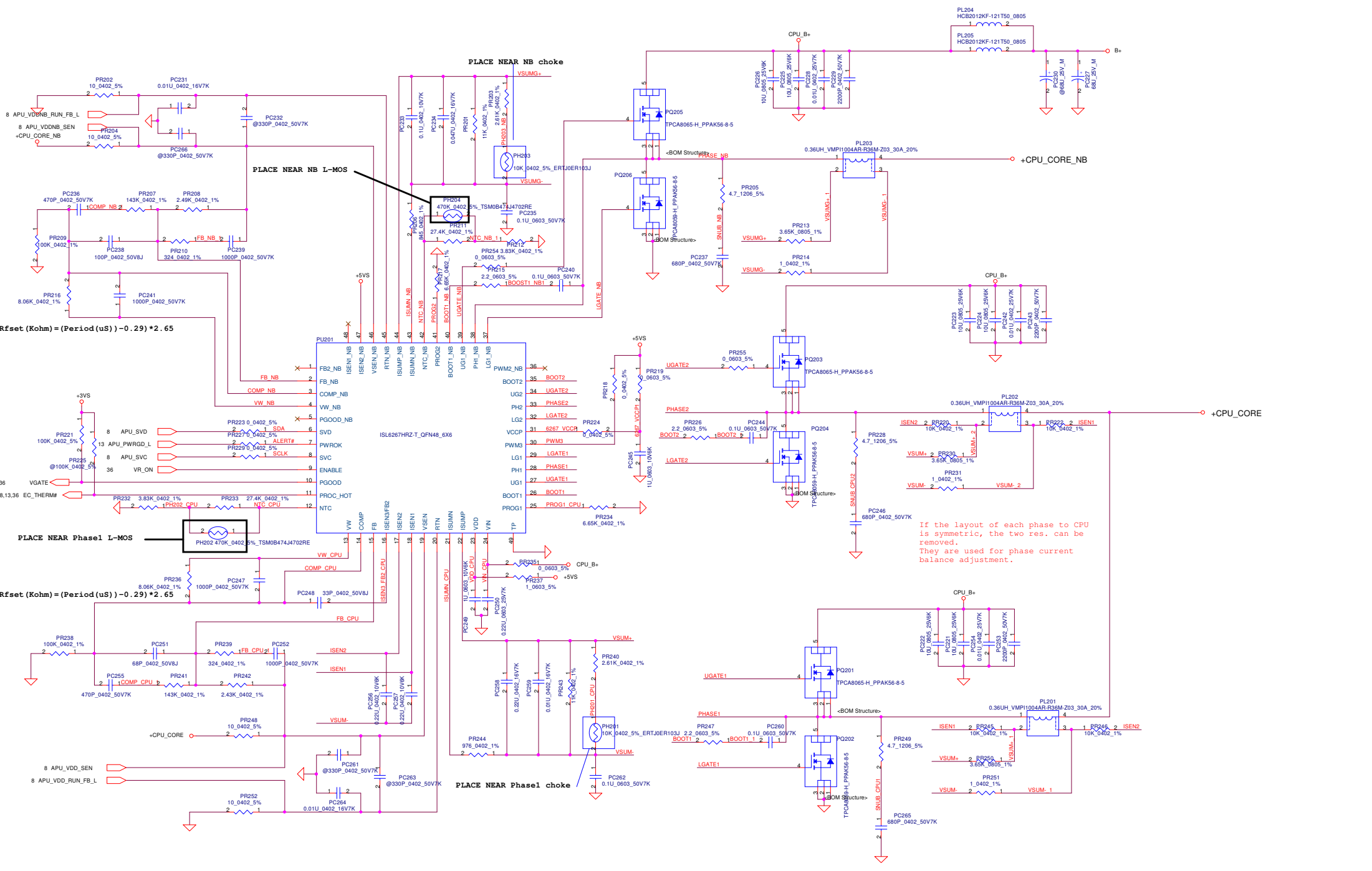
Security Classification		Compal Secret Data		Title	
Issued Date	2011/04/25	Deciphered Date	2012/04/25	PWR+1.1VALWP	
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				<b>NCL61 LA-6321P M/B</b>	
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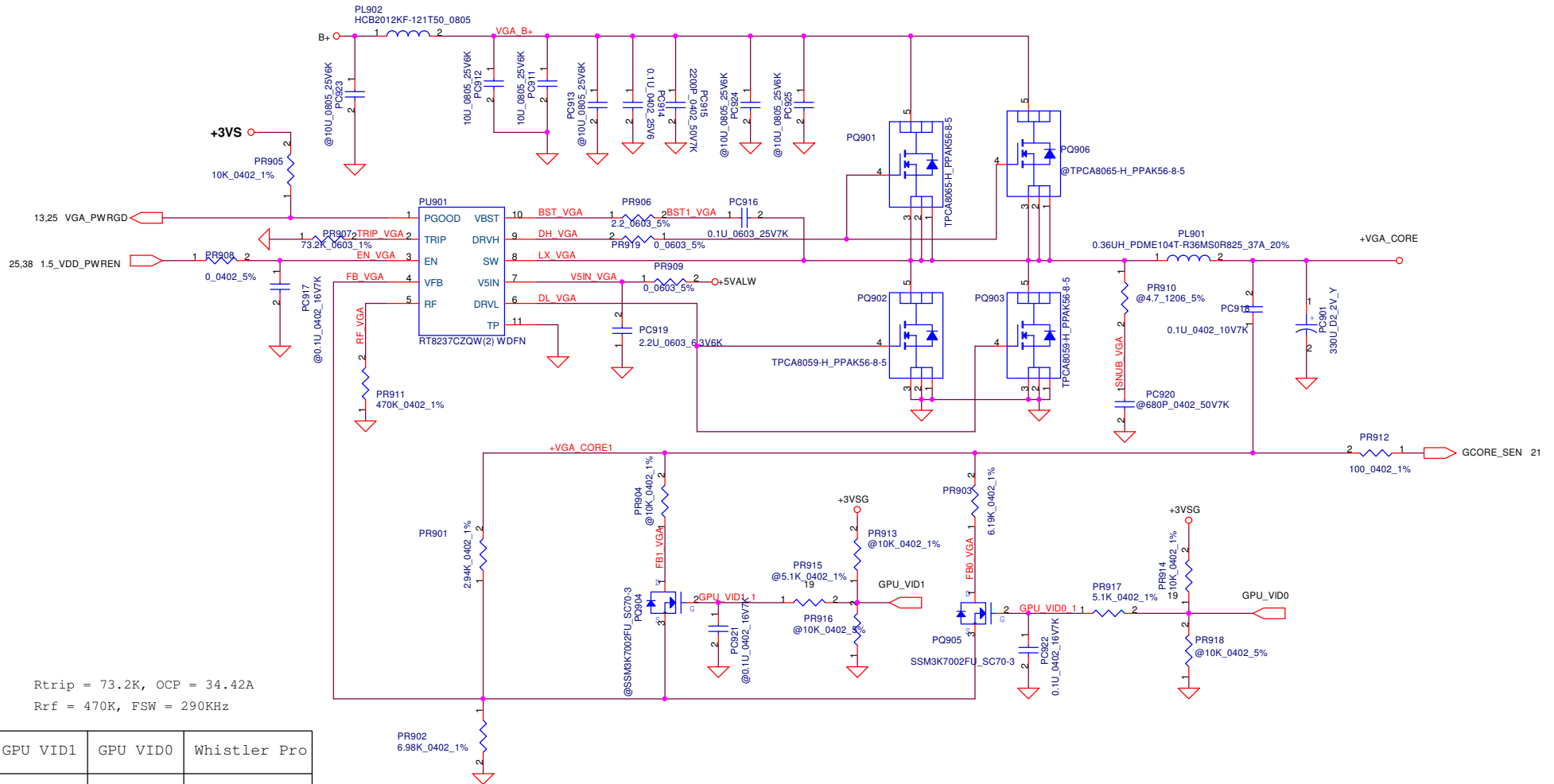


$R_{fset}(\text{Kohm}) = (\text{Period}(\mu\text{s})) - 0.29 * 2.65$

$R_{fset}(\text{Kohm}) = (\text{Period}(\mu\text{s})) - 0.29 * 2.65$

If the layout of each phase to CPU is symmetric, the two res. can be removed. They are used for phase current balance adjustment.

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				<b>PWR +CPU_CORE+CPU_CORE_NB</b>
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				Document Number
				<b>QBL60 LA-7552P</b>
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Date: Monday, April 25, 2011		Sheet 47 of 53		

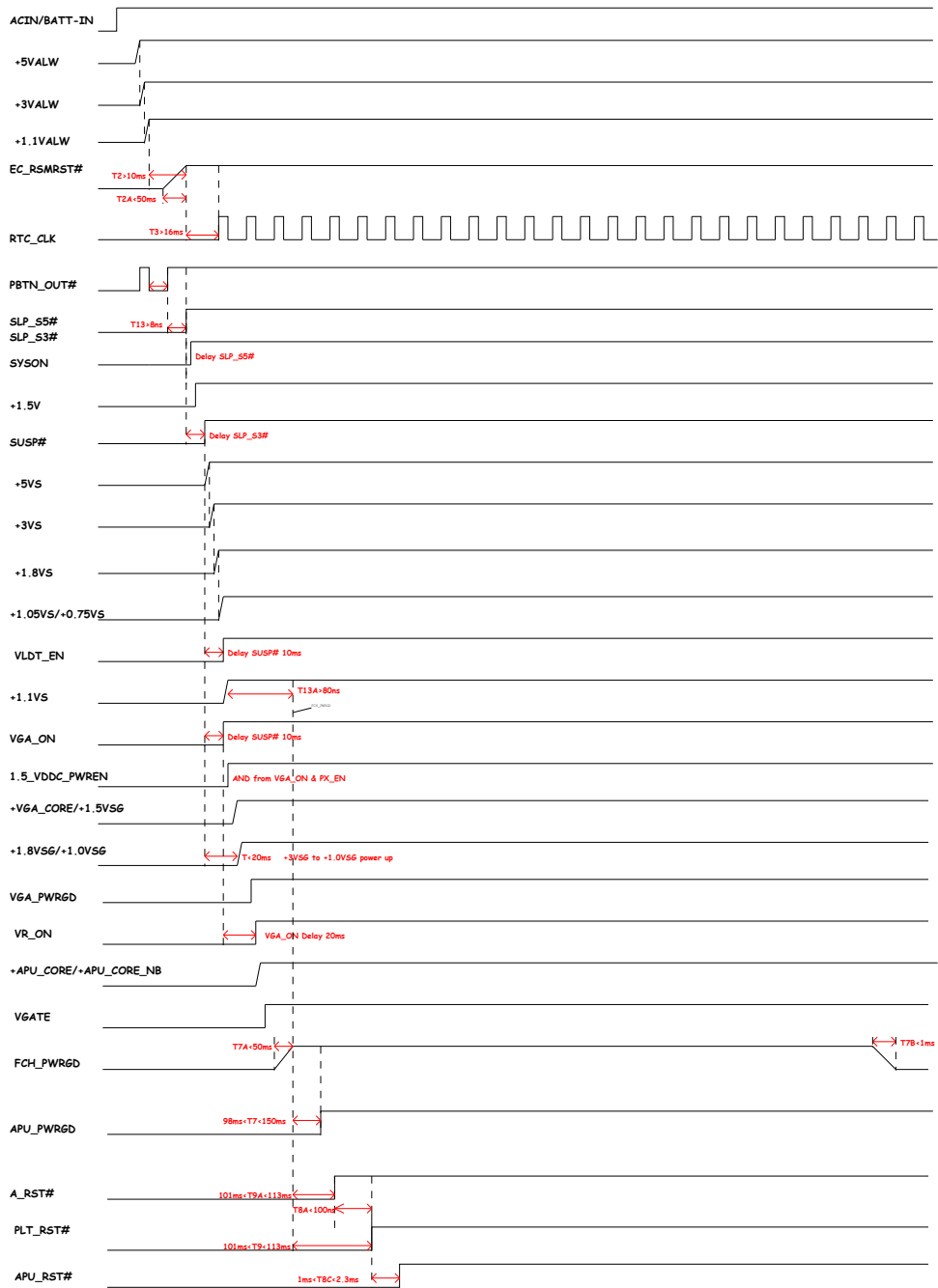


GPU VID1	GPU VID0	Whistler Pro
X	L	1.0V
X	H	0.9V
H	L	
H	H	



Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					

# POWER SEQUENCE



Signal/Parameter	Value	Unit
EC_RSTMRST#	10ms	ms
EC_RSTMRST# (T2A)	50ms	ms
RTC_CLK (T3)	16ms	ms
SYSON	Delay SLP_S5#	ns
SUSP#	Delay SLP_S3#	ns
V6A_ON	Delay SUSP# 10ms	ms
1_5_VDDC_PWREN	AND from V6A_ON & PX_EN	ns
+1.8VS6/+1.0VS6 (T1)	20ms	ms
V6A_PWRGD	V6A_ON Delay 20ms	ms
FCH_PWRGD (T7A)	50ms	ms
APU_PWRGD	98ms-T7=150ms	ms
A_RST#	101ms-T9A=113ms	ms
PLT_RST#	101ms-T9=113ms	ms
APU_RST#	1ms-T8C=2.3ms	ms
FCH_PWRGD (T7B)	1ms	ms

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		For AMD request	0.11	PG#26	Translator change to ANX3110	03/15	ER
2		For AI charge function	0.11	PG#34	Add U2 & U56	03/15	ER
3		For PBL60 MEMO	0.11	PG#32	Change LED1 to Green color.	03/15	ER
4		For switch quality of ME.	0.11	PG#37	Change SW5,SW6 to 100g switch for ME.	03/15	ER
5		For LED brightness.	0.11	PG#32	Change R1584 to 200 ohm. Change R1586,R1588,R1591,R1592,R1593 to 100 ohm	03/15	ER
6		For DFB.	0.12	PG#11	JDIMM1 footprint change to FOX_AS0A626-J8SG-7H_204P-T	03/17	ER
7		For USB3.0 & AI charge.	0.12	PG#34	USBP0 connect to JUSB1 and USBP10 connect to JUSB2.	03/17	ER
8		For Back light function.	0.12	PG#36	U31.15 connect to ENBKL from APU.	03/17	ER
9		For HDMI HPD issue.	0.12	PG#10	Q34 change to 2N7002(ESD) Add R469 to +1.5VS.	03/19	ER
10		For DP0_HPD & DP1_HPD from AMD recommend.	0.12	PG#10	Swap Q13.1 & Q13.3, R618 unmount. Swap Q16.1 & Q16.3, R627 unmount.	03/19	ER
11		For Travis Vendor request	0.12	PG#26	Del DP0_TXN0_C & DP0_TXP0_C	03/22	ER
12		For LED1	0.12	PG#32	LED1 connect to +3VALW	03/22	ER
13		For EC SMBUS	0.2	PG#36	R1021,R1022 change to install.	03/24	ER
14		For Sourcer recommend	0.2		SE100105Z80 change to SE000000K80	03/24	ER
15		For Sourcer recommend	0.2		SE103225Z80 change to SE000008880	03/24	ER
16		For Sourcer recommend	0.2		SB000006A00 change to SB000006A10	03/24	ER
17		For Thermal	0.2	PG#37	Del H4	03/24	ER
18		For +5VS rising time	0.2	PG#38	R1103 change to 47K	03/24	ER
19		For Crystal EA	0.2	PG#29	C1634 change to 12P & C1633 change to 15P	03/24	ER
20		For Crystal EA	0.2	PG#13	C1200 & C1201 change to 12P	03/24	ER
21		For Crystal EA	0.2	PG#19	C353 change to 15P & C354 change to 12P	03/24	ER
22		For EMI request	0.2	PG#36	R1033 change to SM01000DI00 R1055 change to 33 ohm	03/24	ER
23		For EMI request	0.2	PG#28	L38,L39,L40,L41 change to SM070001S00	03/24	ER
24		For EMI request	0.2	PG#27	D1,D2,D3,D6 change to install	03/24	ER
25		For Crystal EA	0.2	PG#13	C1205,C1206 change to 10P	03/24	ER
26		For AI charge	0.2	PG#36 PG#34	U2 reserve CEN# to EC	03/25	ER
27		For AMD spec	0.2	PG#27	R1642 & R1646 change to 4.6K ohm	03/29	ER

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		For EMI request	0.2	PG#30	R1555,R1556,R1557,R1558 change to 0.1uF	03/29	ER
2		For share ROM request	0.2	PG#15 PG#16	U28,R626,R934,R935,R35 change to Un-install R921 change un-install & U910 change to install	03/29	ER
3		For EMI request	0.2	PG#34	D5 change to SC300001Y00	03/29	ER
4		For +3VS leakage from CRT	0.21	PG#27	Add Q101,R1644,R1645 Del R4,R31	03/31	ER
5		For Crystal EA	0.21	PG#13	Y4 change to SJ100007N00 (32.768KHZ 7PF)	03/31	ER
6		For HDMI EA	0.21	PG#34	D32.5 change to connect +5VALW from +5VS	03/31	ER
7		For EMC team requirement (ISN).	0.22	PG#29	Change C1636 from 1000pF to 120pF.	04/19	PR
8		For Thermal team recommend.	0.22	PG#19	Add R78, R79 and reserve R80, R82.	04/19	PR
9		Reserve PX_EN signal.	0.22	PG#36	Reserve PX_EN in EC pin 74.	04/19	PR
10		Follow ME BOM.	0.22	PG#11 PG#12	Swap the location of JDIMM1 & JDIMM2.	04/19	PR
11		Don't use for MP.	0.22	PG#35	Unstuff SW4.	04/19	PR
12		Update Board ID for PR (R1.0).	0.22	PG#37	Change R1026 to 46.4K ohm.	04/19	PR
13		DFM team requirement.	0.22	PG#35	Delete SW3.	04/19	PR
14		DMC team requirement.	0.23	PG#29	Reserve D7 between GND_LAN and GND.	04/21	PR
15		Don't use for MP.	0.23	PG#29	Unstuff C1193.	04/21	PR
16		Key Part list is updated from the customer.	0.23	PG#4	Update U25 (M3-FCH) P/N to SA000043ID0 (S IC 218-0755042 A13 02G050005815 T88!)	04/21	PR
17		Key Part list is updated from the customer.	0.23	PG#13	Update U25 (M2-FCH) P/N to SA000042C80 (S IC 218-0755046 A13 02G050005814 T88!)	04/21	PR
18		Update TS1 as ER build Memo.	0.23	PG#29	Change TS1 from SP050005L00 to SP050006F00. (S X'FORM_IH-160 LAN)	04/21	PR
19		For VGA Sequence.	0.23	PG#38	Change R1127 from 470 ohm to 33 ohm.	04/21	PR
20		Prevent the leakage from CRT monitor.	0.23	PG#27	Add R1644, R1645, Q101 and Del R4, R31.	04/21	PR
21		DFB team requirement.	0.23	PG#34	Del R664-R667 and R672-R675.	04/21	PR
22		ESD team requirement.	0.23	PG#34	Change D5 from SC300001D00 (YSCLAMP0524P SLP25I0P8) to SC300001Y00 (AZ1045-04F DFN2510P10E ESD).	04/21	PR
23		DMC team requirement.	0.23	PG#29	Change the ground of D21, D22, D31, D34 and H8. from GND_LAN to LAN.	04/22	PR
24		DMC team requirement.	0.23	PG#19	Add R83, R84.	04/22	PR
25		DMC team requirement.	1.0	PG#13	Change R657 from 22 ohm to 33 ohm.	04/25	PR
26		DMC team requirement.	1.0	PG#13	Stuff R1561 to 33 ohm and C1509 to 22pF.	04/25	PR
27							

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Reduce the component count for MP.	1.0		Change below the footprints from 0 ohm to R short.	04/25	PR
2					Reference Value Source Part Source Library Page		
3					R537 0_0402_5% R-SHORT X\CIS_SYMB... P06-FS1 PCIE/UMI/TSI		
4					R538 0_0402_5% R-SHORT X\CIS_SYMB... P06-FS1 PCIE/UMI/TSI		
5					R591 0_0402_5% R-SHORT X\CIS_SYMB... P08-FS1 Display/MISC/...		
6					R598 0_0402_5% R-SHORT X\CIS_SYMB... P08-FS1 Display/MISC/...		
7					R606 0_0402_5% R-SHORT X\CIS_SYMB... P08-FS1 Display/MISC/...		
8					R608 0_0402_5% R-SHORT X\CIS_SYMB... P08-FS1 Display/MISC/...		
9					R611 0_0402_5% R-SHORT X\CIS_SYMB... P08-FS1 Display/MISC/...		
10					R81 0_0402_5% R-SHORT X\CIS_SYMB... P14-HUDSON-M2 GPL...		
11					R912 0_0402_5% R-SHORT X\CIS_SYMB... P16-HUDSON-M2 STR...		
12					R1145 0_0603_5% R-SHORT X\CIS_SYMB... P17-HUDSON-M2 Pow...		
13					R1148 0_0603_5% R-SHORT X\CIS_SYMB... P17-HUDSON-M2 Pow...		
14					R19 0_0603_5% R-SHORT X\CIS_SYMB... P17-HUDSON-M2 Pow...		
15					R20 0_0603_5% R-SHORT X\CIS_SYMB... P17-HUDSON-M2 Pow...		
16					R22 0_0402_5% R-SHORT X\CIS_SYMB... P17-HUDSON-M2 Pow...		
17					R23 0_0402_5% R-SHORT X\CIS_SYMB... P17-HUDSON-M2 Pow...		
18					R24 0_0402_5% R-SHORT X\CIS_SYMB... P17-HUDSON-M2 Pow...		
19					R25 0_0603_5% R-SHORT X\CIS_SYMB... P17-HUDSON-M2 Pow...		
20					R26 0_0402_5% R-SHORT X\CIS_SYMB... P17-HUDSON-M2 Pow...		
21					R27 0_0402_5% R-SHORT X\CIS_SYMB... P17-HUDSON-M2 Pow...		
22					R28 0_0402_5% R-SHORT X\CIS_SYMB... P17-HUDSON-M2 Pow...		
23					R937 0_0805_5% R-SHORT X\CIS_SYMB... P17-HUDSON-M2 Pow...		
24					R938 0_0805_5% R-SHORT X\CIS_SYMB... P17-HUDSON-M2 Pow...		
25					R941 0_0805_5% R-SHORT X\CIS_SYMB... P17-HUDSON-M2 Pow...		
26					R945 0_0402_5% R-SHORT X\CIS_SYMB... P17-HUDSON-M2 Pow...		
27					R483 0_0402_5% R-SHORT X\CIS_SYMB... P23-VRAM_DDR3 / CH...		
					R485 0_0402_5% R-SHORT X\CIS_SYMB... P23-VRAM_DDR3 / CH...		
					R511 0_0402_5% R-SHORT X\CIS_SYMB... P24-VRAM_DDR3 / CH...		
					R513 0_0402_5% R-SHORT X\CIS_SYMB... P24-VRAM_DDR3 / CH...		
					R1291 0_0402_5% R-SHORT X\CIS_SYMB... P26-LVDS Translator-A...		
					R570 0_0805_5% R-SHORT X\CIS_SYMB... P26-LVDS Translator-A...		
					R607 0_0805_5% R-SHORT X\CIS_SYMB... P26-LVDS Translator-A...		
					R1634 0_0402_5% R-SHORT X\CIS_SYMB... P27-LVDS CONN / CRT...		
					R1635 0_0402_5% R-SHORT X\CIS_SYMB... P27-LVDS CONN / CRT...		
					R1636 0_0402_5% R-SHORT X\CIS_SYMB... P27-LVDS CONN / CRT...		
					R1641 0_0402_5% R-SHORT X\CIS_SYMB... P27-LVDS CONN / CRT...		
					R1643 0_0603_5% R-SHORT X\CIS_SYMB... P27-LVDS CONN / CRT...		
					R1650 0_0603_5% R-SHORT X\CIS_SYMB... P27-LVDS CONN / CRT...		
					R1651 0_0402_5% R-SHORT X\CIS_SYMB... P27-LVDS CONN / CRT...		
					R560 0_0603_5% R-SHORT X\CIS_SYMB... P29-LAN Realtek RTL81...		
					R647 0_0402_5% R-SHORT X\CIS_SYMB... P29-LAN Realtek RTL81...		
					R658 0_0603_5% R-SHORT X\CIS_SYMB... P29-LAN Realtek RTL81...		
					R1531 0_0805_5% R-SHORT X\CIS_SYMB... P30-HD AUDIO CODEC...		
					R1534 0_0603_5% R-SHORT X\CIS_SYMB... P30-HD AUDIO CODEC...		
					R1537 0_0603_5% R-SHORT X\CIS_SYMB... P30-HD AUDIO CODEC...		
					R1560 0_0603_5% R-SHORT X\CIS_SYMB... P31-RTS5137 Media C...		
					R1573 0_0402_5% R-SHORT X\CIS_SYMB... P32-Mini-Card / LED		
					R1574 0_0402_5% R-SHORT X\CIS_SYMB... P32-Mini-Card / LED		
					R1575 0_0402_5% R-SHORT X\CIS_SYMB... P32-Mini-Card / LED		
					R1576 0_0402_5% R-SHORT X\CIS_SYMB... P32-Mini-Card / LED		
					R1577 0_0402_5% R-SHORT X\CIS_SYMB... P32-Mini-Card / LED		
					R1578 0_0402_5% R-SHORT X\CIS_SYMB... P32-Mini-Card / LED		
					R1579 0_0402_5% R-SHORT X\CIS_SYMB... P32-Mini-Card / LED		
					R1580 0_0402_5% R-SHORT X\CIS_SYMB... P32-Mini-Card / LED		
					R1595 0_0805_5% R-SHORT X\CIS_SYMB... P33-HDD & ODD CONN		
					R1598 0_0805_5% R-SHORT X\CIS_SYMB... P33-HDD & ODD CONN		
					R1049 0_0603_5% R-SHORT X\CIS_SYMB... P35-FAN / PBTN / EC R...		

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