

2N6387, 2N6388

Plastic Medium-Power Silicon Transistors

These devices are designed for general-purpose amplifier and low-speed switching applications.

Features

- High DC Current Gain – $h_{FE} = 2500$ (Typ) @ $I_C = 4.0$ A dc
- Collector–Emitter Sustaining Voltage – @ 100 mA dc
 $V_{CE(sus)} = 60$ V dc (Min) – 2N6387
 $= 80$ V dc (Min) – 2N6388
- Low Collector–Emitter Saturation Voltage –
 $V_{CE(sat)} = 2.0$ V dc (Max) @ $I_C = 5.0$ A dc – 2N6387, 2N6388
- Monolithic Construction with Built-In Base–Emitter Shunt Resistors
- TO–220AB Compact Package
- These Devices are Pb–Free and are RoHS Compliant*

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CE}	60 80	V dc
Collector–Base Voltage	V_{CB}	60 80	V dc
Emitter–Base Voltage	V_{EB}	5.0	V dc
Collector Current – Continuous – Peak	I_C	10 15	A dc
Base Current	I_B	250	mA dc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	65 0.52	W W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	2.0 0.016	W W/ $^\circ\text{C}$
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	–65 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Indicates JEDEC Registered Data.

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	1.92	$^\circ\text{C/W}$
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$

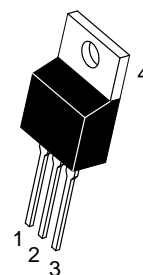
*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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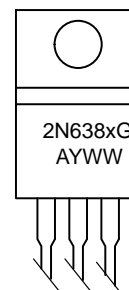
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DARLINGTON NPN SILICON POWER TRANSISTORS 8 AND 10 AMPERES 65 WATTS, 60 – 80 VOLTS



TO–220
CASE 221A
STYLE 1

MARKING DIAGRAM



2N638x = Device Code
x = 7 or 8

G = Pb–Free Package
A = Assembly Location
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
2N6387G	TO–220 (Pb–Free)	50 Units / Rail
2N6388G	TO–220 (Pb–Free)	50 Units / Rail

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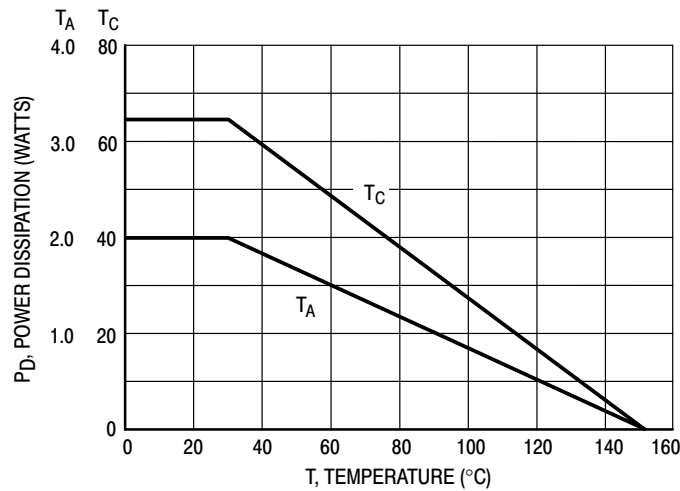


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted) (Note 2)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (Note 3) (I _C = 200 mAdc, I _B = 0)	V _{CEO(sus)}	60 80	– –	Vdc
Collector Cutoff Current (V _{CE} = 60 Vdc, I _B = 0) (V _{CE} = 80 Vdc, I _B = 0)	I _{CEO}	– –	1.0 1.0	mAdc
Collector Cutoff Current (V _{CE} = 60 Vdc, V _{EB(off)} = 1.5 Vdc) (V _{CE} = 80 Vdc, V _{EB(off)} = 1.5 Vdc) (V _{CE} = 60 Vdc, V _{EB(off)} = 1.5 Vdc, T _C = 125°C) (V _{CE} = 80 Vdc, V _{EB(off)} = 1.5 Vdc, T _C = 125°C)	I _{CEX}	– – – –	300 300 3.0 3.0	μAdc mAdc
Emitter Cutoff Current (V _{BE} = 5.0 Vdc, I _C = 0)	I _{EBO}	–	5.0	mAdc
ON CHARACTERISTICS (Note 3)				
DC Current Gain (I _C = 5.0 Adc, V _{CE} = 3.0 Vdc) (I _C = 10 Adc, V _{CE} = 3.0 Vdc)	h _{FE}	1000 100	20,000 –	–
Collector-Emitter Saturation Voltage (I _C = 5.0 Adc, I _B = 0.01 Adc) (I _C = 10 Adc, I _B = 0.1 Adc)	V _{CE(sat)}	– –	2.0 3.0	Vdc
Base-Emitter On Voltage (I _C = 5.0 Adc, V _{CE} = 3.0 Vdc) (I _C = 10 Adc, V _{CE} = 3.0 Vdc)	V _{BE(on)}	– –	2.8 4.5	Vdc
DYNAMIC CHARACTERISTICS				
Small-Signal Current Gain (I _C = 1.0 Adc, V _{CE} = 5.0 Vdc, f _{test} = 1.0 MHz)	h _{fe}	20	–	–
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f = 1.0 MHz)	C _{ob}	–	200	pF
Small-Signal Current Gain (I _C = 1.0 Adc, V _{CE} = 5.0 Vdc, f = 1.0 kHz)	h _{fe}	1000	–	–

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Indicates JEDEC Registered Data.

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

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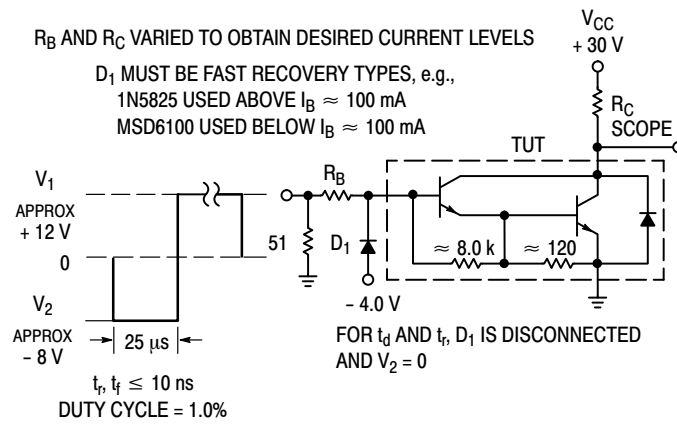


Figure 2. Switching Times Test Circuit

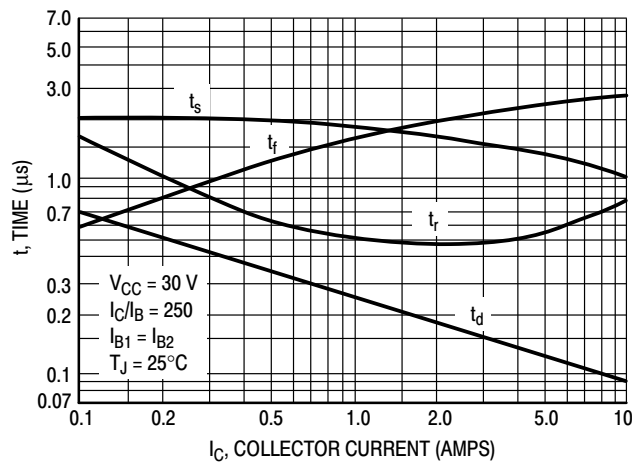


Figure 3. Switching Times

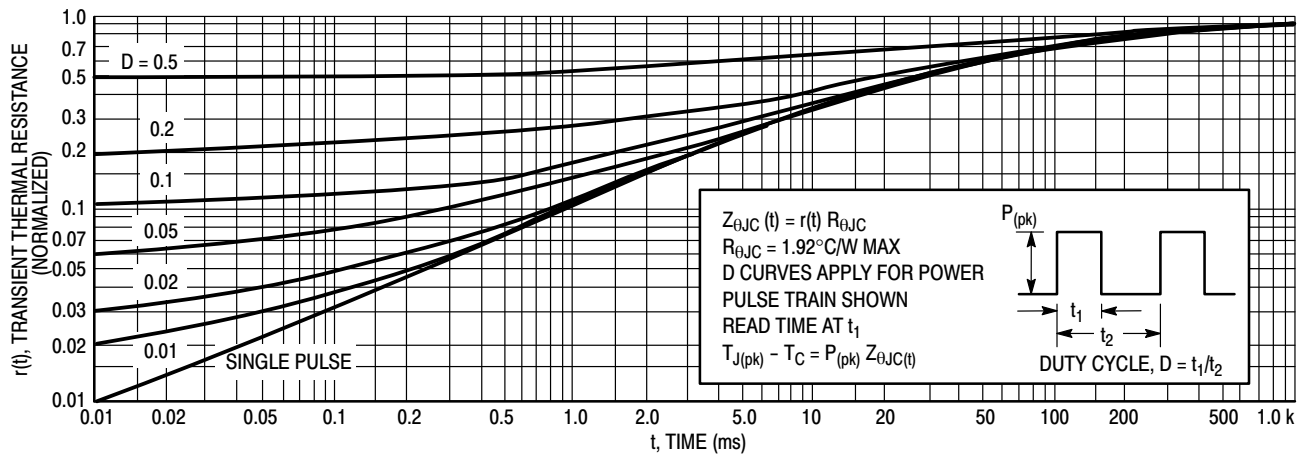


Figure 4. Thermal Response

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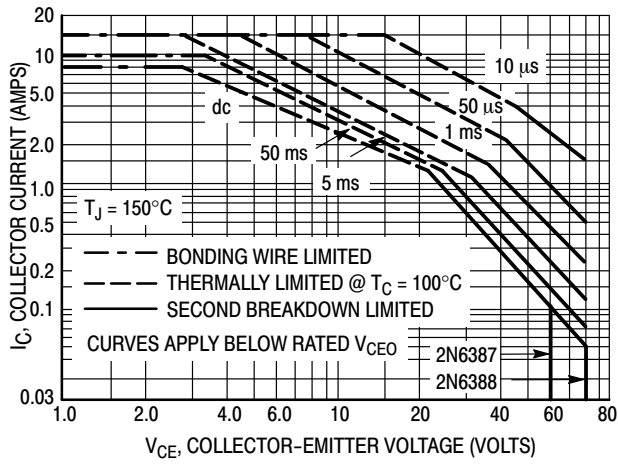


Figure 5. Active-Region Safe Operating Area

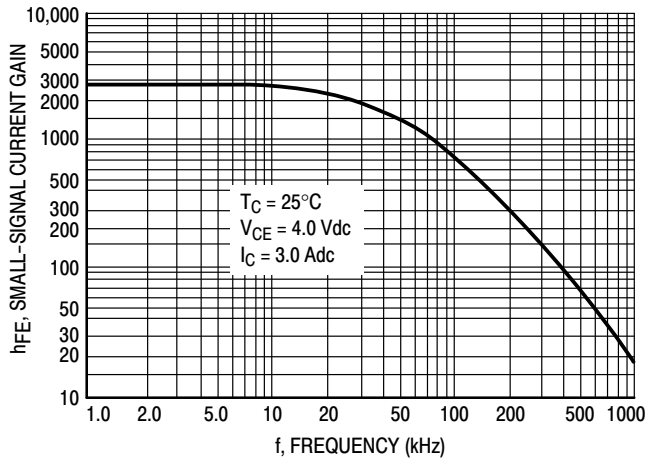


Figure 6. Small-Signal Current Gain

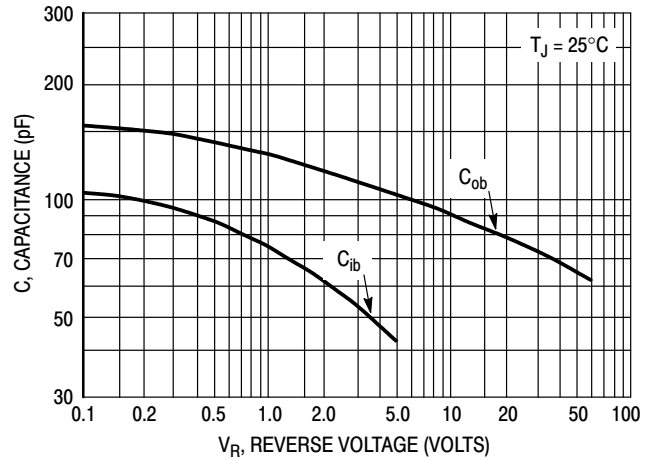


Figure 7. Capacitance

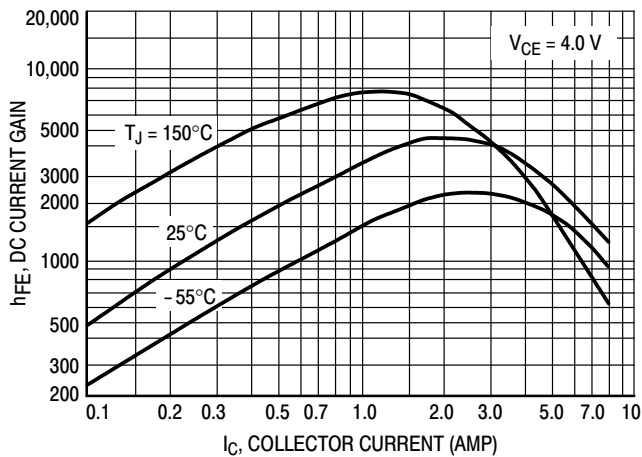


Figure 8. DC Current Gain

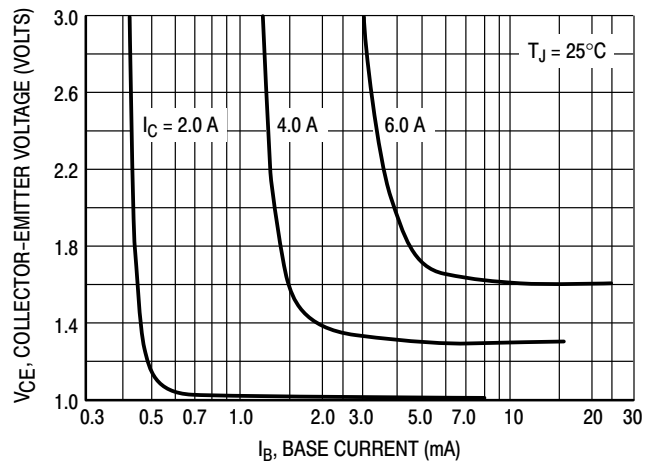


Figure 9. Collector Saturation Region

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

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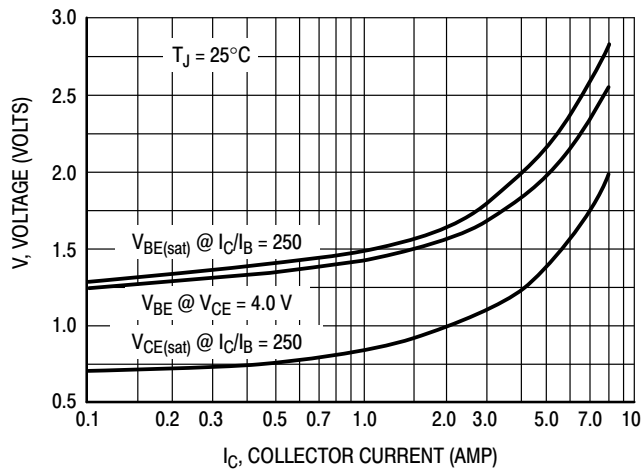


Figure 10. "On" Voltages

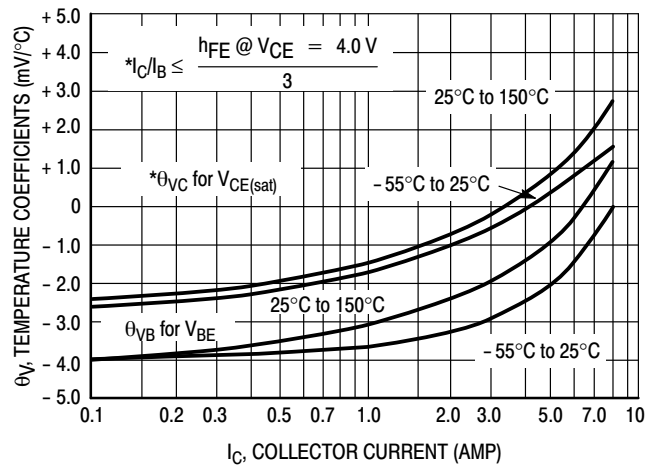


Figure 11. Temperature Coefficients

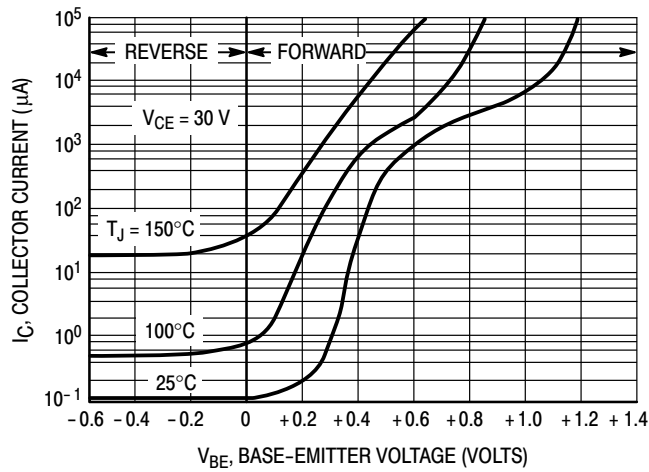


Figure 12. Collector Cut-Off Region

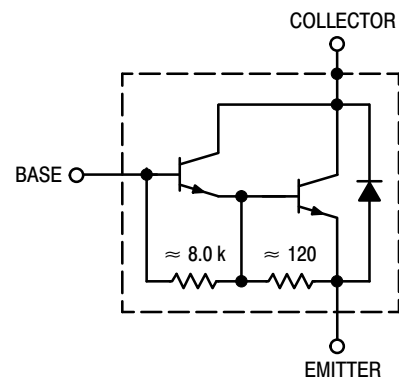


Figure 13. Darlington Schematic

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