Application note

IGBT and MOSFET Drivers Correctly Calculated

Introduction

This application note describes the calculation of the gate drive performance figures required for a given application. The values as derived from this application note serve as a base for selecting the most appropriate driver.

All CONCEPT ratings given in the datasheets refer directly to the usable performance figures in the application. No further derating or correction has to be made for the internal power consumption of the driver or other intrinsic parameters.

For a fast overview, equations 1, 4 and 5 are most relevant.

Required Drive Power

The gate driver serves to turn the power device on and off, respectively. In order to do so, the gate driver charges the gate of the power device up to its final turn-on voltage V_{GE_on}, or the drive circuit discharges the gate down to its final turn-off voltage V_{GE_off}.

The transition between the two gate voltage levels requires a certain amount of power to be dissipated in the loop between gate driver, gate resistors and power device. This figure is called the drive power P_{DRV}. The gate driver has to be chosen according to the drive power required for a given power module.

The drive power is calculated from the gate charge Q_{Gate}, the switching frequency f_{IN}, and the actual driver output voltage swing ΔV_{Gate}:

$$P_{DRV} = Q_{Gate} \cdot f_{IN} \cdot \Delta V_{Gate} \qquad \text{(Eq. 1)}$$

If there is an external capacitor C_{GE} present (auxiliary gate capacitor), then the gate driver also needs to charge and discharge this capacitor as shown in Figure 1.

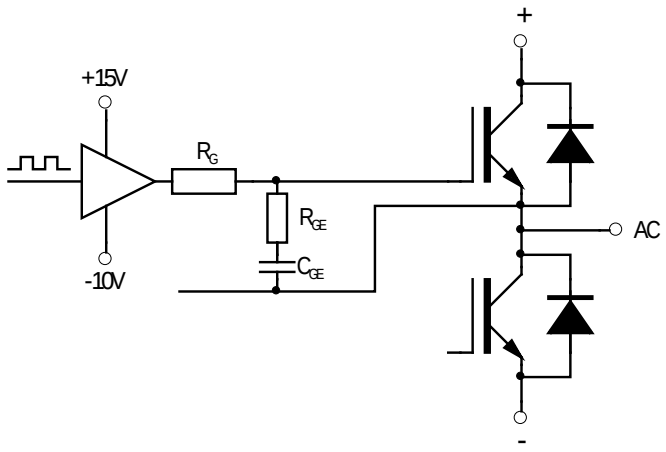

Fig. 1: Gate drive with additional RC element

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The value of R_{GE} is not influencing the required drive power as long as C_{GE} is fully charged and discharged during one cycle. The required drive power becomes:

$$P_{DRV} = Q_{Gate} \cdot f_{IN} \cdot \Delta V_{Gate} + C_{GE} \cdot f_{IN} \cdot \Delta V_{Gate}^{2} \quad \text{(Eq. 2)}$$

The above equations are true in non-resonant gate drives. Drive power does not depend on the value of the gate resistors or the duty cycle as long as the switching transition goes from fully on to fully off and back. The parameter gate charge Q_{Gate} is next to be determined.

Gate Charge

Q_{Gate} must never be calculated from the IGBT or MOSFET input capacitance C_{ies}. C_{ies} is merely a first order approximation of the gate charge curve in the origin (V_{GE} = 0V). The gate charge curve of a power semiconductor is highly non-linear. That is why the gate charge must be derived from integrating the gate charge curve between V_{GE_off} and V_{GE_on}.

If Q_{Gate} is given in the datasheet, it is important to check if the gate charge is given for is the same gate voltage swing as used in the application. Gate charges from different gate voltage swings are not generally comparable. As an example, there is no exact way to determine the gate charge for V_{GE} = -10V to +15V if Q_{Gate} is given for V_{GE} = 0V to +15V.

In such cases, when there is no gate charge diagram (Q_{Gate} vs. V_{GE}), the only way to obtain Q_{Gate} is to measure it. Figure 2 shows a typical turn-on transition of a gate driver. The gate drive output current I_{OUT} is charging the power device's gate. Consequently, the area under the output current curve is the total gate charge as shown in Figure 2 (see Figure 4 for schematic). The integration time should be high enough to cover the full gate voltage swing (see output, GH; output GL). The integration time should not be extended beyond the settling of the driver output voltages to their final values, or the settlement of the driver output current to zero.

$$Q_{Gate} = \int I_{OUT} dt \quad \text{(Eq. 3)}$$

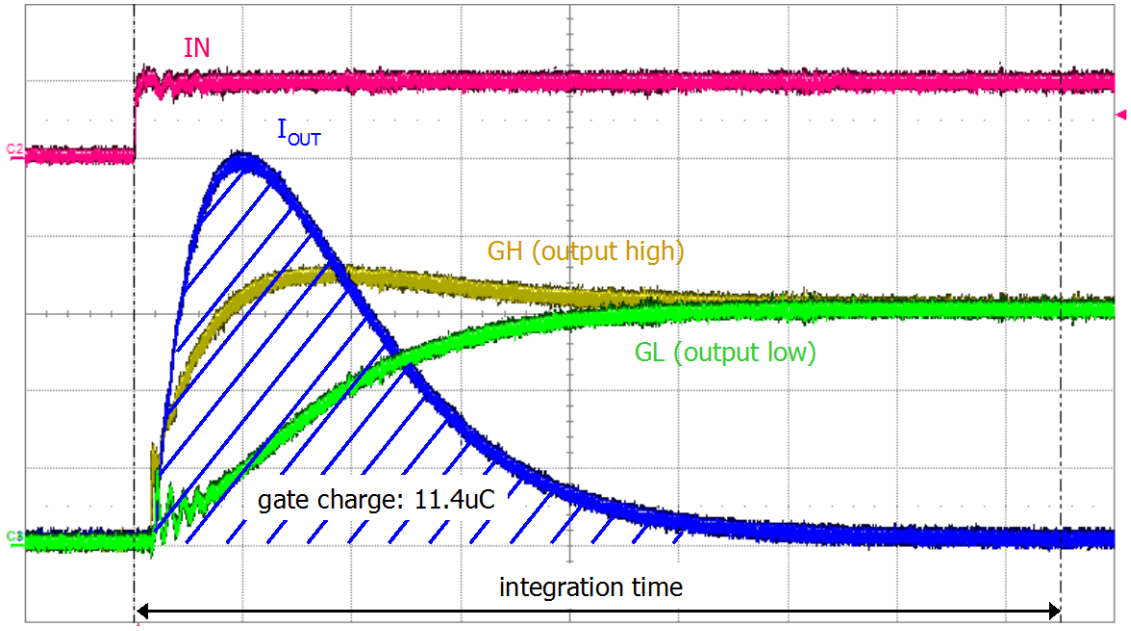

Fig. 2: Gate charge measurement by integrating the output current over time

Care must be taken if the output current is exhibiting oscillations. In a practical setup, the measured gate charge is often influenced by current oscillations due to longer integration time and due to inaccuracies by a large number of smaller numbers being added instead of fewer large numbers. Therefore, it is strongly recommended to take a non-oscillating setup for the measurement of the gate charge.

Driver output current oscillations may lead to additional power dissipation in the gate driver unit, due to clamping effects and non-linear behaviour of the output stages and controlling circuitry. Therefore, the maximum usable gate drive power is always derived from setups with non-oscillating driver output current.

Resonant gate driving may exploit the oscillation phenomena with benefit at high switching frequency. Resonant gate drives are not within the scope of this application note.

Maximum Drive Current: Recommendation

Another important performance parameter of gate drive circuits is the maximum gate drive current $I_{OUT,max}$. $I_{OUT,max}$ must be high enough to drive the lowest chosen gate resistor value with the highest chosen gate voltage swing. The simplistic first order maximum is:

$$\hat{I}_{OUT(1.Order)} = \frac{\Delta V_{Gate}}{R_{Gate\_Min}} \qquad \text{(Eq. 4)}$$

It is recommended to chose the maximum gate drive current according to $I_{OUT,max} > \hat{I}_{OUT(1.\ Order)}$ if there are oscillations present in the gate current. Caution has to be used if the gate current oscillation is showing low damping. The peak current in this case can be very high and is only accessible by measurement.

Practical experience shows that typically less than 70% of the above value $\hat{I}_{OUT(1.\ Order)}$ is seen in the working circuit for small gate resistor values, if there are no oscillations in the gate current. The reason for that reduction is the parasitic inductance in the gate loop. This parasitic inductance is limiting the current slope at the beginning of the gate charge process. Therefore, it is recommended to chose the gate driver according to the following requirement, with a reduction factor of up to 0.7 for small gate resistor values, if there are no oscillations present in the gate loop:

$$I_{OUT,\max} \geq 0.7 \cdot \hat{I}_{OUT(1.Order)} \qquad \text{(Eq. 5)}$$

The actual peak current at the driver output always has to be reconfirmed by measurement when using Equation5.

Example:

If you would like to drive an IGBT module with 0.5Ω external turn-on gate resistance and 0.2Ω module internal resistance at a gate voltage swing of 25V (+15 / -10V), the gate driver must be capable of at least 25A output current at turn on.

A theoretical basis for the practically experienced reduction factor of 0.7 is given in section “Maximum Drive Current: Background”.

Variable Output Voltage Swing

The gate driver’s output voltage swing does change slightly over output power. This is due to the softness characteristic of the high voltage isolated DC/DC converter in the driver. The worst case calculation is derived from the maximum gate voltage swing. Please check with the driver datasheet to obtain the gate voltage swing at the intended output power range, or measure the output voltage in the real setup.

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Strictly speaking the gate charge should be measured exactly at the target gate voltage swing. If the gate charge is taken from a higher gate voltage swing (at low frequency), the calculated drive power requirement is higher than the real drive power requirement (at target frequency). Practically there is no need to consider this effect if the intended accuracy is not better than 5%.

Maximum Operation Temperature

CONCEPT drivers are rated for full output power at –40°C to 85°C unless stated otherwise in the datasheet. If there is no derating explicitly given, the maximum drive power and current can be used over the whole temperature range.

The temperature rating refers to ambient temperature under unforced, natural convection with no additional airflow. Even mild levels of forced air cooling (air circulation by a fan) can significantly increase heat transfer from the driver – leading to even higher reliability figures.

Maximum Switching Frequency

Several parameters influence the maximum obtainable switching frequency. First, there is the resulting output power as considered in the preceding sections. Second is the variable power dissipation in the gate resistors. The higher the gate resistor is, the lower the power dissipated in the driver output stage at a given frequency. The third limiting effect is the self-heating of the driver due to high switching frequency.

In Figure 3, a sample diagram of output power vs. switching frequency is shown for several gate resistor values. The shape and parameters of the curves are specific to a certain gate driver; the curves shown in Figure 3 are not universally valid.

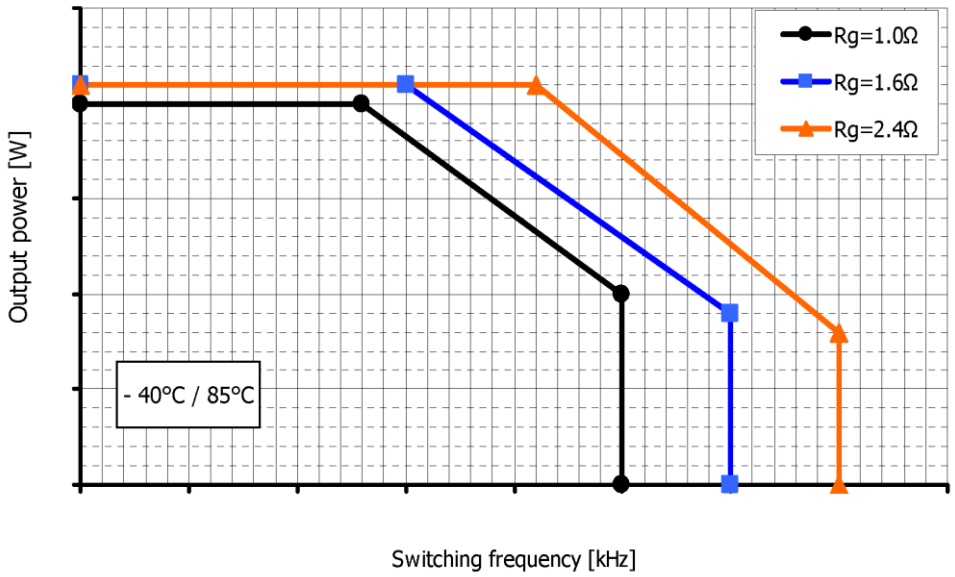

Fig. 3: Permissible output power vs. switching frequency

Maximum Drive Current: Background

The theoretical background for the established real-life reduction factor is derived from the following question:

What peak current can flow in a realistic gate loop as long as there are no oscillations?

The analysis is solely focused on the variation of the gate resistor while leaving all other parameters constant. Only non-resonant gate drives are considered. It is assumed that a non-oscillating gate current waveform is preferable.

Figure 4 shows the model gate circuit, consisting of a driver stage with outputs GH, GL; the individual gate resistor paths $R_{g,on/off}$ and associated stray inductances $L_{g,on/off}$; and the common gate current path to the power device with the associated stray inductance L_{gg}. The power device is modelled by a constant capacitance. This is of course a simplification, but it is justified only at the beginning of the gate charge process. The beginning of the gate charge process is the most relevant stage, because the charging current takes its maximum here.

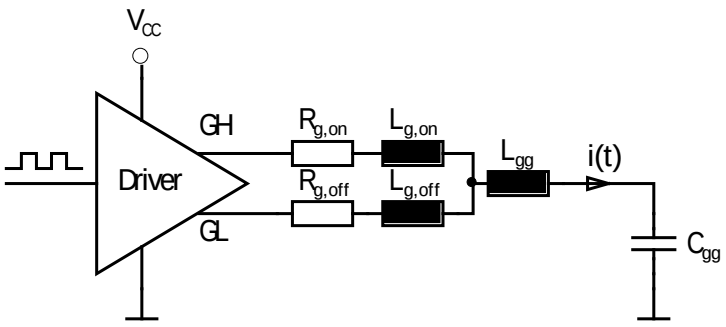

Fig. 4: Model circuit for deriving the maximum gate drive current

The gate current i(t) is governed by the well known second order differential equation for RLC circuits:

$$L_g \cdot \frac{d^2 i(t)}{dt^2} + R_g \cdot \frac{di(t)}{dt} + \frac{i(t)}{C_{gg}} = 0 \qquad \text{(Eq. 6)}$$

L_g and R_g are the respective sum of L and R in the turn-on and turn-off path, respectively. The boundary between oscillating and non-oscillating solutions is set by the ratio of L_g, C_{gg}, and R_g. Non-oscillating solutions for i(t) must fulfil the damping condition:

$$R_{g(non-osc)} \geq 2\sqrt{\frac{L_g}{C_{gg}}} \qquad \text{(Eq. 7)}$$

The minimum gate resistor to retain a non-oscillating gate current waveform is given by Equation 8:

$$R_{g,\min(non-osc)} = 2\sqrt{\frac{L_g}{C_{gg}}} \qquad \text{(Eq. 8)}$$

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The highest possible current peak $\hat{I}_{max(non\text{-}osc)}$ in a non-oscillating waveform can thus be expressed as the peak current in the critically damped case. The peak gate current $\hat{I}_{max(non\text{-}osc)}$ is then becoming:

$$\hat{I}_{\max(non-osc)} = \frac{2}{e} \cdot \frac{\Delta V_{Gate}}{R_{g,\min(non-osc)}} \approx 0.74 \cdot \frac{\Delta V_{Gate}}{R_{g,\min(non-osc)}} \quad \text{(Eq. 9)}$$

Where e is the Euler number.

It is important to note that Equation 9 is only true for the maximum current in the non-oscillating case. For gate resistor values $R_g > R_{g,min(non\text{-}osc)}$ the peak current will always be smaller than $\hat{I}_{max(non\text{-}osc)}$. For high values of R_g the gate current is following Equation 4, but still the peak gate current will always be smaller than $\hat{I}_{max(non\text{-}osc)}$. It is thus sufficient to have a driver strength (meaning the maximum driver output current) according to Equation 9. The value of $R_{g,min(non\text{-}osc)}$ has to be determined by measurement for every new gate loop setup and power device.

The theoretically derived reduction factor of 0.74 for $\hat{I}_{max(non\text{-}osc)}$ is further reduced in real applications by the limited driver switching speed, the transmission line nature of real gate loops, and the internal time constants of the driver's blocking capacitors. The practically recommended reduction factor of 0.70 is thus in good agreement with the theoretically derived maximum of 0.74.

Example:

If the gate driver with output gate voltage swing ΔV_{Gate}=25V is connected to the IGBT with a loop inductance of 20nH, and if the IGBT's input capacitance is 30nF, then:

$$R_{g,\min(non-osc)} = 2\sqrt{\frac{20nH}{30nF}} = 1.63\Omega$$

For gate resistor values R_g below 1.63Ω the gate current will start oscillating in this example. It is assumed that this is not desired in the gate drive. At R_g=1.63Ω the gate current will take on its non-oscillating maximum:

$$\hat{I}_{\max(non-osc)} \approx 0.74 \cdot \frac{\Delta V_{Gate}}{R_{g,\min(non-osc)}} = 0.74 \cdot \frac{25V}{1.63\Omega} = 11.4A$$

For higher gate resistor values, the reduction factor will rise from 0.74 towards 1.0. However, the associated gate current will decrease and will always be smaller than $\hat{I}_{max(non\text{-}osc)}$.

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