Understanding Voids in Flip Chip Interconnects

Eric D. Perfecto

GLOBALFOUNDRIES
Tel: 1-845-894-4400

eric.perfecto@globalfoundries.com

This presentation is available only to CPMT members, any reproduction requires written permission from the presenter.

The slides included here do not represent an endorsement of GLOBALFOUNDRIES on the technologies presented, they were included by the author for educational purposes only.

Outline

1st and 2nd Level Packaging Introduction

Voids

- Ball Drop (BGA and u-BGA) Voids
- Solder Screen Voids
- Surface Voids
    - Fabrication Voids
- Stress Driven Voids
    - Thermal Stress Voids
    - Electromigration Stress Voids

Testing Methods

Summary

1st and 2nd Level Packaging Technology Elements

Chip- 1st level interconnect

C4(solder) + Underfill

Heat sinks

Cu, Al, complex design

1st level packages organic, ceramic

Heat spreaders

passive, active

BGA

Printed Wiring Board (PWB)

Thermal Interface Materials

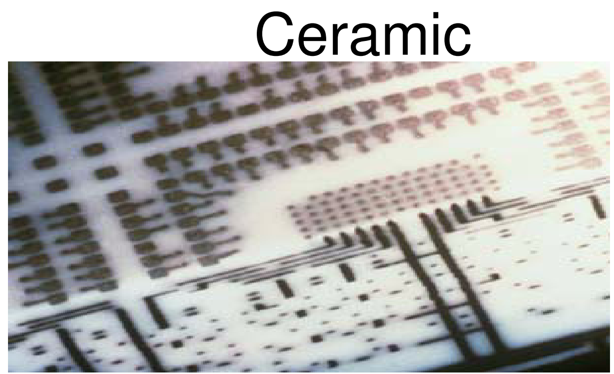
paste, gels, metals

1st-2nd level interconnect

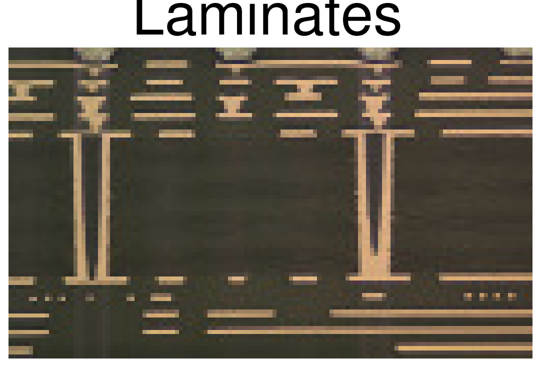
solder, mechanical

Chip Carrier Options:

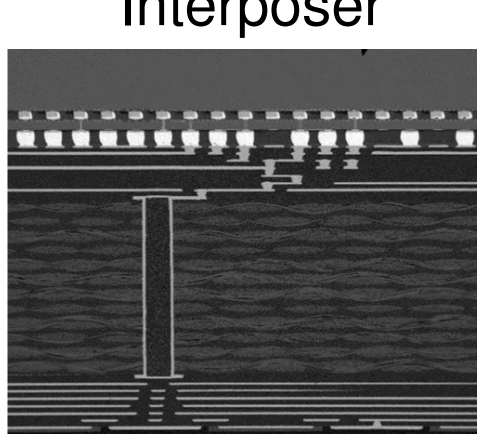
Ceramic



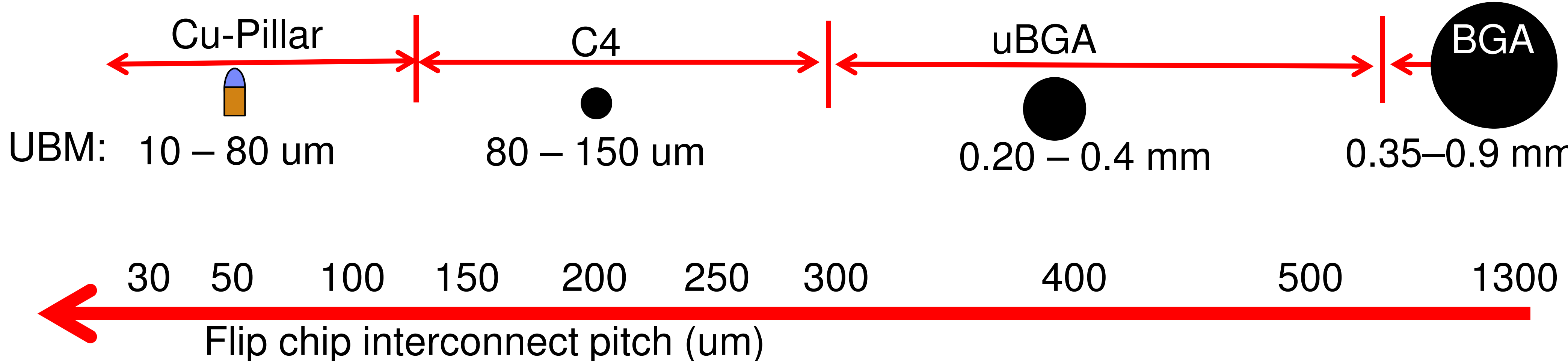
Laminates

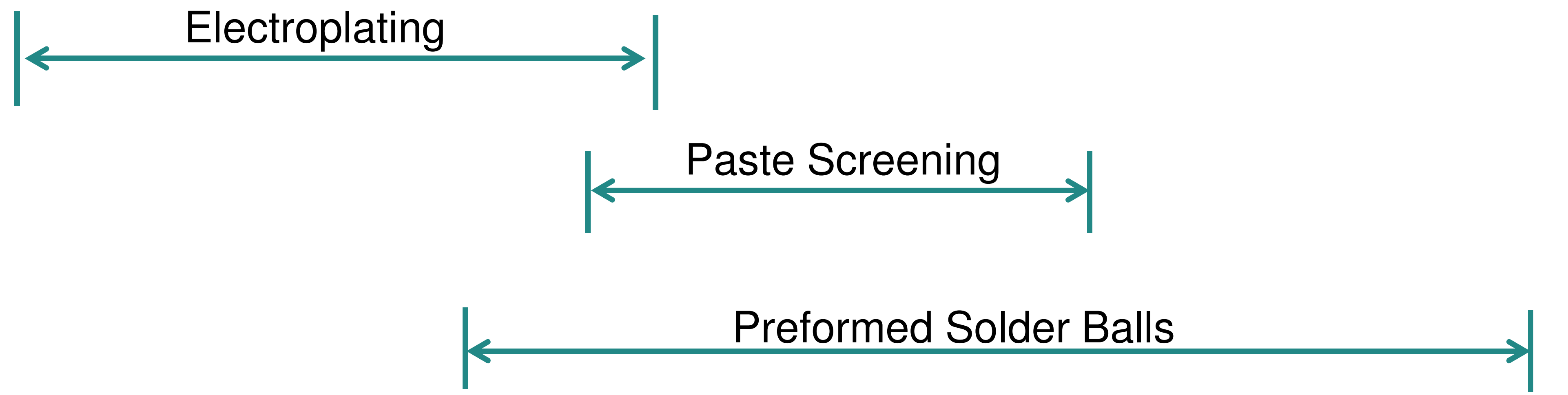


Interposer

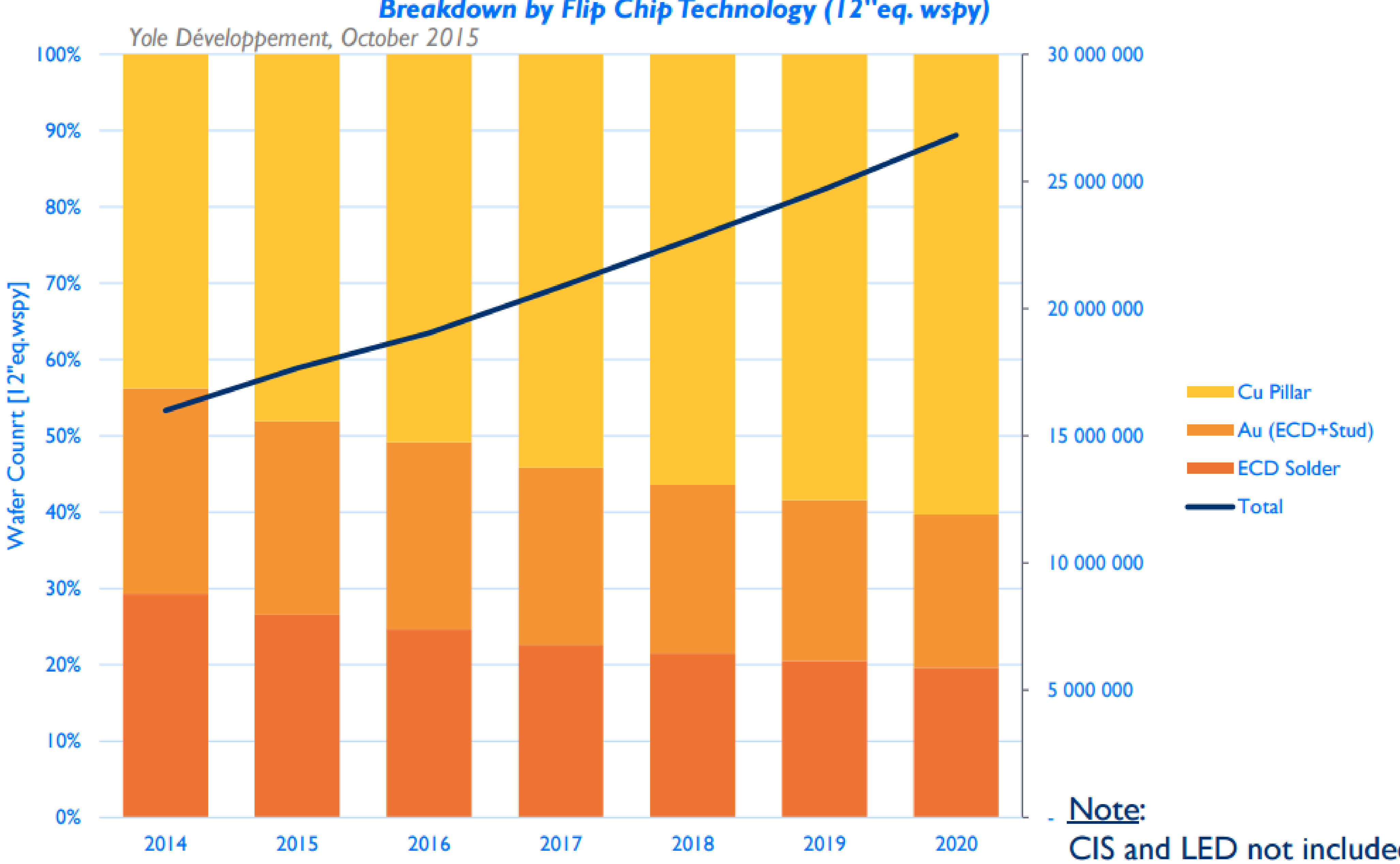


Bumping General Dimensions





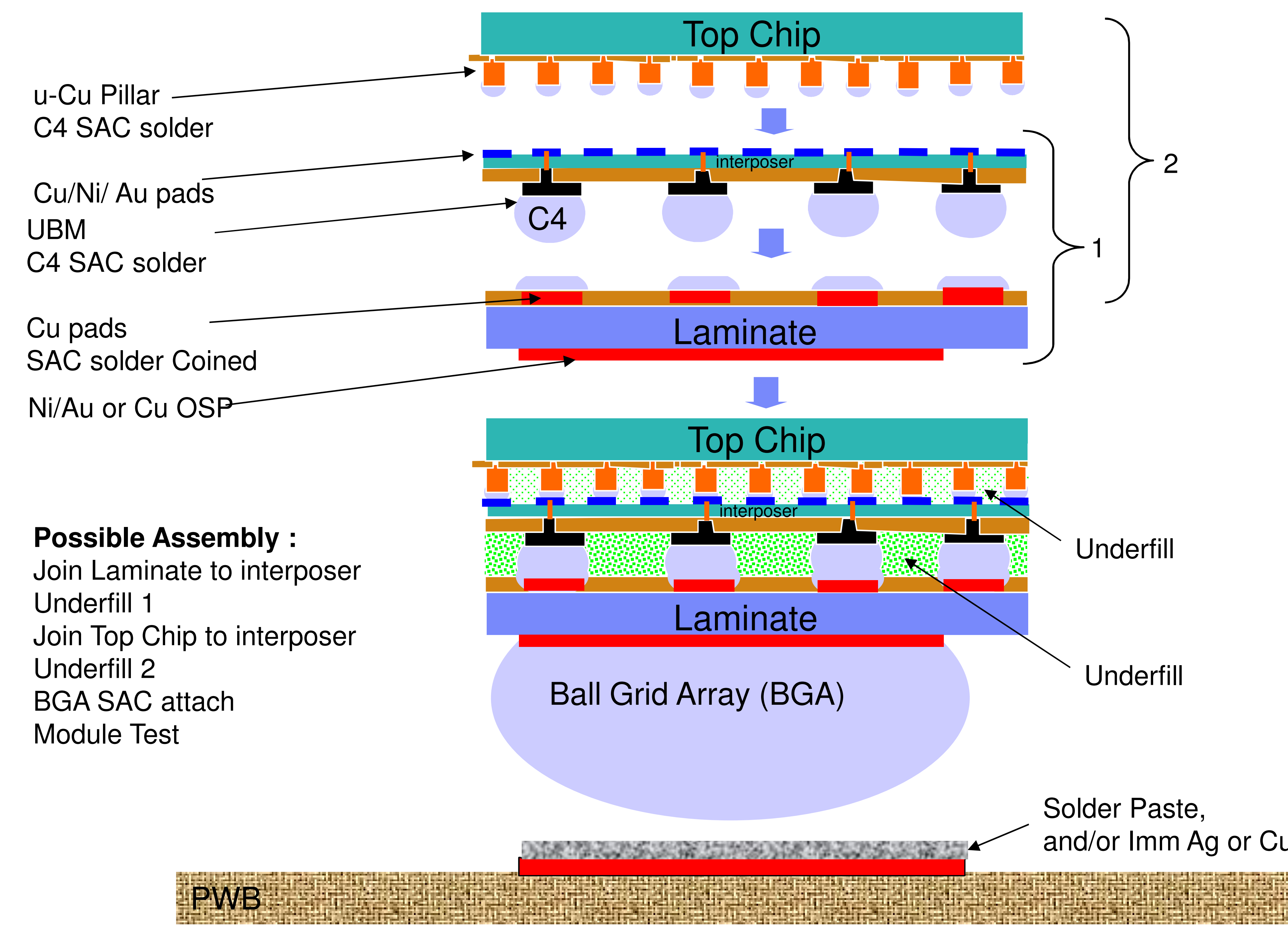
Flip Chip Bump Capacity Forecast



Cu Pillar is the fastest growing segment of the flip chip portfolio.

Source: 2015 Yole Flip Chip Report

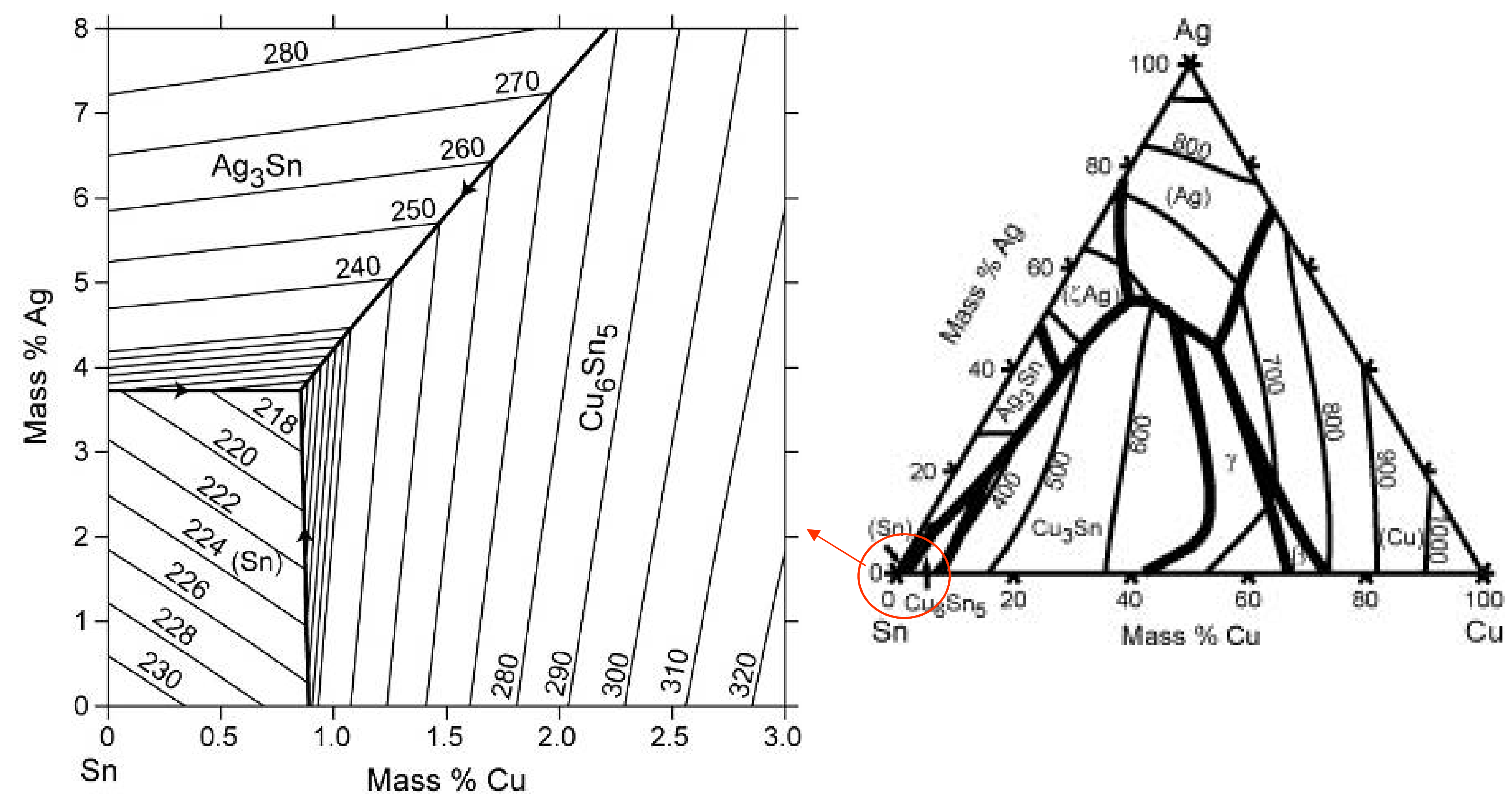
Interposer Assembly



Possible Assembly :

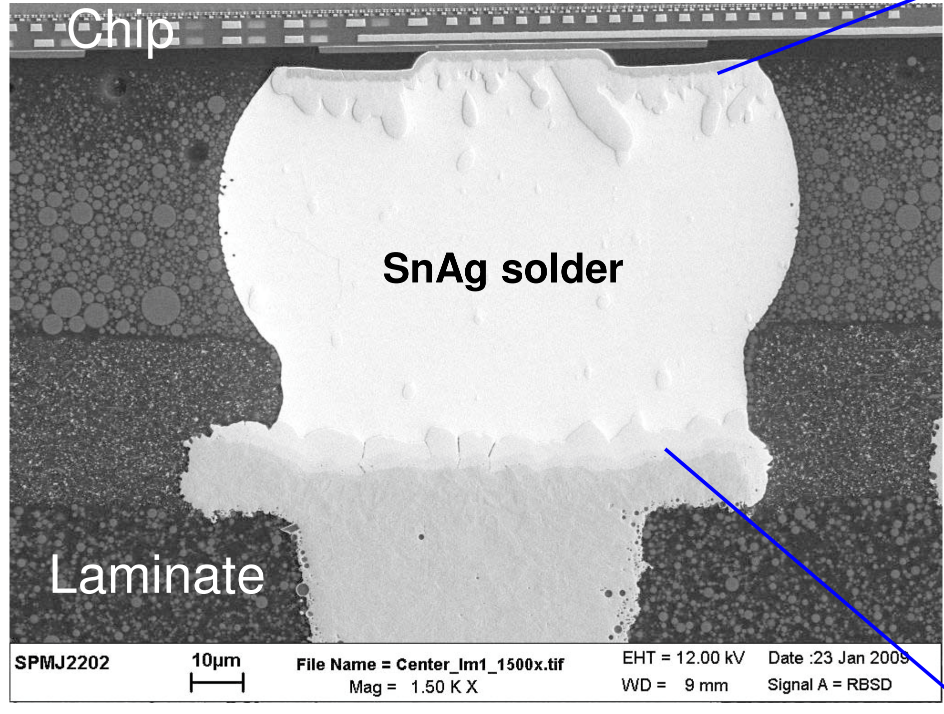
Join Laminate to interposer
Underfill 1
Join Top Chip to interposer
Underfill 2
BGA SAC attach
Module Test

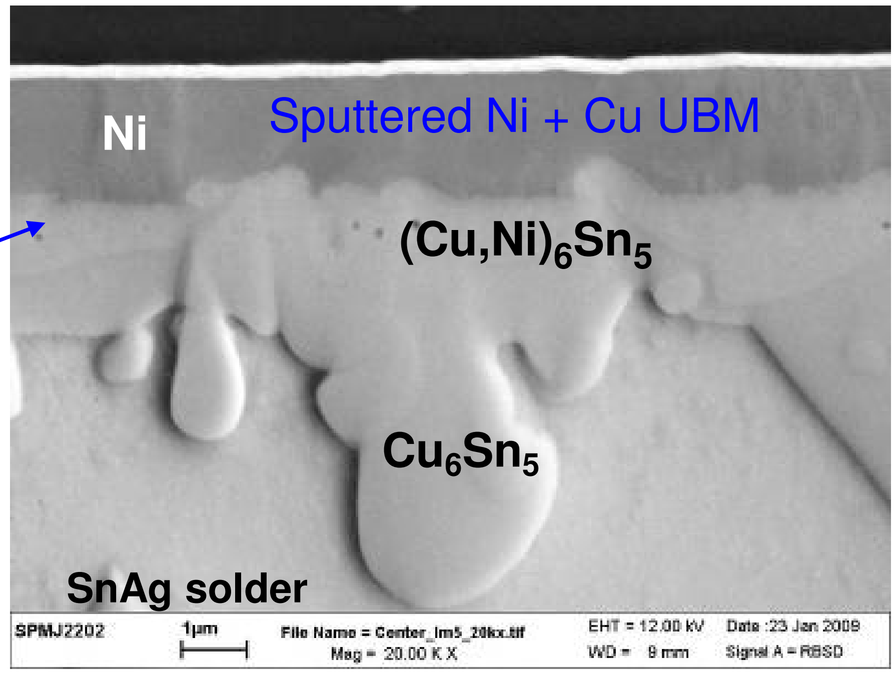
Sn-Ag-Cu Solder Ternary Phase Diagram

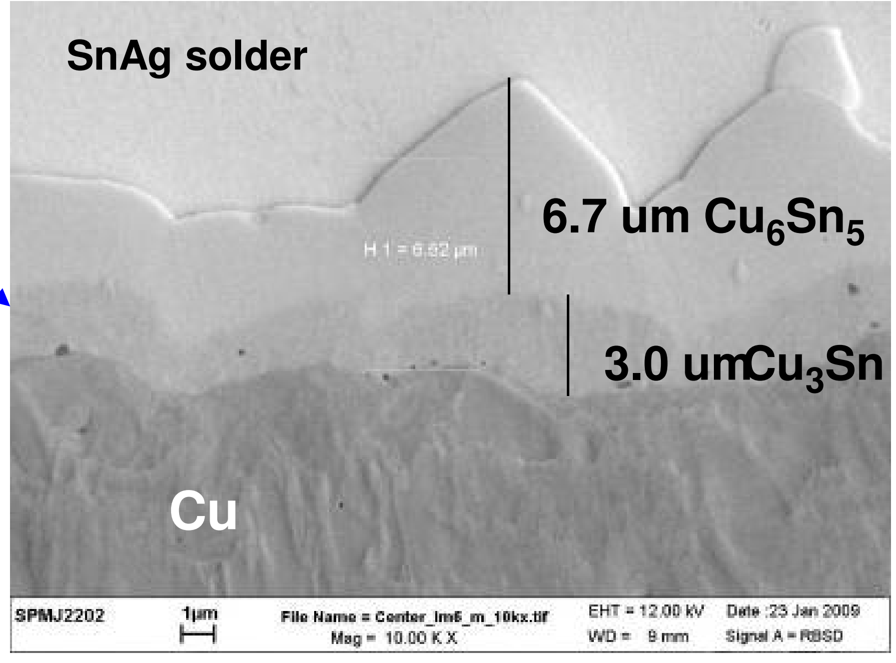


http://www.metallurgy.nist.gov/phase/solder/agcusn.html

Intermetallic Formation on Flip Chip Application







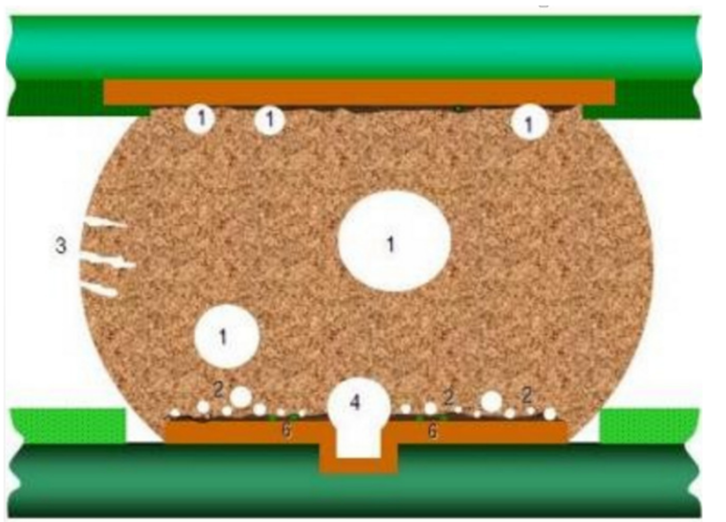
Ni/Cu is a very effective barrier for Pb-free applications – typically used on the chip side.

Thick Cu or solder on laminate side.

Ni-Solders results in $\mathbf{Ni_3Sn_4}$ Intermetallic (IMC)

BGA and u-BGA Void Types

	Types of Voids	Description
S	**Macrovoids**	Voids were formed as volatile ingredients of the fluxes within the solder paste, usually found everywhere in solder joint.
P	**Planar Microvoids**	Voids generated by anomalies in surface finish application process, generally located in one plane and found at the solder-to-land interface.
S	**Shrinkage Voids**	Caused by the solidification of SAC solders, formed as linear cracks with rough edges from the surface of the solder joints.
P	**Micro-via Voids**	Caused by microvias in lands.
P	**Pinhole Voids**	Voids generated by excursions in the copper plating process at board supplier.



1: Macrovoids
2: Planar Microvoids
3: Shrinkage Voids
4: Micro-Via Voids
5: IMC Microvoids
6: Pinhole Voids

S = Solder

P= Landing Pad

R. Aspandiar , presentation at SMTA Chapter meeting (2005)
R. Aspandiar, “Voids in Solder Joints,” SMTA Journal, V19 I4, 2006

BGA: Shrinkage and Pinhole Voids

Shrinkage Voids:

Hot tear voids are formed during the solidification of the solder during BGA joining. Increase cooling rate can minimize this defect.

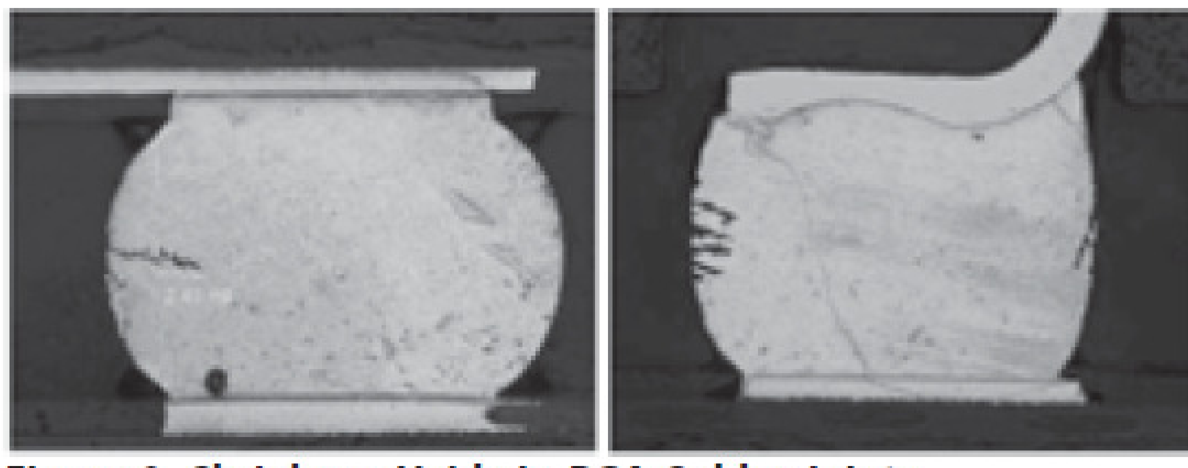


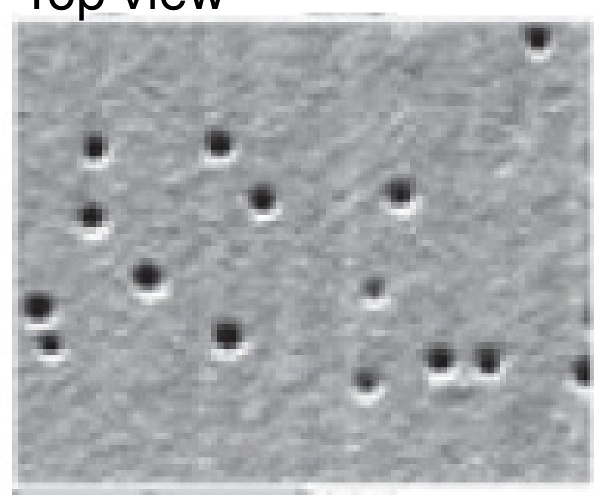
Figure 9. Shrinkage Voids in BGA Solder Joints.

Pinhole Microvoids:

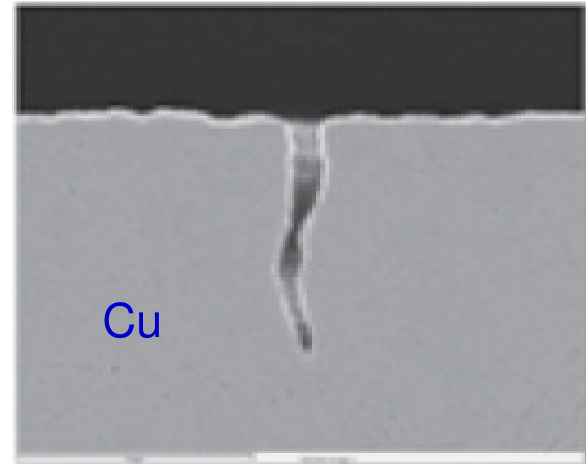
1 to 3 um in diameter crevices in the plated Cu matrix of the BGA receiving pad can entrap fluids resulting on void formation above IMC at ball attach.

Pinhole Microvoids:

Top view

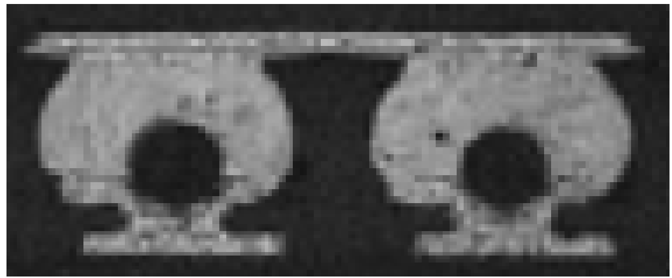


x-section



Raiyo F. Aspandiar, "Voids in Solder Joints," SMTA Journal, V19, Issue 4, 2006

BGA: Microvia Voids

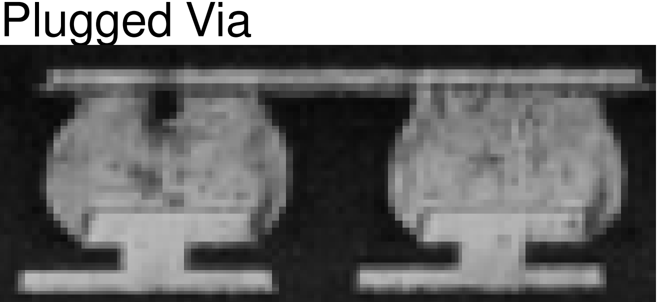


Raiyo F. Aspandiar, “Voids in Solder Joints,” SMTA Journal, V19, Issue 4, 2006

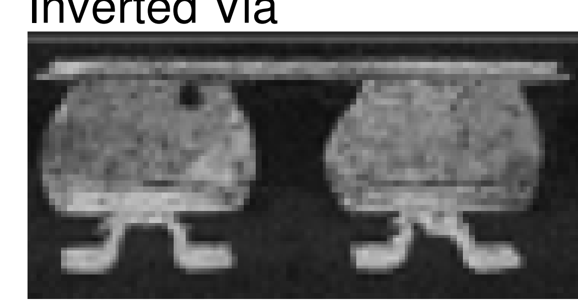
Microvia Voids:

Via cavities within the BGA landing pad results on poor solder paste coverage, entrapping air. Large bubbles are attached to the UBM and do not escape. No solder paste fill results in increased voids propensity.

Plugged Via



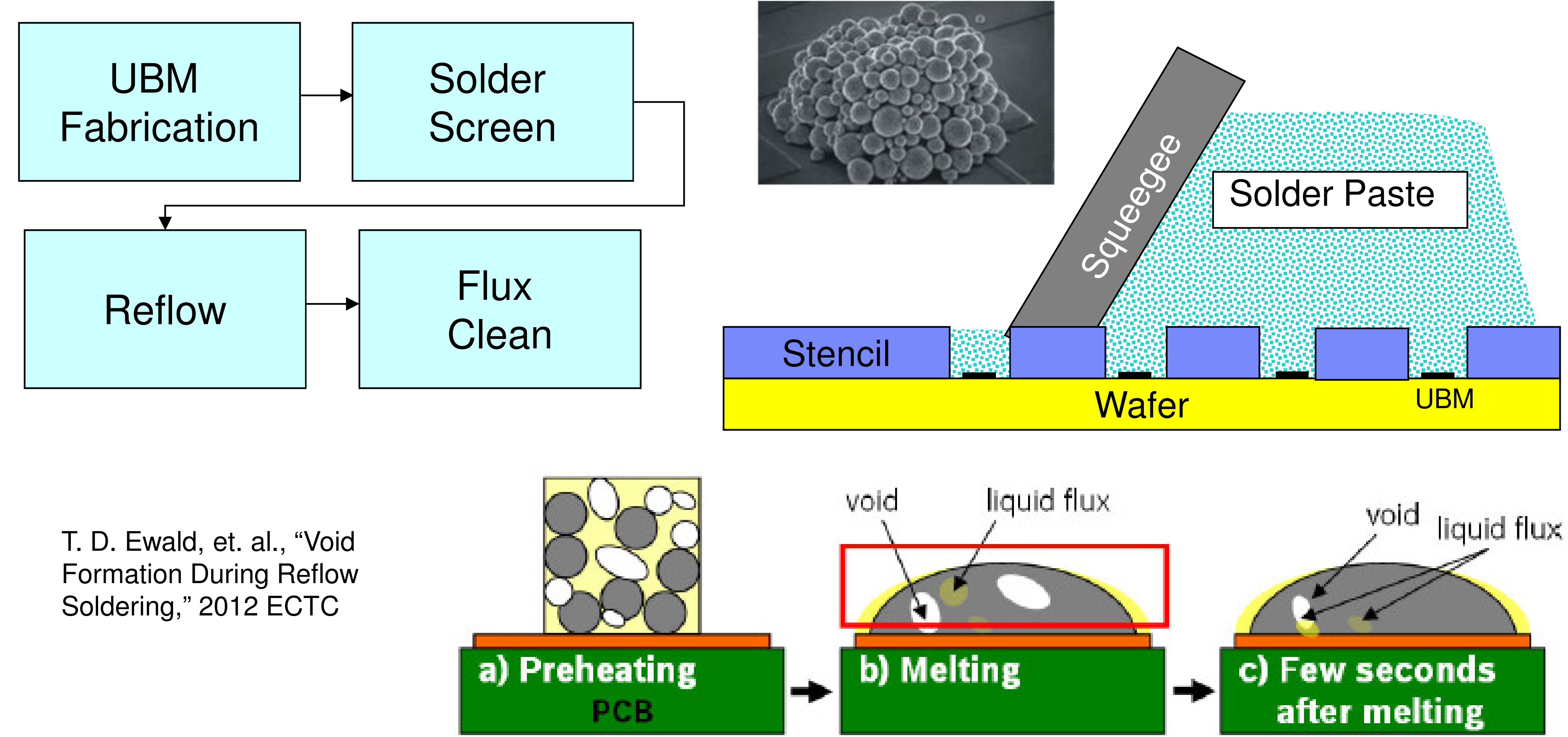
Inverted Via



Mitigation:

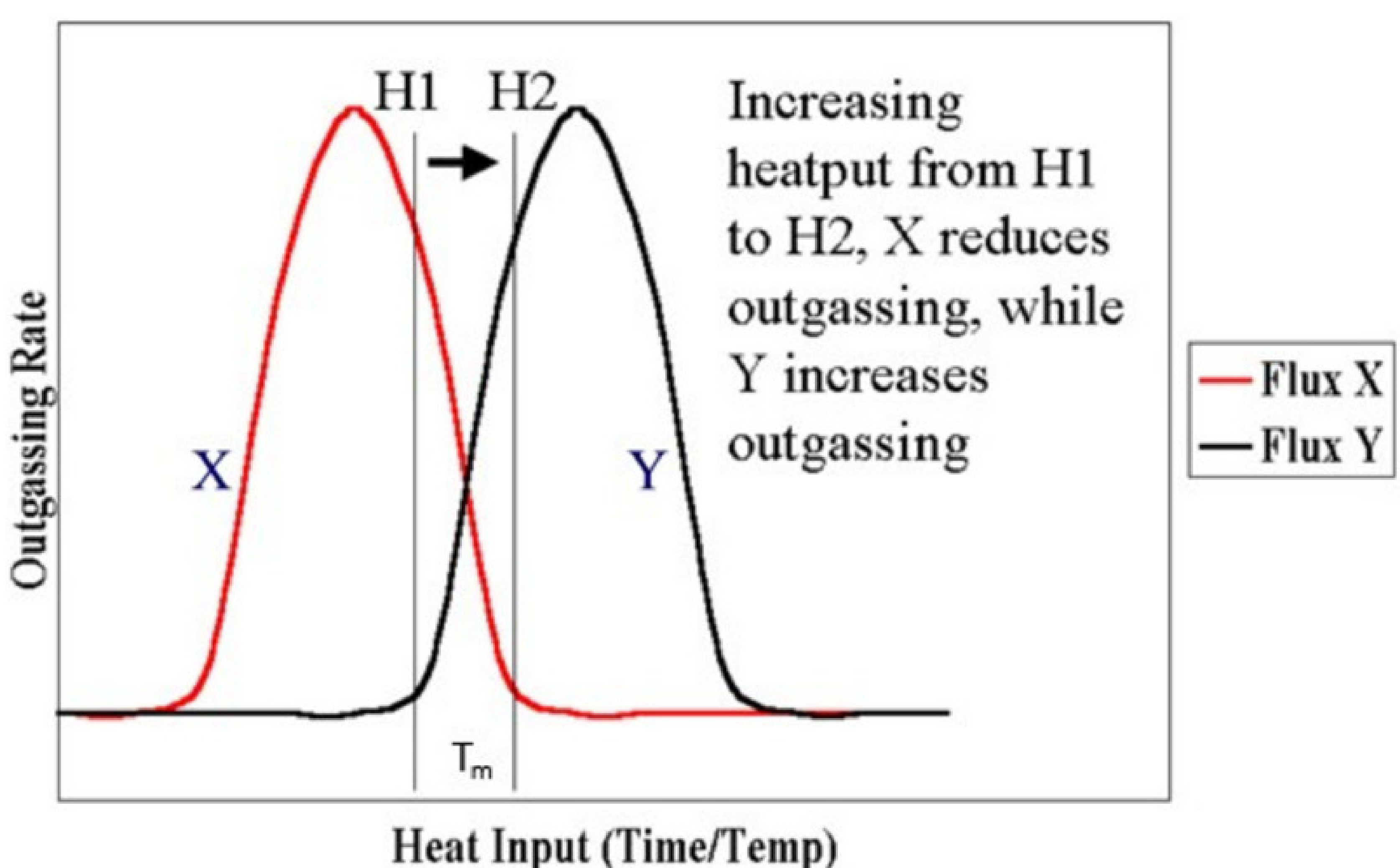
- Eliminate the via topography: dog-bone, plugged or inverted microvias.
- Increase via size for better fill
- Optimize surface finishing for solder wetting and better fill.
- On chip to laminate joining, solder paste is <u>first reflowed</u> and coined (mechanically flattened) prior to chip joining.

Voids in Flip Chip Stencil Printing



- Solder paste voids can be form during reflow due to solder dewetting.
- Flux volume, Flux evap. temperature, paste volume, pad surface area, pad surface finish and reflow environment, all play a role in void formation.

Solder paste Flux Selection and Voids



http://www.indium.com/blog/voiding-in-bgas.php

BGA: Planar Voids Root Cause and Solution

Microetch preceding plating → **Silver Immersion Plating** → **Subsequent reflow/assembly**

"High Risk" Process Cycle:

Unfavorable peroxide etch creates micro-topography and sites susceptible to subsequent cave formation

Caves formed when high plating rate electrolyte forms silver roof over micro-topography and high risk sites. Cave volume magnified as roof forms

During reflow cycle, caves are exposed via solder melt, silver dissolution, and copper consumption. Voids formed do not escape

~10um

Optimized Process Cycle:

Preferred etch creates "rolling" topography and less high risk sites for subsequent cave formation

Minimal cave formation: Lower rate plating electrolyte permits controlled plating and copper displacement over "rolling" copper surface

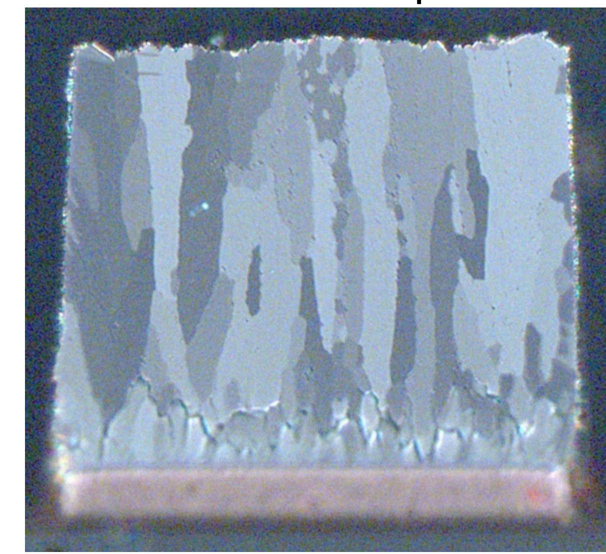
No significant void formation due to minimal cave presence entering reflow operation

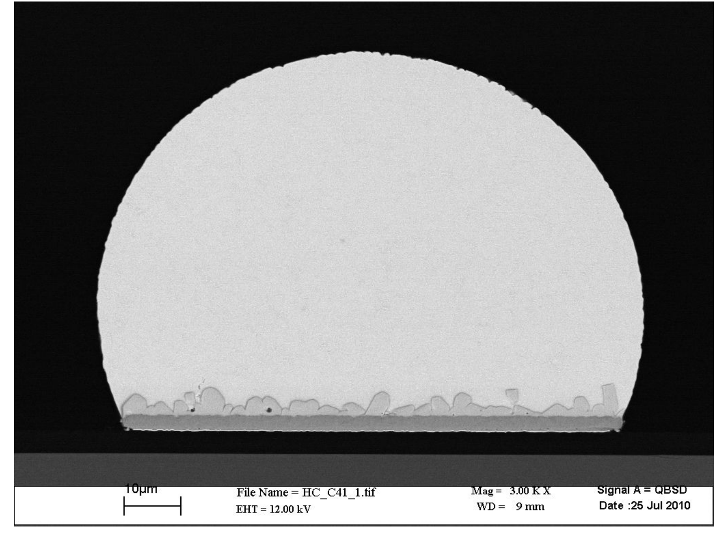
D. Cullen, et. al., "Eliminating Microvoid Risk Via an Optimized Surface Finish Process," International Conf. on Lead-free Soldering, Toronto, CA, May 2006.

Pattern Electroplating Process

Electroplated Pb-free Process	
Sputter Seed	
Resist Apply Define Pattern	
Electroplate UBM (Cu, Ni) + SnAg solder	
Resist Strip	
Seed Etch	
Reflow	

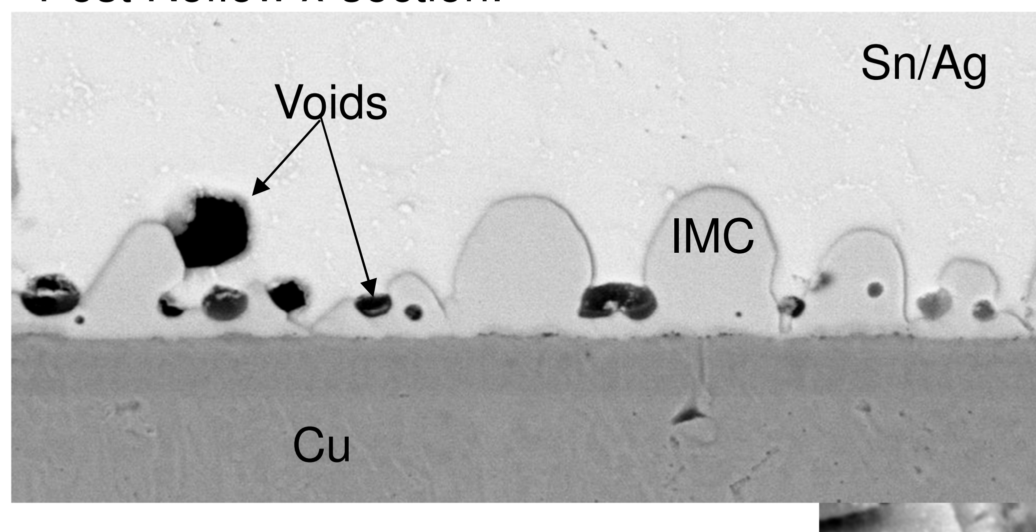
UBM and C4 – As plated





Electroplating Induced Interfacial (Planar) Voids

Post Reflow x-section:



Top view SEM of expose IMC after the solder was chemically etched:

Voids are between IMC and solder

Voids

IMC

1µm File Name = C_4.tif EHT = 15.00 kV Mag = 10.00 K X WD = 8 mm Signal A = SE2 Date :17 Jul 2010

C. L. Arvin, E. Perfecto, et. al, "Interfacial Voids at the Under Bump Metallurgy and Solder Interface," ECS in Boston, MA, Fall 2011.

Incorporation of Species at SnAg Plating which contribute to Void Formation

- **Corrosion of bottom metal in SnAg bath**
- **Co-deposition of organics within solder (more prevalent as bath ages)**
- **Colloidal deposition**

Ag complexer
- Prevent deposition of Ag in solution
- Slows mass transport of Ag to surface
- Release during electron transfer

Source of Organic to Volatilize

Colloids

Corrosion of UBM leads to Ag with organics

Co-dep of organics

Mass Transfer

Double Layer

H^+ MS^-

R1 Cu^{2+}

Ag

Sn^{2+}

Adsorption

Electron Transfer

Sn^{2+}_{ads}

$Sn^{2+} + 2e^- \rightarrow Sn$

Sn

R_1

Ag^+

R1

Ag^+_{ads}

$\rightarrow Ag^+_{ads} \rightarrow Ag$

R_1 R_2 R_3

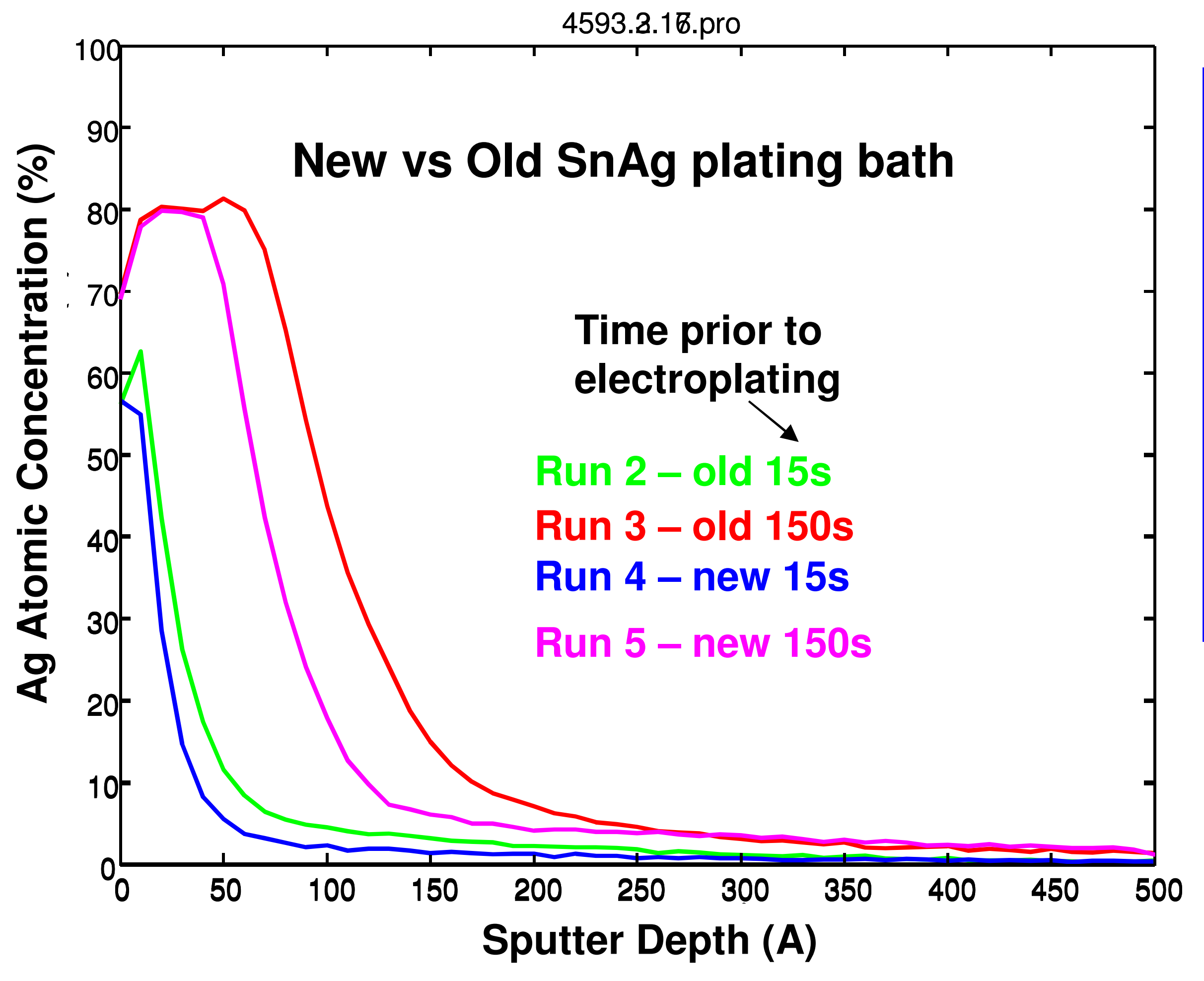
$Ag^+ + e^- \rightarrow Ag$

$Cu \rightarrow 2e^- + Cu^{2+}$

$Ag^+ + e^- \rightarrow Ag$

C. L. Arvin, E. Perfecto, et. al, "Interfacial Voids at the Under Bump Metallurgy and Solder Interface," ECS in Boston, MA, Fall 2011.

Electroplating Induced Interfacial (Planar) Voids



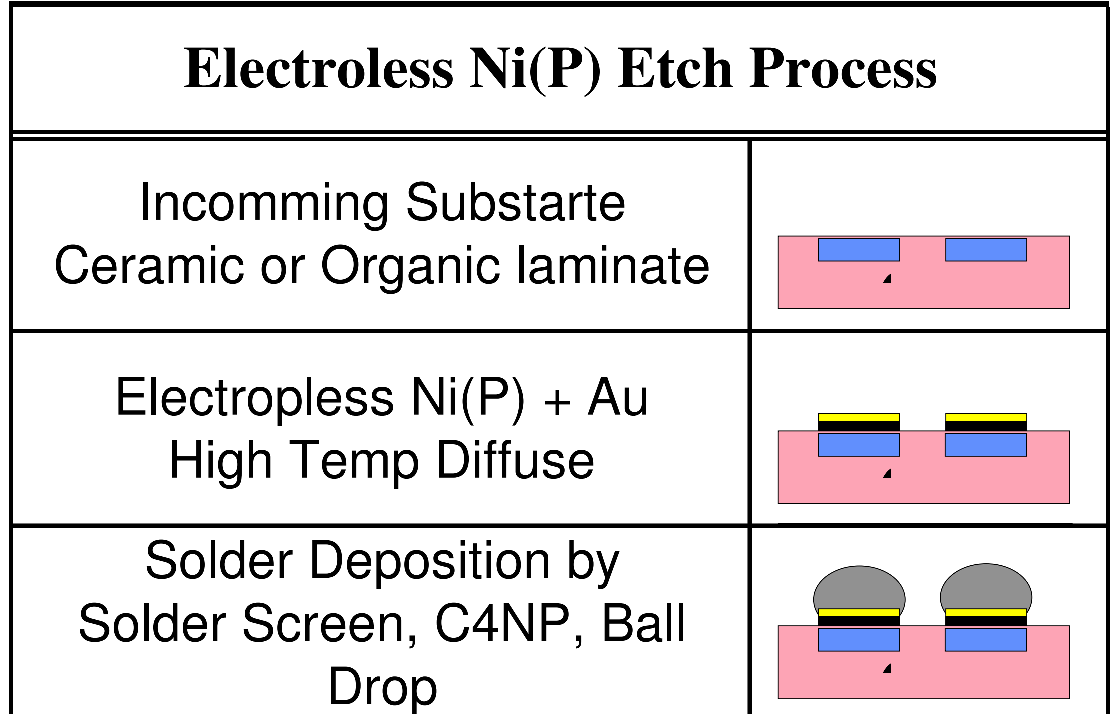
Experimental matrix:

- Plate pure metal (Ni, Cu,)
- Immerse in SnAg bath (5 sec or 150sec)
- Repeat with old SnAg plating bath (5sec or 150 sec)
- Depth profile using Auger

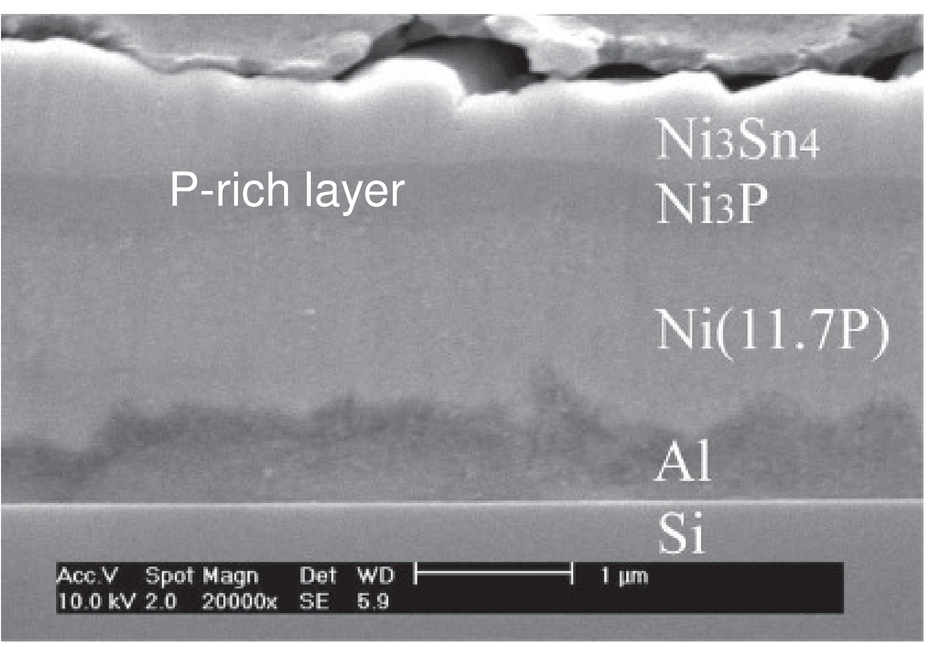
- Bath age impacts the on-set of interfacial voids
- Propensity for Ag to corrode Ni (zero @ 150 sec) < Cu (25A at 5 sec / 110A at 150 sec)
- Propensity to form room temperature intermetallics with solder Cu >> Ni

C. L. Arvin, E. Perfecto, et. al, "Interfacial Voids at the Under Bump Metallurgy and Solder Interface," ECS in Boston, MA, Fall 2011.

Electroless Ni(P) UBM



Electroless Ni(P) Etch Process	
Incomming Substarte Ceramic or Organic laminate	
Electropless Ni(P) + Au High Temp Diffuse	
Solder Deposition by Solder Screen, C4NP, Ball Drop	

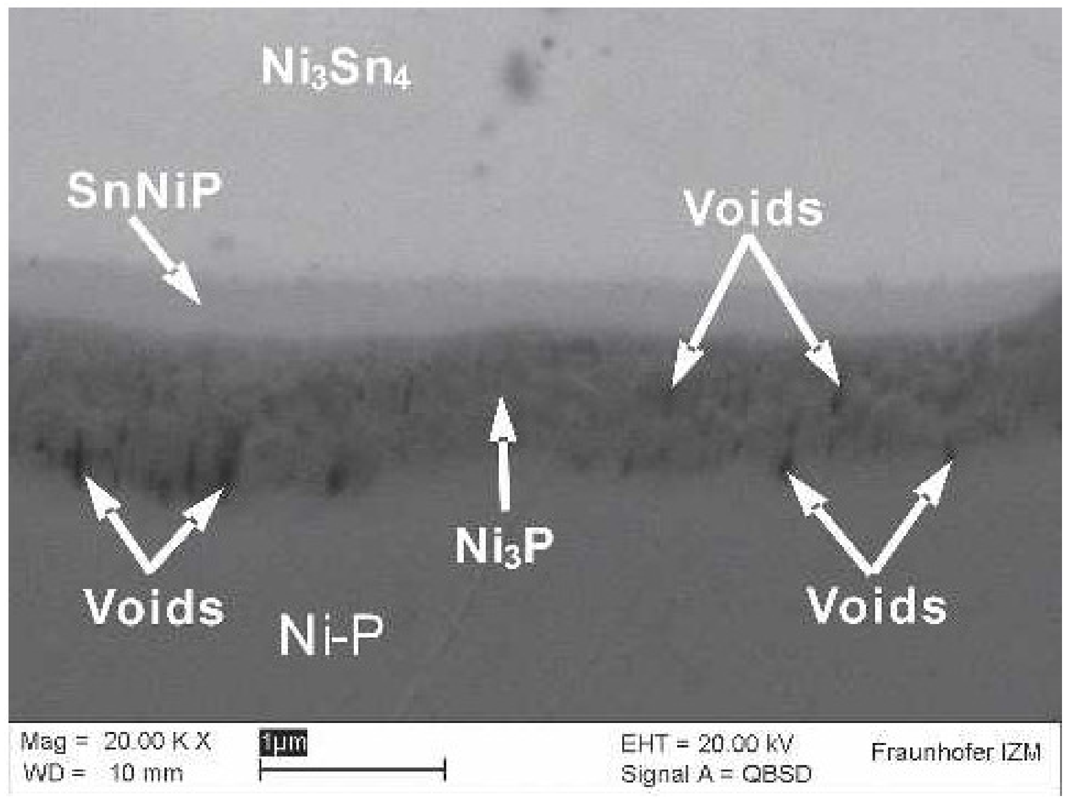


Upon joining the Sn-based solder to the electroless Ni(P) UBM pad, the Ni reacts with the solder forming a Ni_3Sn_4 intermetallic. This reaction results in the formation of a crystalline Ni_3P layer also known as P-rich layer between the IMC and the Ni(P). Micro voids form on this layer.

NiV, NiW and NiSi UBM barrier have the same problem as Ni(P). This is known as reaction-assisted crystallization.

HTS: Electroless Ni(P) voids

Sn3.5%Ag
aged at 150C
for 1000hrs



Voids are generated in the crystalline Ni_3P layer after thermal stress.

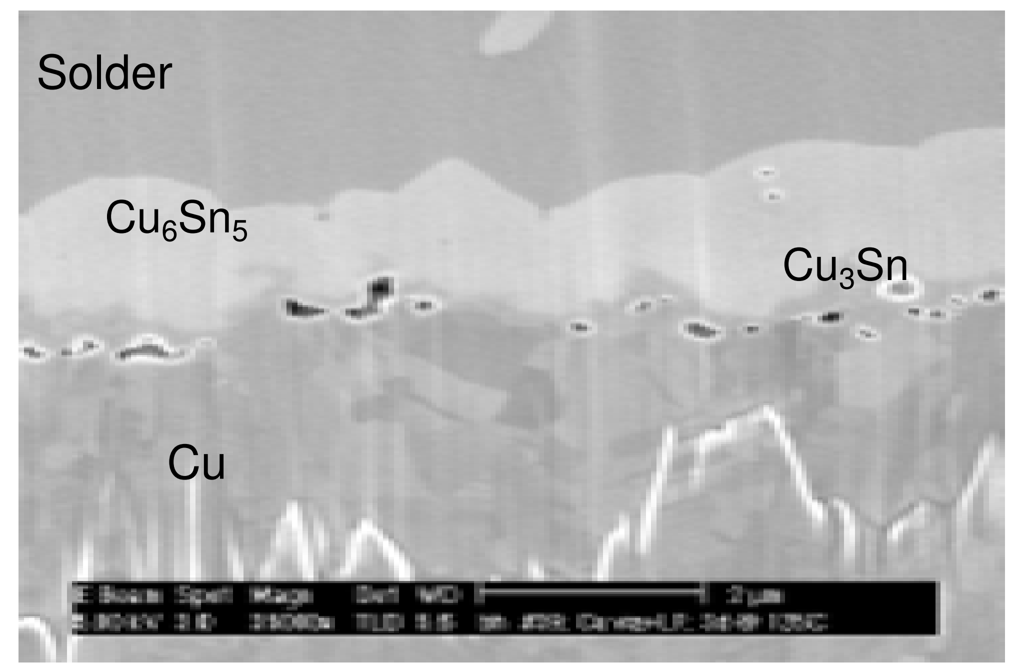
- ENEC/OSP (Electroless Ni(P) + Electroless Copper + OSP) results in a robust $(Cu, Ni)_6Sn_5$ IMC which reduces the Ni consumption and so the Ni_3P formation.

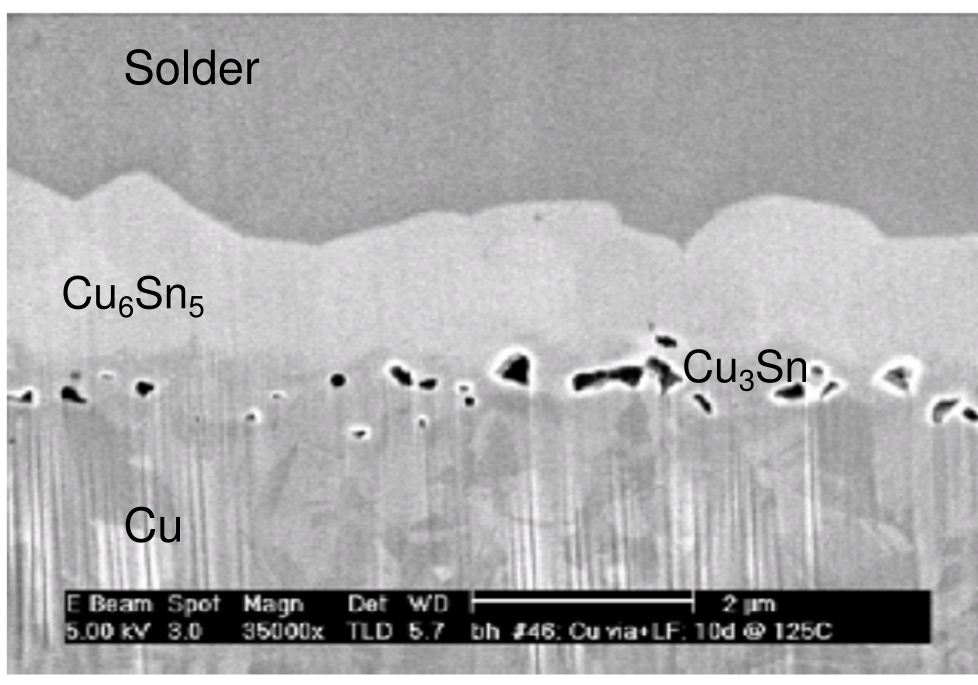
M. L. Huang, et al, “Morphology and growth kinetics of intermetallic compounds in solid-state interfacial reaction of electroless NiP with Sn-based lead-free solders,” Journal of Electronic Materials, January 2006

Young-Doo Jeon, et. at., “Thin Electroless Cu/OSP on Electroless Ni as a Novel Surface Finish Joints,” 2006 ECTC

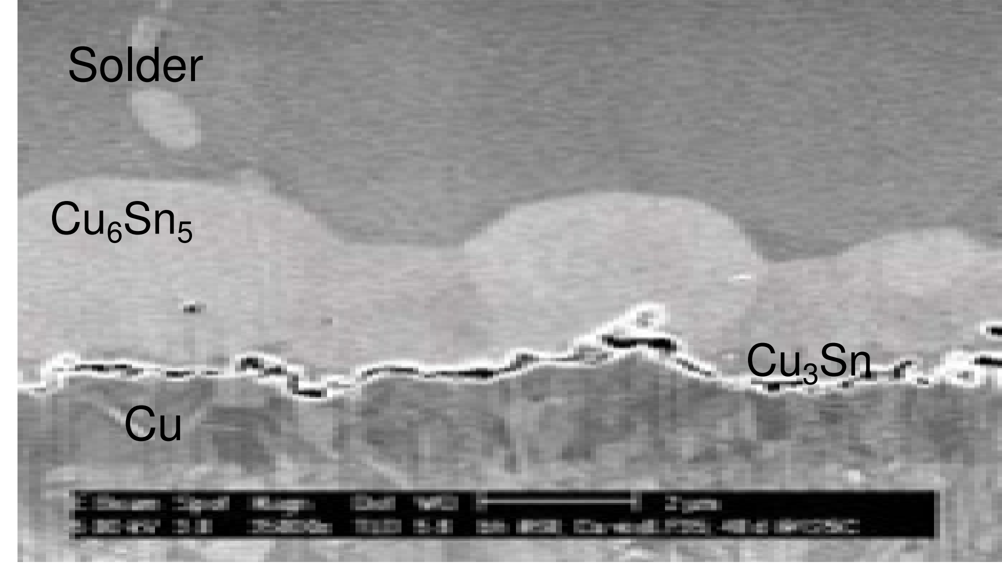
HTS Stress and Kirkendall Voids

3 days of 125°C aging





40 days of 125°C aging



Tz-Cheng Chiu, et. al., “Effect of Thermal Aging on Board Level Drop Reliability for Pb-free BGA Packages,” 2004 ECTC

Kirkendall Voids and IMC Voids

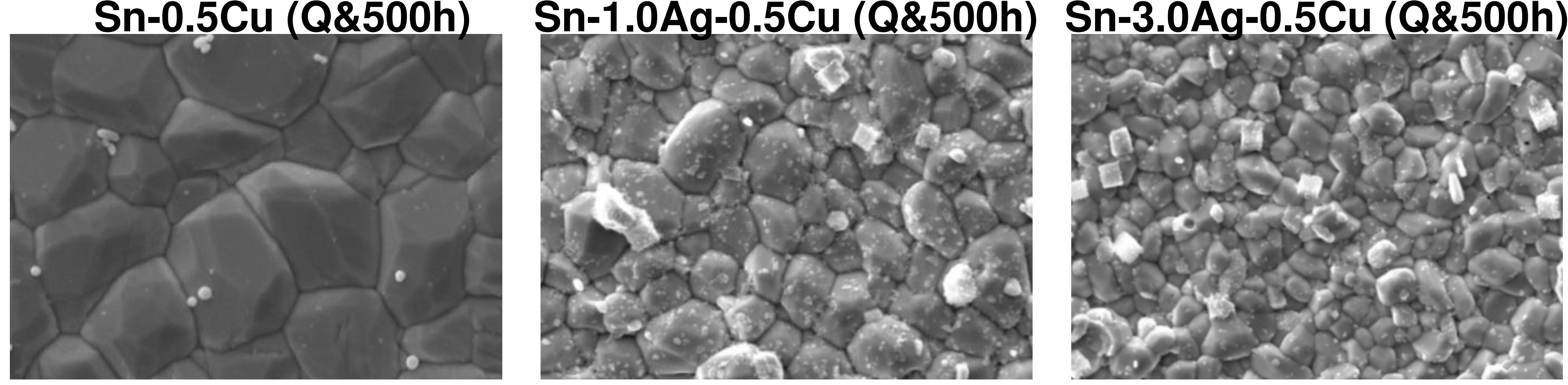
Kirkendell Voids - Mechanism 1:
- During Joining of Sn solders with Cu surface the Cu_6Sn_5 intermetallic crystallizes, along Cu layer, stopping further dissolution of Cu.
- Also a thin intermetallic layer, Cu_3Sn, forms between Cu and Cu_6Sn_5.
- During thermal aging, atomic vacancies are left by Cu atoms migration from the Cu side – which are not filled by the Sn atoms.
- These vacancies coalesce into the so called Kirkendall voids at Cu - Cu_3Sn interface, and in Cu_3Sn layer.
- Voids can increase to form a discontinuous layer.

Impurities - Mechanism 2:
- Impurities in the plated Cu resulting in morphology and diffusion changes and void generation.

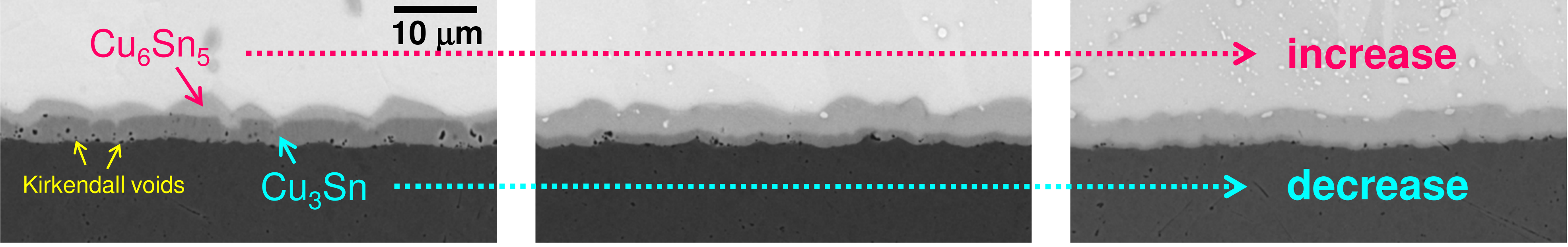
Vol. Reduction - Mechanism 3:
- Volume reduction and therefore voids during the conversion of Cu_6Sn_5 to Cu_3Sn.

Mitigation:
- Replacing the Cu OSP layer with a Ni(P) or Ni(P)/Cu layer.
- Solder additives such as Ni, Bi, Zn.
- Increase purity of plated Cu.

Effect of %Ag in Cu_3Sn IMCs Growth



After thermal aging at 150 C/500 hrs, the size of Cu_6Sn_5 grains remains stable.



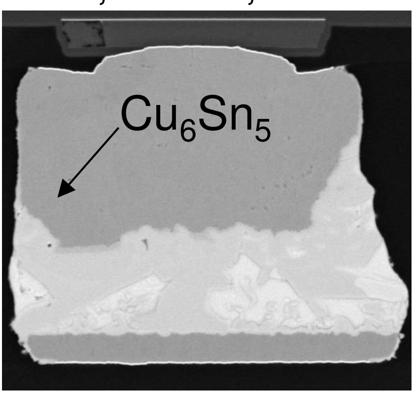
Cu_3Sn layer was reduced with increase of Ag% in the solder, but the thickness of total IMCs was similar. (Kirkendall voids reduction)

Increase in %Ag, reduces the Cu_6Sn_5 grain size

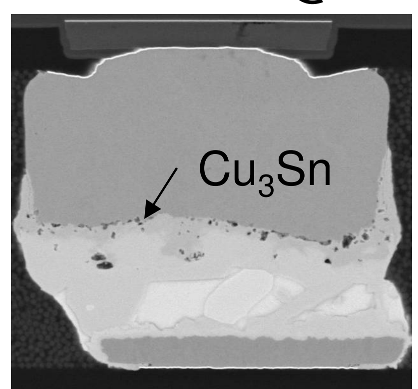
Moon Gi Cho, et. al., “Effect of Ag on Ripening Growth of Cu6Sn5 Grains,” 2010 ECTC

Kirkendall Void in Cu_3Sn IMC   Stack: 14Cu/15SnAg

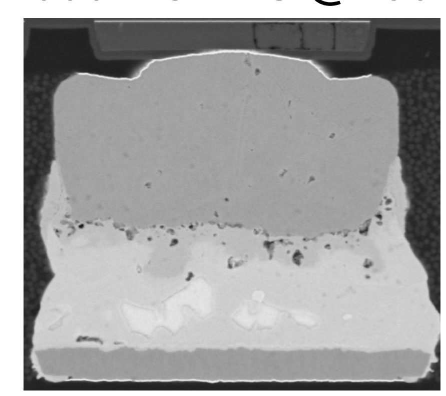
T0, no UF,



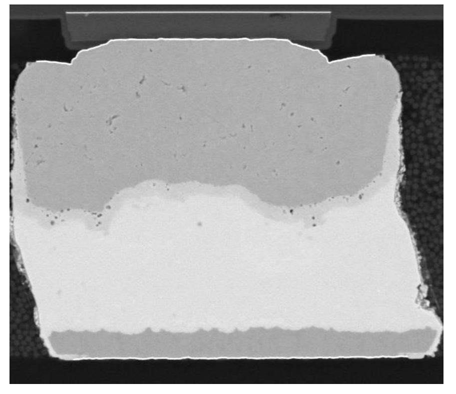
T0+ 500 hrs HTS@150C, UF



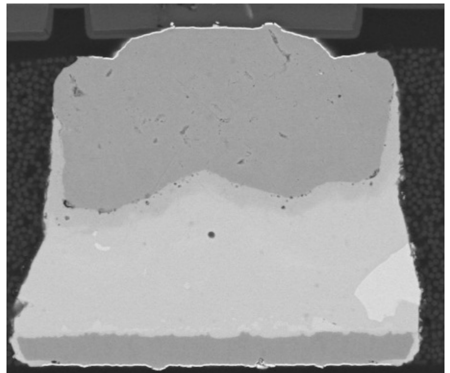
T0+1000 hrs HTS @150C, UF



T0+ 250C, 30 min, UF



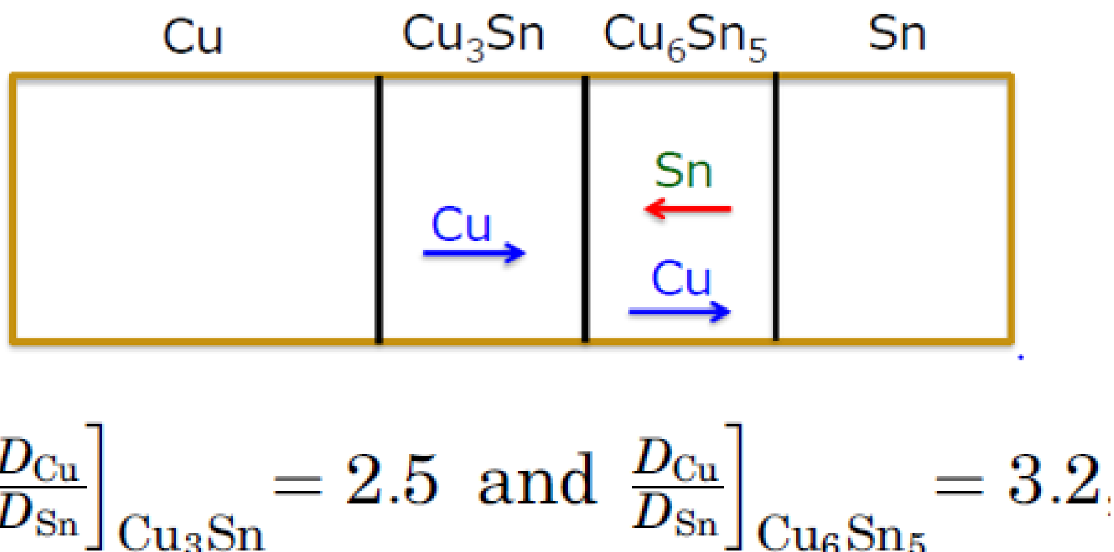
T0+ 250C, 30 min + 1000hrs HTS @150C, UF



- The size and number of Kirkendall voids increased with 500 hrs at 150 C HTS and remained stable at 1000hrs HTS.
- Full conversion of intermetallic prior to HTS testing mitigated the Cu_3Sn IMC and the amount of Kirkendall voids at that intermetallic.

H. Zhang, E. Perfecto, et.al., "An Effective Method for Full Solder Intermetallic Compound Formation and Kirkendall Void Control in Sn-base Solder Micro-joints," 2015 ECTC

Microvoiding Vs. Kirkendall Voids



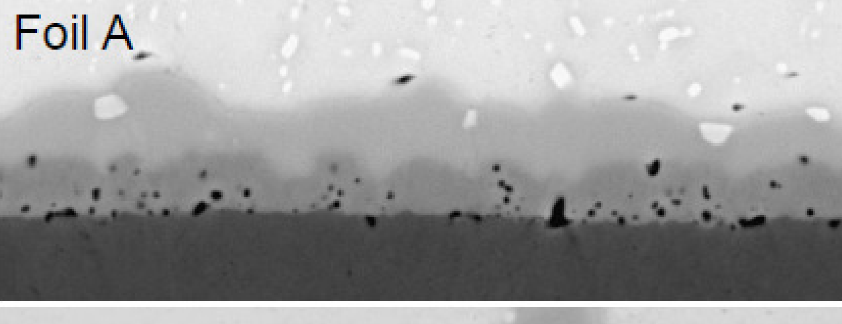
Where D_{Cu} and D_{Sn} are the intrinsic diffusion coefficients of Cu and Sn, respectively.

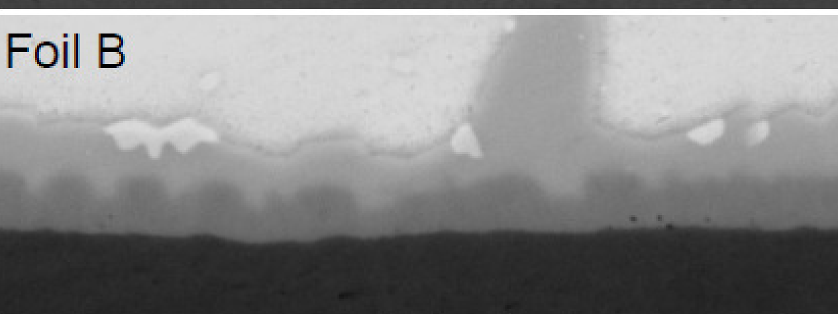
- If the voids are solely due to diffusion effects, the voids will concentrate at the Cu_3Sn–Cu_6Sn_5 interface.

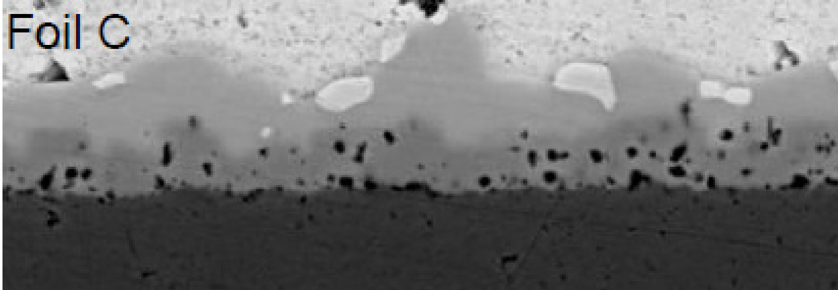
S. Kumar, et. al., “Microvoid Formation at Solder-Cooper Interfaces During Annealing,” JEM V40, No.12, 2011

Voids Generation vs Impurities in Plated Cu

Commercial Cu foils for PCB







1 week@175°C

SIMS impurity measurement (ppm)

	Foil A	Foil B	Foil C
Cl	**57**	**8**	**59**
C	**28**	**8**	**47**
O	**5**	**1**	**12**
S	**0.5**	**0.02**	**6**

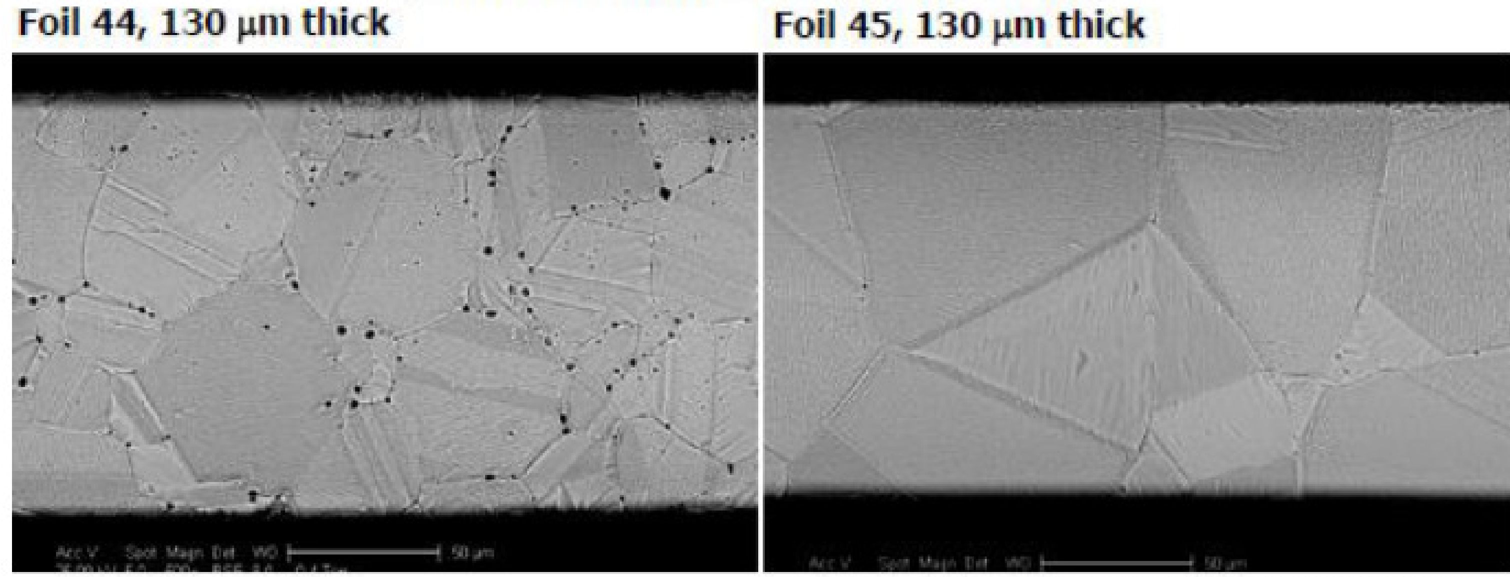
In the high voiding Cu foils, the impurity levels are in the tens of ppm or less

Bath additives:
- Suppressor: polyethylene glycol (PEG)
- Brightener: Bis-(3-sulphopropyl)-disulfide (SPS)
- Accelerators: Thiol (-SH) or Sulfonate (-SO3)

From P. Borgersen

Y. Liu, L. Yin, et. at , IEEE Trans. Comp. Pack. Techno. 33,127 (2010)

Cu Impurity Voids and UBM



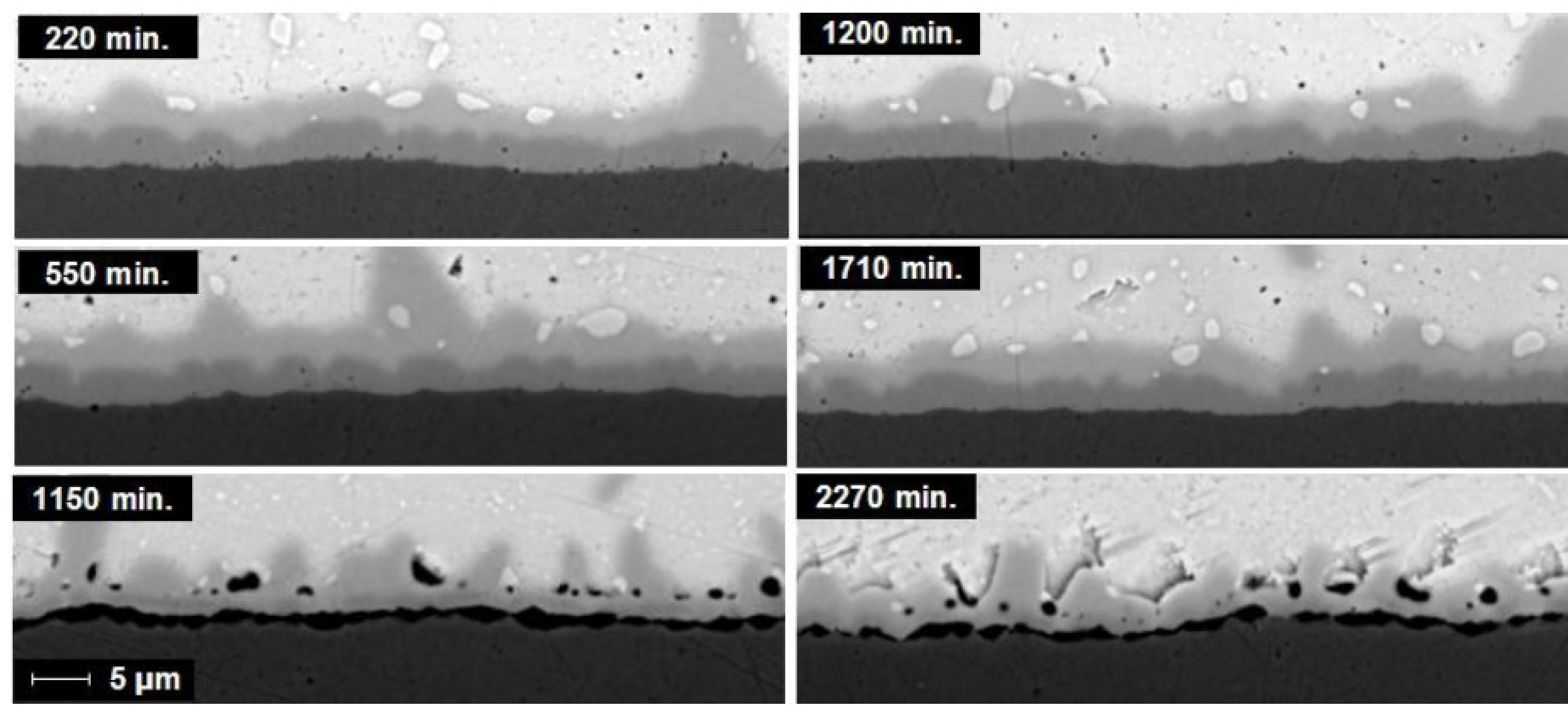
Correlation between impurities that can be decomposed/gasified and voiding is clear, and they do affect further grain growth:

From P. Borgersen

L Yin and P. Borgersen, J. Mater. Res. 25, 455 (2011)

Voids Understanding: Cu Plating Bath Age

SPS+PEG+Cl-, 10 mA/cm^2 SPS replenishment at 1160 min.



At 550 and 1710 min. the voiding level appears to be the least.

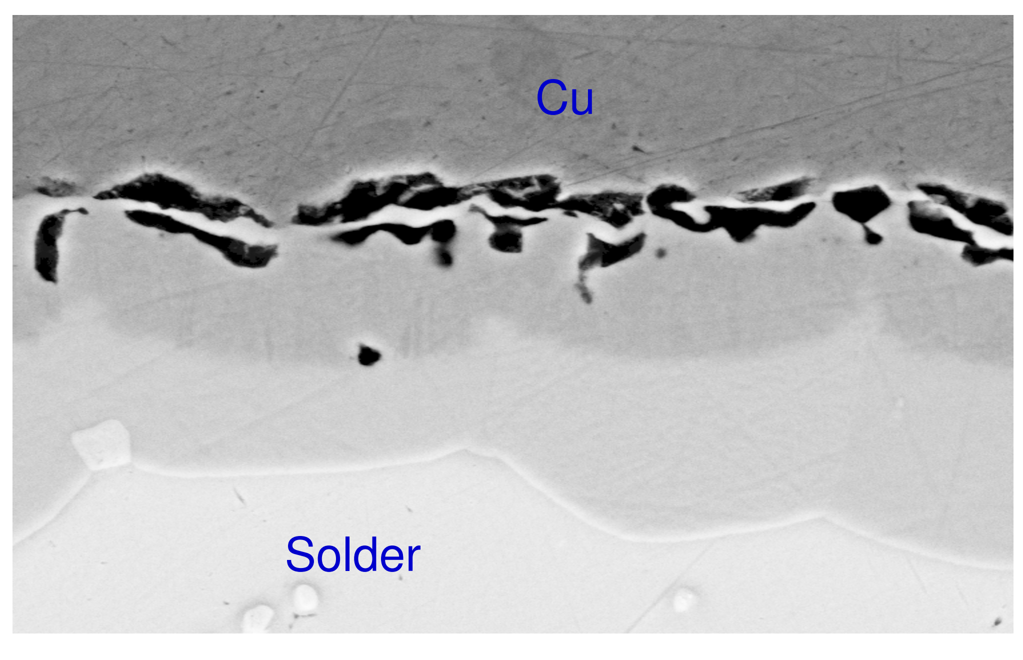
- Bath Temperature and current density can also modulate void formation.

From P. Borgersen

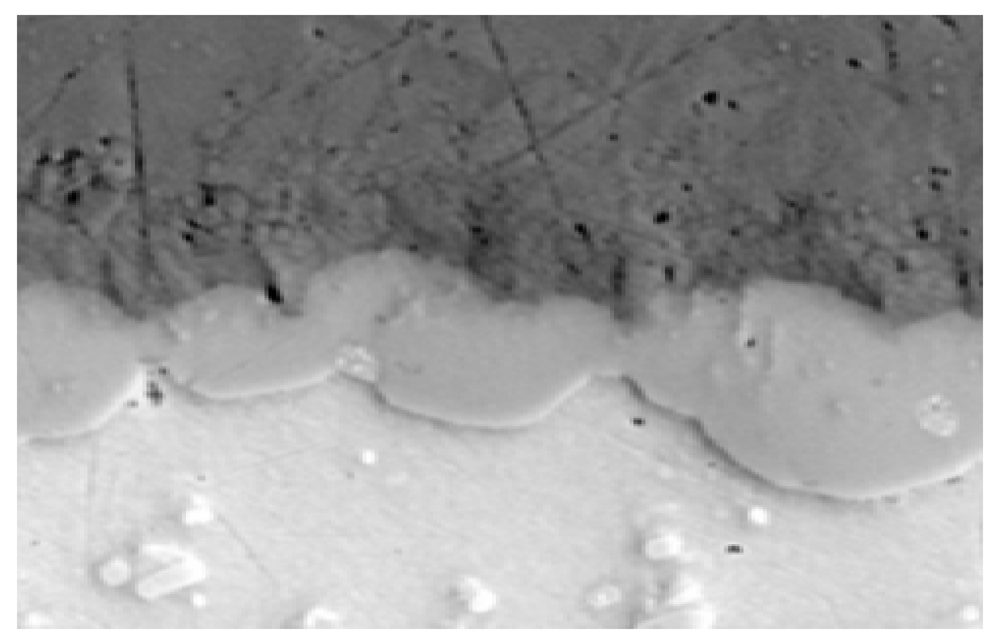
L Yin, et al., "Towards a better Understanding of the Effect of Cu Electroplating Process Parameters on Cu3Sn Voiding," JEM, V41, No.2, 2012

Solder Additives Mitigates IMC Voids

Joints Aged at 150 C for 1000 hrs



SAC



SAC + 0.6%Zn

Also Ni and Co addition into the solder reduce the Cu3Sn and voids.

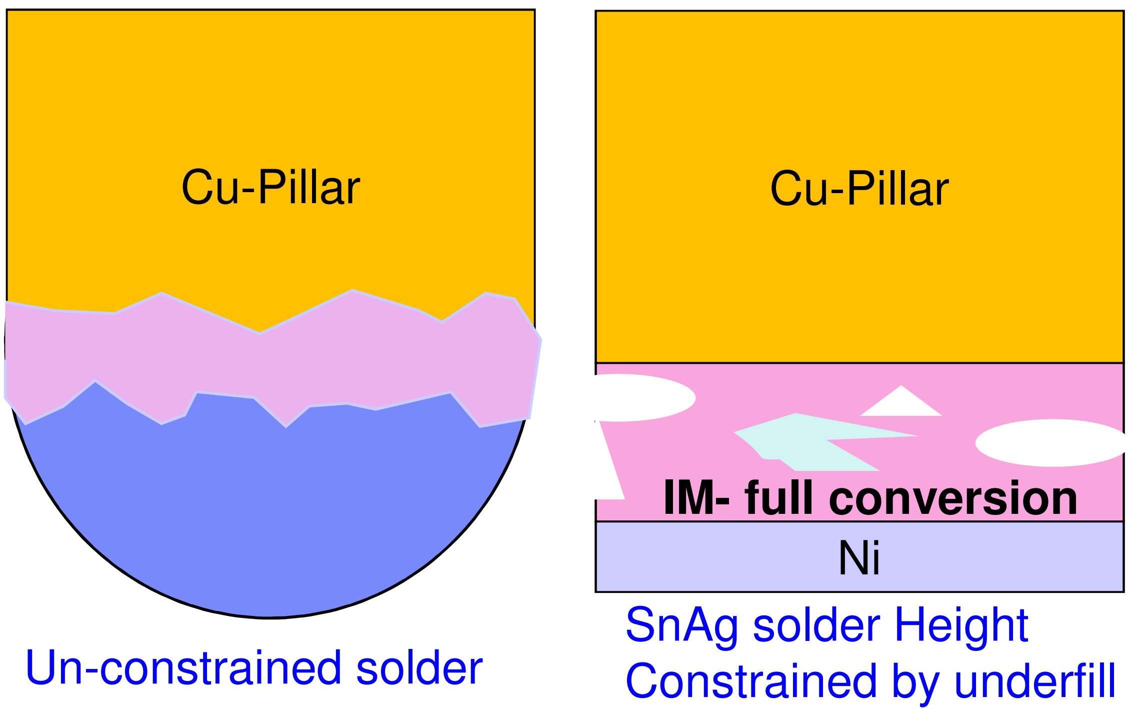
I. DeSousa, et. al., “The Influence of Low Level Doping on the Thermal Evolution of SAC Alloy Solder Joints with Cu Pad Structures,” ECTC 2006

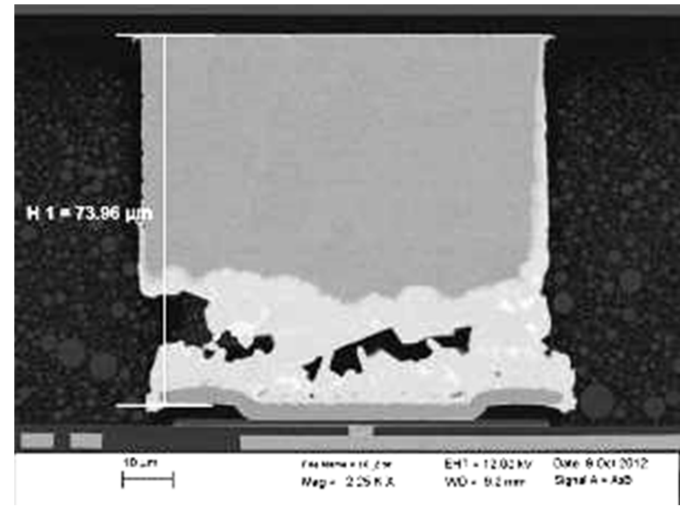
Thermal Stress Voids Through IMC Volume Reduction

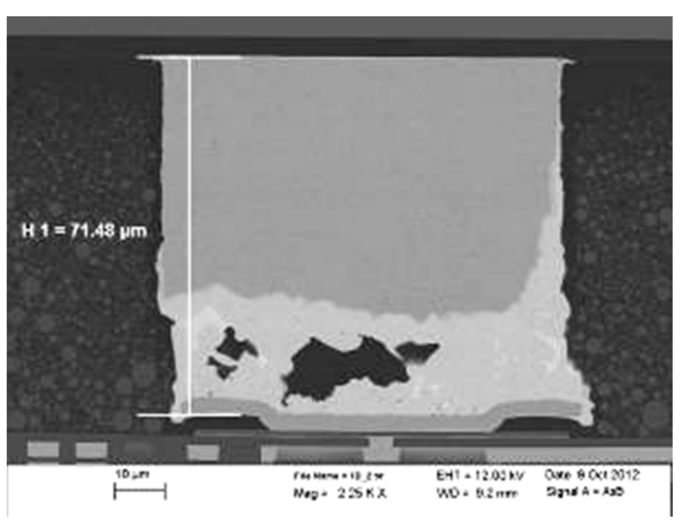
Volume decrease @ IM formation:

$6Cu + 5Sn \rightarrow Cu_6Sn_5 \rightarrow \sim 5\ \%$

$3Cu + Sn \rightarrow Cu_3Sn \rightarrow \sim 7.6\ \%$

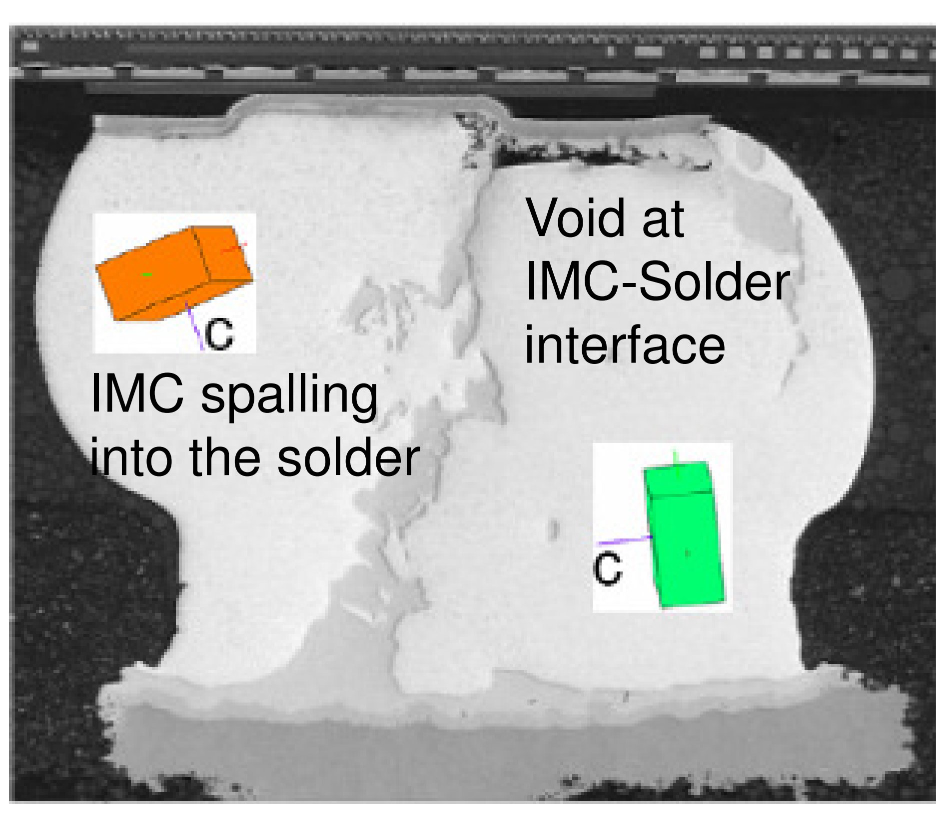






Voids and impurities migrate to the IMC center

Electromigration fails



M. Lu, et. al., “Comparison of Electromigration Performance for Pb-free Solders and Surface Finishes,” 2008 ECTC

x 10^3 A/cm^2
40.0
13.9
4.8
1.66
0.58
0.2

Current Density (x10^4 A/cm^2)
3.0
2.5
2.0
1.5
1.0
0.5
Z
X
Y

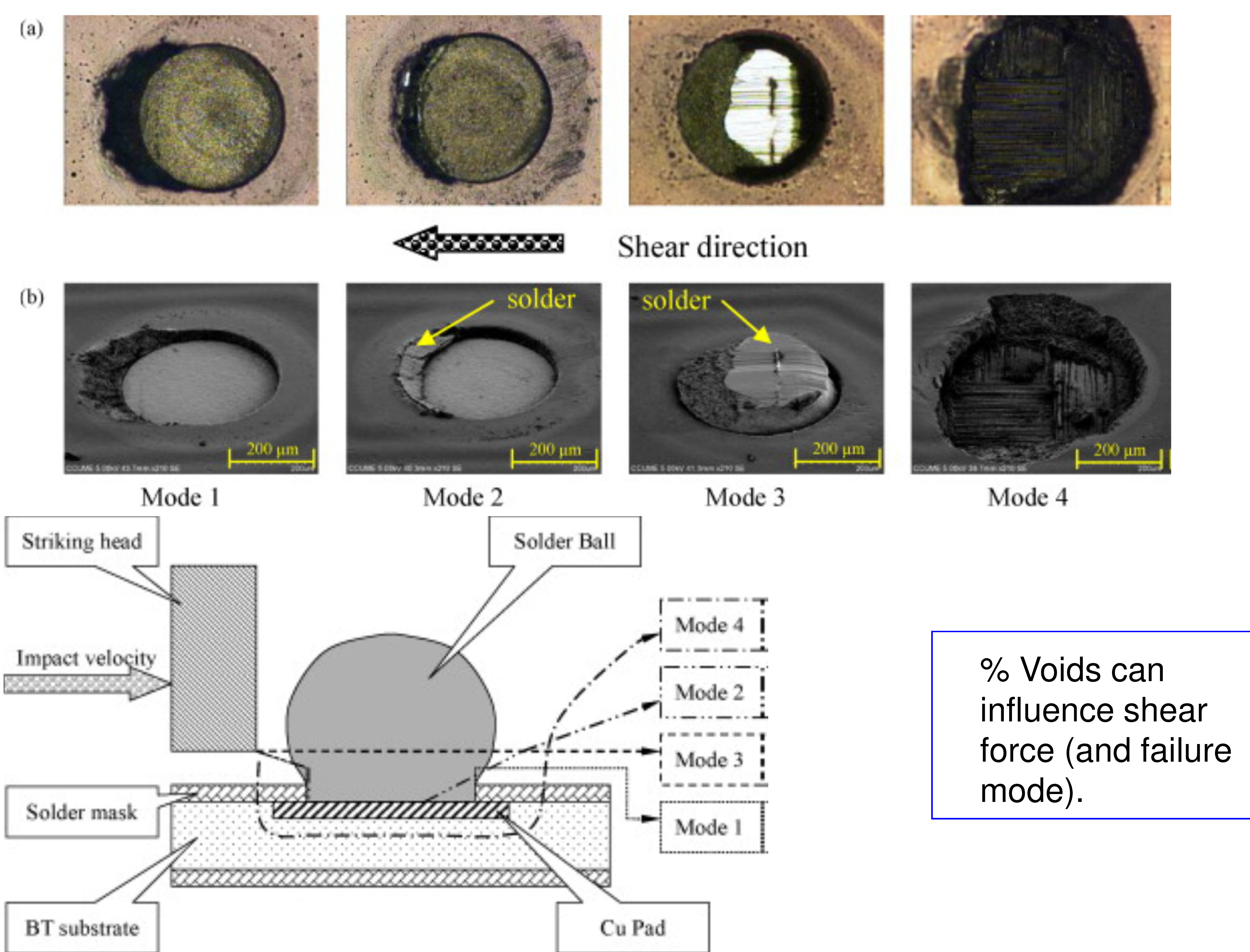
Current crowding:
Highest current density occurs at the point where the UBM meets the BEOL wiring

Chia-Ming Tsai, PhD Thesis

Testing Methods

▪ Ball Shear	Destructive
▪ Chip Pull	Destructive
▪ Ball Pull	Destructive
▪ X-ray (2D)	Non-Destructive
▪ X-ray tomography (3D)	Non-Destructive
▪ X-section	Destructive

Individual Solder Shear Test



% Voids can influence shear force (and failure mode).

C. Y. Lin, et. al., "Failure Mode Analysis of Lead-free Solder," 2008 ICEPT-HDP

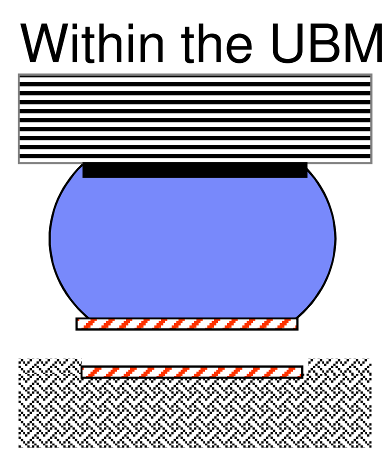
Chip Pull Testing

- Purpose
  - Destructive test to check for structure and process robustness.
  - Chip is attached to the organic carrier and pulled with an ingstron tool. Fail interfaces and pull strength is examined.
- Sample Chip Pulls (destructive)
  - Inspect for solder joints: good wetting, contact non-wets, non-contact non-wets
  - Large I/O chips require support substrate to prevent sample breakage.

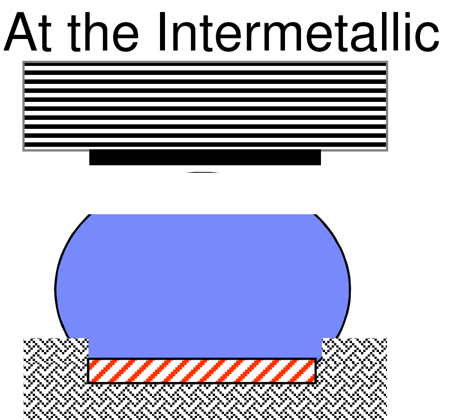
Failure modes

In the BEOL

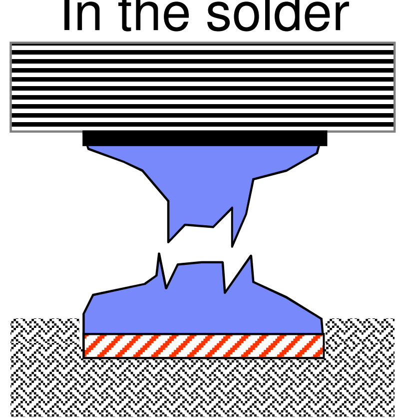
Within the UBM



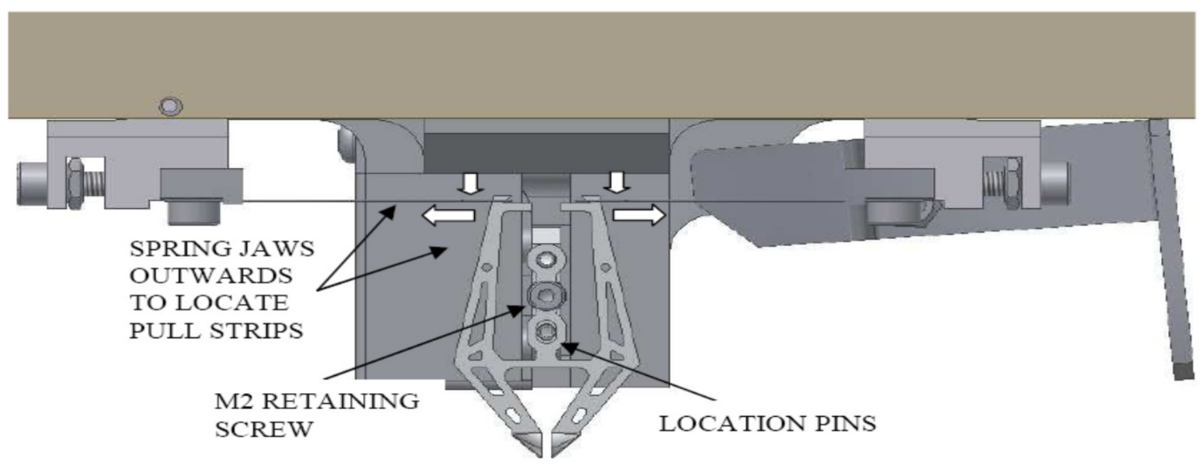
At the Intermetallic



In the solder



Individual Bump Pull Test



Dage tool Testing Setup:

- Test speed
  - 1000mm/s (high speed ball pull)
- Land force: 10 gram.

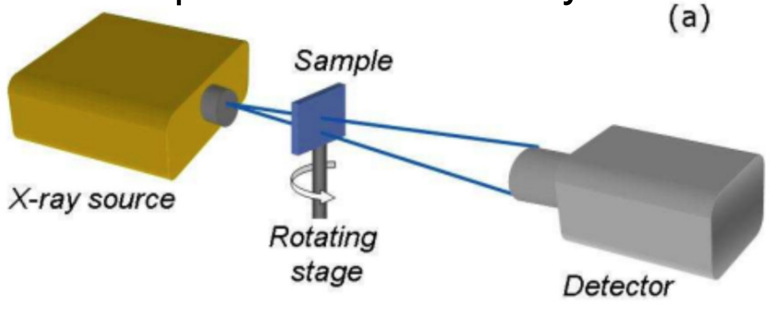
- Typical force: 60 gf
- Failed interfaces:
  - At solder
  - At BEOL (pulled out)
  - At UBM or intermetallic

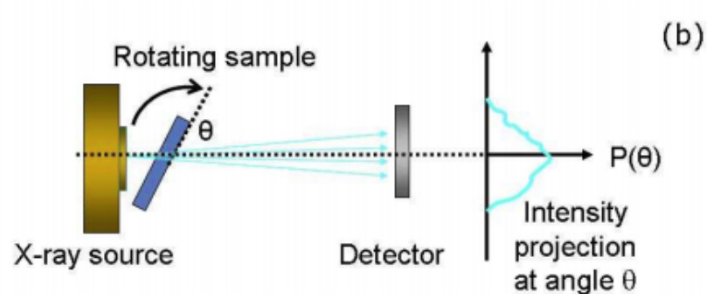
➔ New addition is automatic wire placement and wire pull.

3D X-Ray (X-Ray CT) Computed Tomography

3D X-Ray (X-Ray CT)

- 2D images are mathematically superimposed and processed to obtain a three dimensional map of the sample
- Virtual cross-sections at any give location. Resolution is limited by:
  - position wrt the source to freely rotate without hitting it.
  - the spot size of the x-ray source





M. Pacheco and D. Goyal, "Detection and Characterization of Defects in Microelectronic Packages and Boards by Means of High-Resolution X-Ray CT," 2011 ECTC

Physical x-sections

2D X-Ray image

Non-wet failing bump

Passing bump

3D-CT

Cracked joint

Good joint

Virtual Planar View

Virtual Cross Section View

X-Ray 2D Inspection

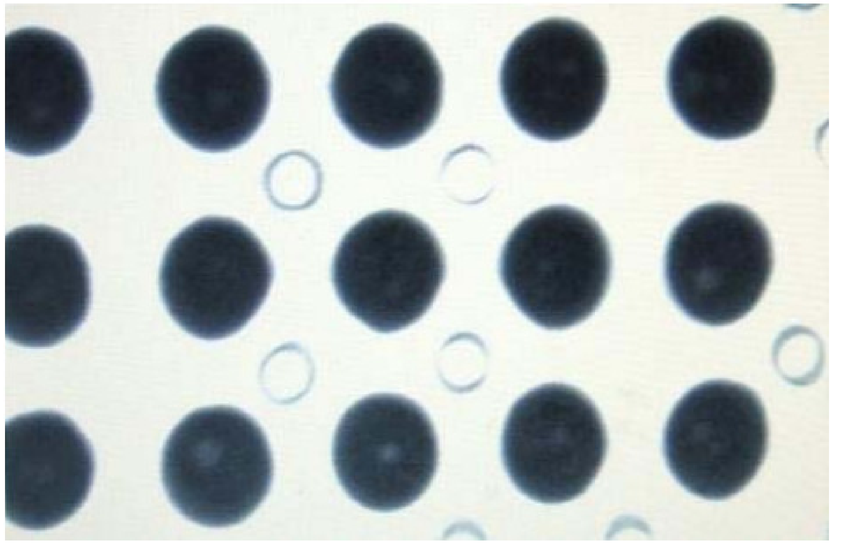
2D X-ray is the most common monitor tool for in-line solder void monitoring.

- BGS /CSP Package to substrate criteria:

Location of Void	Class I	Class II	Class III
Void in Solder (Solder Sphere)	60% of Diameter = 36% of Area	45% of Diameter = 20.25% of Area	30% of Diameter = 9% of Area
Void at Interface of Solder Sphere and Substrate	50% of Diameter = 25% of Area	35% of Diameter = 12.25% of Area	20% of Diameter = 4% of Area

Table 1: IPC 7095 Requirements for Void Classification

Michael A. Previti, et. al., "Four Ways to Reduce voids in BGA/CSP Package to Substrate Connections," Cookson Electronics

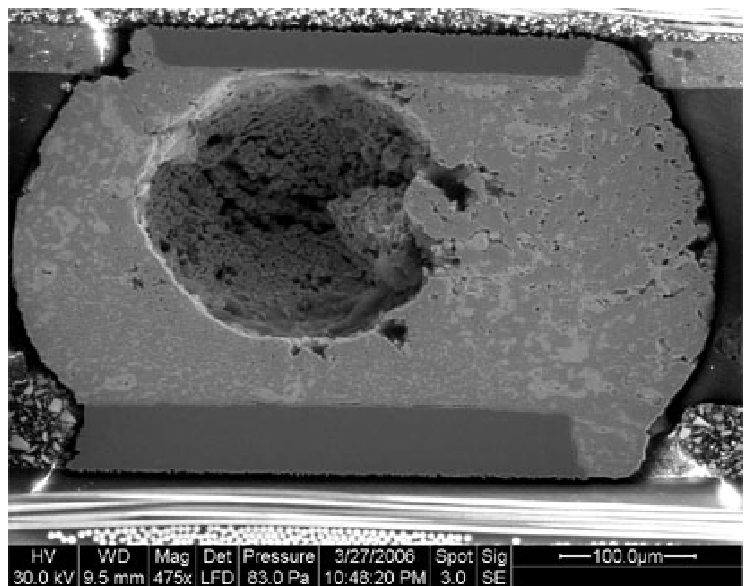


X-section Method for Void Detection

X-section options:

1) Mechanical polish for large voids

2) Focus Ion beam (FIB) for small voids



http://www.indium.com/blog/voiding-in-bgas.php / CALCE

Summary

- Pb-free solder interconnect in Flip Chip, Cu-Pillar, CSP, and BGA continues to grow each year. And one of the major defect types in Pb-free applications is solder voids.

- There are many root caused for solder voids: fabrication, assembly and life stress. Most of them are understood and structure or process changes are available to produce a more robust Pb-free interconnect.

- By looking at the voids size and location, a good prediction of its origin can be estimated.

- Additionally, there are several testing methods that are used to characterized and monitor the fabrication and assembly processes to control any process drift and void formation.

Thank you.