Thermal Design Basics

INTRODUCTION

For reliability reasons, integrated circuits handling appreciable power are increasingly called upon to observe *thermal management*. All semiconductors have some specified safe upper limit for junction temperature (T_J), usually on the order of 150°C (sometimes 175°C). Like maximum power supply voltages, maximum junction temperature is a worst case limitation which must not be exceeded. In conservative designs, it won't be approached by less than an ample safety margin. Note that this is critical, since semiconductor lifetime is inversely related to operating junction temperature. Simply put, the cooler ICs are, the more they can approach their maximum life.

This limitation of power and temperature is basic, and is illustrated by a typical data sheet statement as in Figure 1. In this case it is for the AD8017AR, an 8-pin SOIC device.

> *The maximum power that can be safely dissipated by the AD8017 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated device is determined by the glass transition temperature of the plastic, approximately +150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of +175°C for an extended period can result in device failure.*

Figure 1: Maximum Power Dissipation Data Sheet Statement for the AD8017AR, an ADI Thermally Enhanced SOIC Packaged Device

Tied to these statements are certain conditions of operation, such as the power dissipated by the device, and the package mounting specifics to the printed circuit board (PCB). In the case of the AD8017AR, the part is rated for 1.3 W of power at an ambient of 25°C. This assumes operation of the 8-lead SOIC package on a two-layer PCB with about 4 in^2 (~2500 mm^2) of 2 oz. copper for heat sinking purposes. Predicting safe operation for the device under other conditions is covered below.

THERMAL DESIGN BASICS

The symbol θ is generally used to denote *thermal resistance*. Thermal resistance is in units of °C/watt (°C/W). Unless otherwise specified, it defines the resistance heat encounters transferring from a hot IC junction to the ambient air. It might also be expressed more specifically as θ_{JA}, for *thermal resistance, junction-to-ambient*. θ_{JC} and θ_{CA} are two additional θ forms used, and are further explained below.

In general, a device with a thermal resistance θ equal to 100°C/W will exhibit a temperature differential of 100°C for a power dissipation of 1 W, as measured between two reference points. Note that this is a linear relationship, so 1 W of dissipation in this part will produce a 100°C differential (and so on, for other powers). For the AD8017AR example, θ is about 95°C/W, so 1.3 W of dissipation produces about a 124°C junction-to-ambient temperature differential. It is of course this rise in temperature that is used to predict the internal temperature, in order to judge the thermal reliability of a design. With the ambient at 25°C, this allows an internal junction temperature of about 150°C. In practice most ambient temperatures are above 25°C, so less power can then be handled.

For any power dissipation P (in watts), one can calculate the effective temperature differential (ΔT) in °C as:

$$\Delta T = P \times \theta \qquad\qquad \text{Eq. 1}$$

where θ is the total applicable thermal resistance. Figure 2 summarizes a number of basic thermal relationships.

◆ θ = **Thermal Resistance (°C/W)**
◆ **P = Total Device Power Dissipation (W)**
◆ **T = Temperature (°C)**
◆ **ΔT = Temperature Differential = P × θ**
◆ θ_{JA} = **Junction-Ambient Thermal Resistance**
◆ θ_{JC} = **Junction-Case Thermal Resistance**
◆ θ_{CA} = **Case-Ambient Thermal Resistance**
◆ $\theta_{JA} = \theta_{JC} + \theta_{CA}$
◆ $T_J = T_A + (P \times \theta_{JA})$
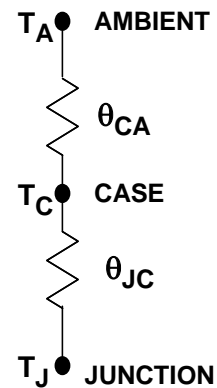◆ *Note: $T_{J(Max)}$ = 150°C (Sometimes 175°C)*

Figure 2: Basic Thermal Relationships

Note that series thermal resistances, such as the two shown at the right, model the total thermal resistance path a device may see. Therefore the total θ for calculation purposes is the sum, i.e., $\theta_{JA} = \theta_{JC} + \theta_{CA}$. Given the ambient temperature T_A, P, and θ, then T_J can be calculated. As the relationships signify, to maintain a low T_J, either θ or the power being dissipated (or both) must be kept low. A low ΔT is the key to extending semiconductor lifetimes, as it leads to lower maximum junction temperatures.

In ICs, one temperature reference point is always the device junction, taken to mean the hottest spot inside the chip operating within a given package. The other relevant reference point will be either T_C, the case of the device, or T_A, that of the surrounding air. This then leads in turn to the above mentioned individual thermal resistances, θ_{JC} and θ_{JA}.

Taking the most simple case first, θ_{JA} is the thermal resistance of a given device measured between its *junction* and the *ambient* air. This thermal resistance is most often used with small, relatively low power ICs such as op amps, which often dissipate 1 W or less. Generally, θ_{JA} figures typical of op amps and other small devices are on the order of 90-100°C/W for a plastic 8-pin DIP package, as well as the better SOIC packages.

It should be clearly understood that these thermal resistances are *highly* package dependent, as different materials have different degrees of thermal conductivity. As a general guideline, thermal resistance of conductors is analogous to electrical resistances, that is copper is the best, followed by aluminum, steel, and so on. Thus copper lead frame packages offer the highest performance, i.e., the lowest θ.

HEAT SINKING

By definition, a *heat sink* is an added low thermal resistance device attached to an IC to aid heat removal. A heat sink has additional thermal resistance of its own, θ_{CA}, rated in °C/W. However, most current op amp packages don't easily lend themselves to heat sink attachment (exceptions are older TO-99 metal can types). Devices meant for heat sink attachment will often be noted by a θ_{JC} dramatically lower than the θ_{JA}. In this case θ will be composed of more than one component. Thermal impedances add, making a net calculation relatively simple. For example, to compute a net θ_{JA} given a relevant θ_{JC}, the thermal resistance of the heat sink, θ_{CA}, or *case* to *ambient* is added to the θ_{JC} as:

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \hspace{3cm} \text{Eq. 2}$$

and the result is the θ_{JA} for that specific circumstance.

More generally however, modern ICs *don't* use commercially available heat sinks. Instead, when significant power needs to be dissipated, such as $\geq$ 1 W, low thermal resistance copper PCB traces are used as the heat sink. In such cases, the most useful form of manufacturer data for this heat sinking are the boundary conditions of a sample PCB layout, and the resulting θ_{JA} for those conditions. This is in fact the type of specific information supplied for the AD8017AR, as mentioned earlier. Applying this approach, example data illustrating thermal relationships for such conditions is shown by Figure 3. These data apply for an AD8017AR mounted to a heat sink with an area of about 4 square inches on a 2 layer, 2 ounce copper PCB.

These curves indicate the maximum power dissipation vs. temperature characteristic for the AD8017, for maximum junction temperatures of both 150°C and 125°C. Such curves are often referred to as *derating* curves, since allowable power decreases with ambient temperature.
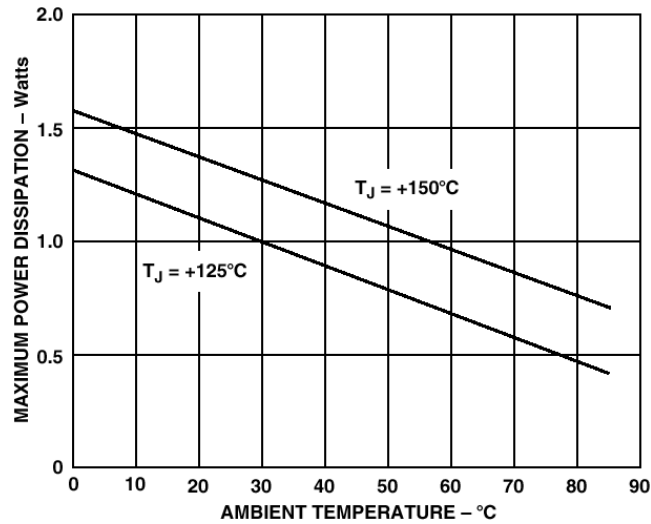
Figure 3: Thermal Rating Curves for AD8017AR Op Amp

With the AD8017AR, the proprietary ADI *Thermal Coastline* IC package is used, which allows additional power to be dissipated with no increase in the SO-8 package size. For a $T_{J(max)}$ of 150°C, the upper curve shows the allowable power in this package, which is 1.3 W at an ambient of 25°C. If a more conservative $T_{J(max)}$ of 125°C is used, the lower of the two curves applies.

A performance comparison for an 8-pin standard SOIC and the ADI Thermal Coastline version is shown in Figure 4. Note that the Thermal Coastline provides an allowable dissipation at 25°C of 1.3 W, whereas a standard package allows only 0.8 W. In the Thermal Coastline heat transferal is increased, accounting for the package's lower θ_{JA}.
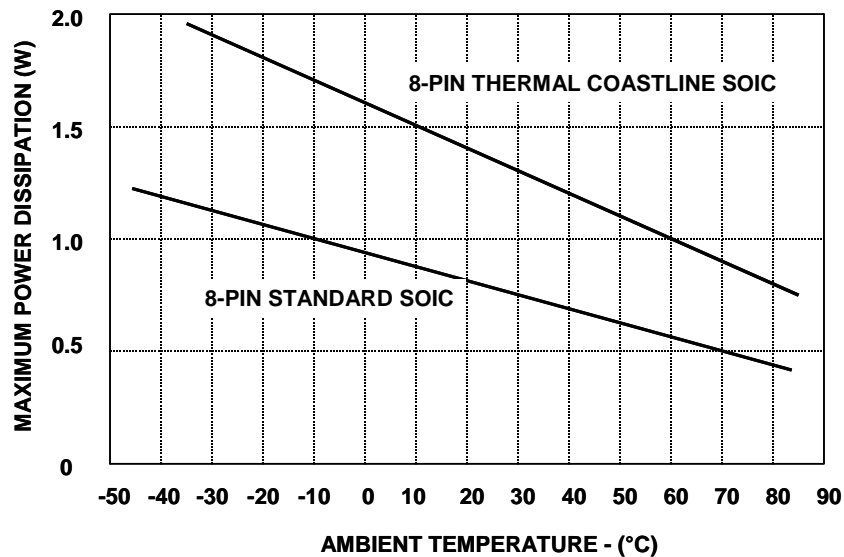

Figure 4: Thermal Rating Curves for Standard (Lower) and ADI Thermal Coastline (Upper) 8-Pin SOIC Packages

Even higher power dissipation is possible, with the use of IC packages better able to transfer heat from chip to PCB. An example is the AD8016 ADSL line driver device, available with two package options rated for 5.5 and 3.5 W at 25°C, respectively, as shown in Figure 5.

Taking the higher rated power option, the AD8016ARP PSOP3 package, when used with a 10 inch² 1 oz. heat sink plane, the combination is able to handle up to 3 W of power at an ambient of 70°C, as noted by the upper curve. This corresponds to a θ_{JA} of 18°C/W, which in this case applies for a maximum junction temperature of 125°C.
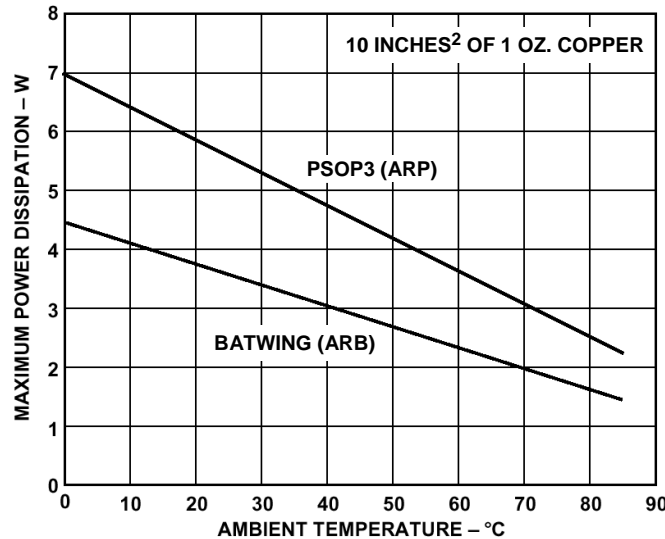

Figure 5: Thermal Characteristic Curves for the AD8016 BATWING (Lower) and PSOP3 (Upper) Packages, for T$_{J(Max)}$ Equal to 125°C

The reason the PSOP3 version of the AD8016 is so better able to handle power lies with the use of a large area copper slug. Internally, the IC die rest directly on this slug, with the bottom surface exposed as shown in Figure 6. The intent is that this surface be soldered directly to a copper plane of the PCB, thereby extending the heat sinking.
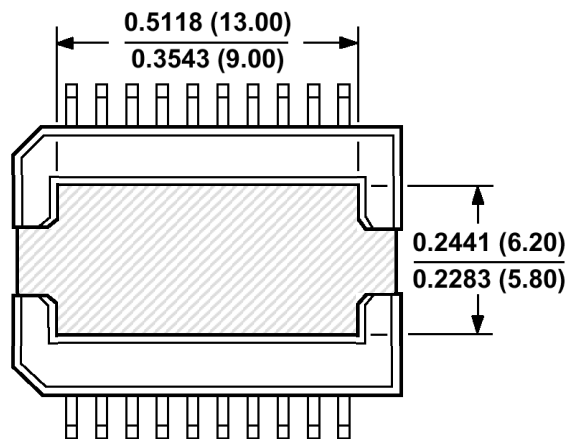

Figure 6: Bottom View of AD8016 20-Lead PSOP3 Package Showing Copper Slug for Aid in Heat Transfer (Central Grayed Area)

Both of the AD8016 package options are characterized for both still and moving air, but the thermal information given above applies *without* the use of directed airflow. Therefore, adding additional airflow lowers thermal resistance further (see Reference 2).

For reliable, low thermal resistance designs with op amps, several design *Do's and Don'ts* are listed below. Consider all of these points, as may be practical.

1. Do use as large an area of copper as possible for a PCB heat sink, up to the point of diminishing returns.

2. In conjunction with 1), do use multiple (outside) PCB layers, connected together with multiple vias.

3. Do use as heavy copper as is practical (2 oz. or more preferred).

4. Do provide sufficient natural ventilation inlets and outlets within the system, to allow heat to freely move away from hot PCB surfaces.

5. Do orient power-dissipating PCB planes vertically, for convection-aided airflow across heat sink areas.

6. Do consider the use of external power buffer stages, for precision op amp applications.

7. Do consider the use of forced air, for situations where several watts must be dissipated in a confined space.

8. Don't use solder mask planes over heat dissipating traces.

9. Don't use excessive supply voltages on ICs delivering power.

For the most part, these points are obvious. However, one that could use some elaboration is number 9. Whenever an application requires only modest *voltage* swings (such as for example standard video, 2 V p-p) a wide supply voltage range can often be used. But, as the data of Figure 7 indicates, operation of an op amp driver on higher supply voltages produces a large IC dissipation, even though the load power is constant.

In such cases, as long as the distortion performance of the application doesn't suffer, it can be advantageous to operate the IC on lower supplies, say ±5 V, as opposed to ±15 V. The above example data was calculated on a dc basis, which will generally tax the driver more in terms of power than a sine wave or a noise-like waveform, such as a DMT signal (see Reference 2). The general principles still hold for these ac waveforms, i.e., the op amp power dissipation is high when load current is high and the voltage low.
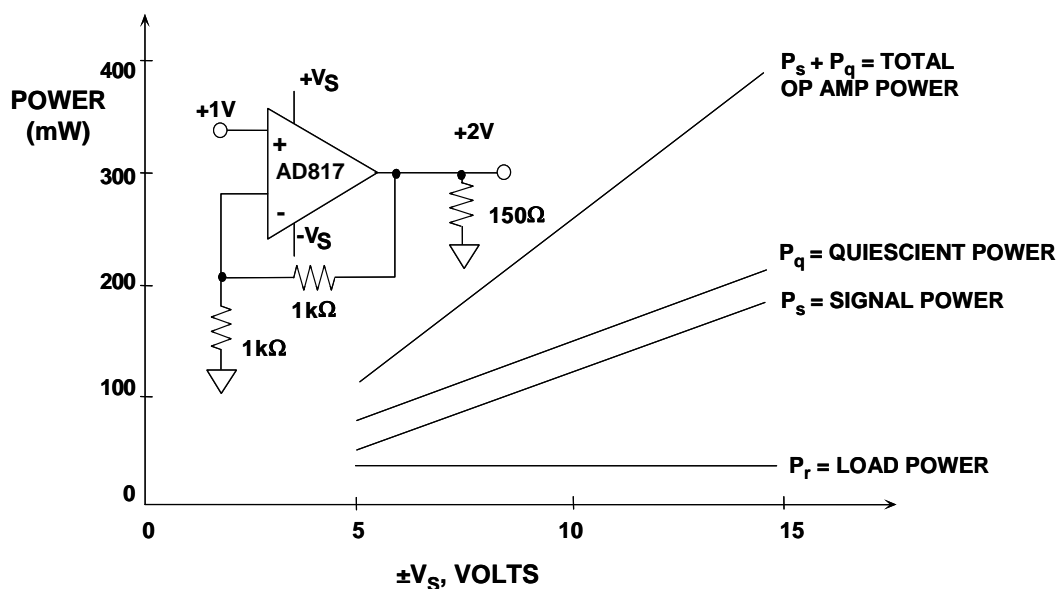
Figure 7: Power Dissipated in Video Op Amp Driver for Various Supply Voltages With Low Voltage Output Swing

While there is ample opportunity for high power handling with the thermally enhanced packages described above for the AD8016 and AD8017, the increasingly popular smaller IC packages actually move in an opposite direction. Without question, it is true that today's smaller packages do noticeably sacrifice thermal performance. But, it must be understood that this is done in the interest of realizing a smaller size for the packaged op amp, and, ultimately, a much greater final PCB density for the overall system.

These points are illustrated by the thermal ratings for the AD8057 and AD8058 family of single and dual op amp devices, as is shown in Figure 8. The AD8057 and AD8058 op amps are available in three different packages. These are the SOT-23-5, and the 8-pin μSOIC, along with standard SOIC.

As the data shows, as the package size becomes smaller and smaller, much less power is capable of being removed. Since the lead frame is the only heatsinking possible with such tiny packages, their thermal performance is thus reduced. The θ_{JA} for the packages mentioned is 240, 200, and 160°C/W, respectively. Note this is more of a *package* than *device* limitation. Other ICs with the same packages have similar characteristics.

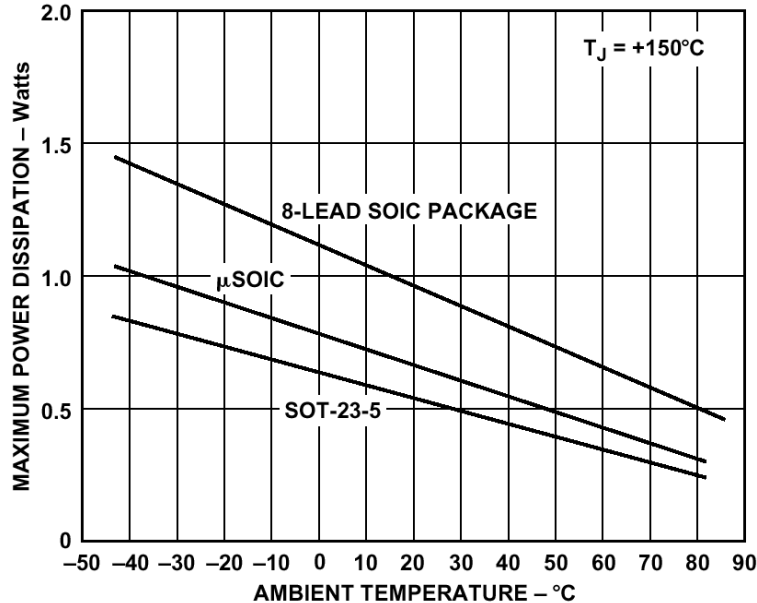**Figure 8: Comparative Thermal Performance for Several AD8057/58 Op Amp Package Options**

DATA CONVERTER THERMAL CONSIDERATIONS

At first glance, one might assume that the power dissipation of an ADC or a DAC will remain constant for a given power supply voltage. However, many data converters, especially CMOS ones, have power dissipations that are highly dependent upon not only output data loading but also the sampling clock frequency. Since many of the newer high-speed converters can dissipate between 1.5 and 2 W maximum power under the worst case operating conditions, this point must be well understood in order to ensure that the package is mounted in such a way as to maintain the junction temperature within acceptable limits at the highest expected operating temperature.

The discussion on grounding in Tutorial MT-031 emphasized that the digital outputs of high performance ADCs, especially those with parallel outputs, should be lightly loaded (5-10 pF) in order to prevent digital transient currents from corrupting the SNR and SFDR. Even under light output loading, however, most CMOS and BiCMOS ADCs have power dissipations which are a function of sampling clock frequency and in some cases, the analog input frequency and amplitude.

For example, Figure 9 shows the AD9245 14-bit, 80-MSPS, 3-V CMOS ADC power dissipation versus frequency for a 2.5-MHz analog input and 5-pF output loading of the data lines. The graphs show the digital and analog power supply currents separately as well as the total power dissipation. Note that total power dissipation can vary between approximately 310 mW and 380 mW as the sampling frequency is varied between 10 and 80 MSPS.
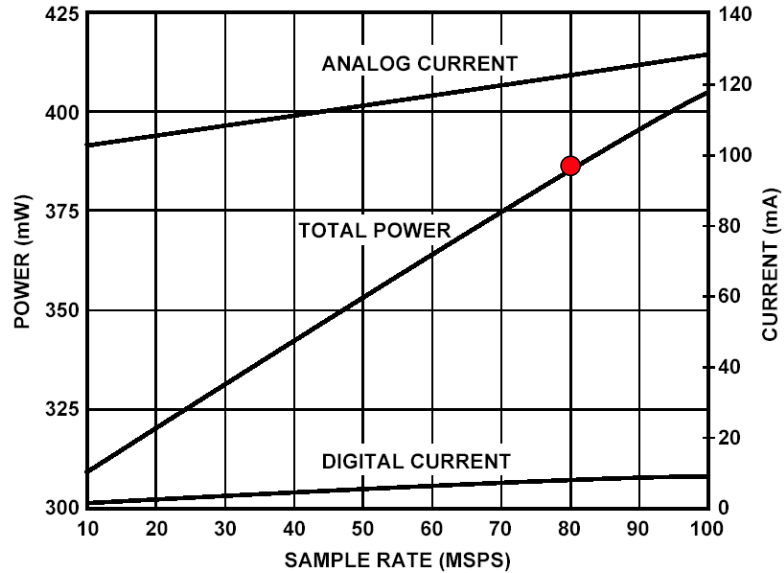
Figure 9: AD9245 14-Bit, 80-MSPS, 3-V CMOS ADC Power Dissipation vs. Sample Rate for 2.5-MHz Input, 5-pF Output Loads

The AD9245 is packaged in a 32-pin leadless chip scale package as shown in Figure 10. The bottom view of the package shows the exposed paddle which should be soldered to the PC board ground plane for best thermal transfer. The worst-case package junction-to-ambient resistance, θ_{JA}, is specified as 32.5°C/W, which places the junction 32.5°C $\times$ 0.38 = 12.3°C above the ambient for a power dissipation of 380 mW. For a maximum operating temperature of +85°C, this places the junction at a modest 85°C + 12.3°C = 97.3°C.
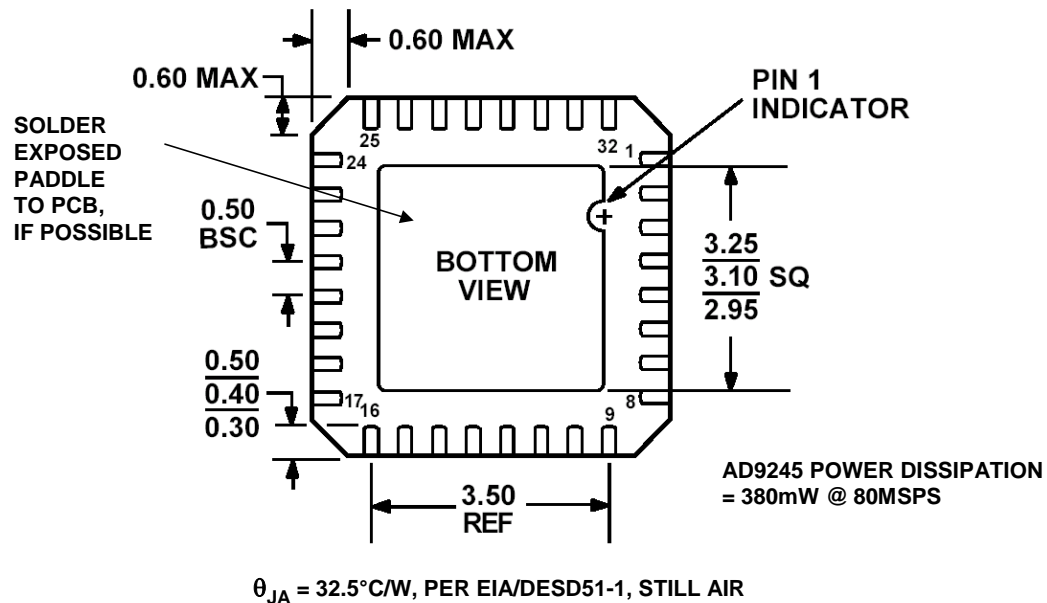

Figure 10: AD9245 CP-32 Lead-Frame Chip-Scale Package (LFCSP), Bottom View

The AD9430 is a high performance 12-bit, 170-/210-MSPS 3.3-V BiCMOS ADC. Two output modes are available: dual 105-MSPS demultiplexed CMOS outputs, or 210-MSPS LVDS outputs. Power dissipation as a function of sampling frequency is shown in Figure 11. Analog and digital supply currents are shown for CMOS and LVDS modes for an analog input frequency of 10.3 MHz. Note that in the LVDS mode and a sampling frequency of 210 MSPS, total supply current is approximately 455 mA—yielding a total power dissipation of 1.5 W.
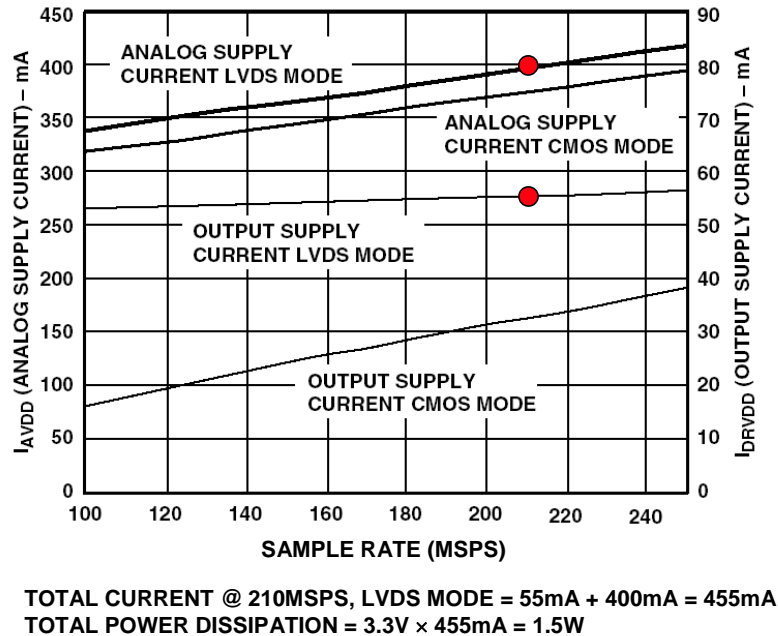

TOTAL CURRENT @ 210MSPS, LVDS MODE = 55mA + 400mA = 455mA
TOTAL POWER DISSIPATION = 3.3V × 455mA = 1.5W

*Figure 11: AD9430 12-Bit 170-/210-MSPS ADC Supply
Current vs.Sample Rate for 10.3-MHz Input*

The AD9430 is available in a 100-lead thin plastic quad flat package with an exposed pad (TQFP/EP) as shown in Figure 12. The conducive pad is connected to chip ground and should be soldered to the PC board ground plane. The θ_{JA} of the package when soldered to the ground plane is 25°C/W in still air. This places the junction 25°C × 1.5 = 37.5°C above the ambient temperature for 1.5 W of power dissipation. For a maximum operating temperature of +85°C, this places the junction at 85°C + 37.5°C = 122.5°C.

16.00 SQ

SOLDER HEAT SLUG
TO GROUND PLANE
IF POSSIBLE

STILL AIR:

θ_{JA} = 25°C/W, SOLDERED

θ_{JA} = 32°C/W, UNSOLDERED

AD9430 POWER DISSIPATION
IN LVDS MODE @ 210MSPS
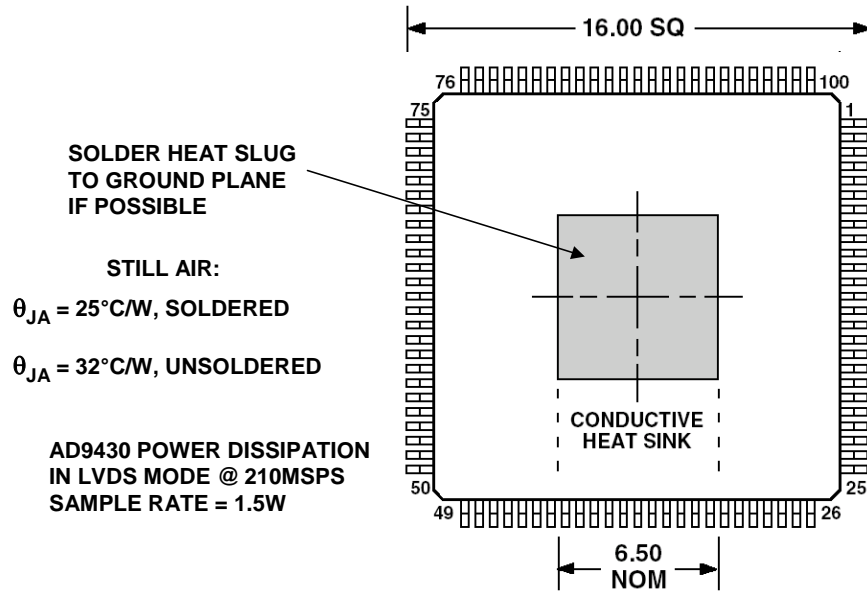SAMPLE RATE = 1.5W

CONDUCTIVE
HEAT SINK

6.50
NOM

Figure 12: AD9430 100-Lead e-PAD TQFP

The AD6645 is a high performance 14-bit, 80-/105-MSPS ADC fabricated on a high speed complementary bipolar process (XFCB), and offers high SFDR (89 dBc) and SNR (75 dB). Although there is little variation in power as a function of sampling frequency, the maximum power dissipation of the device is 1.75 W. The package is a thermally enhanced 52-lead PowerQuad 4® with an exposed pad as shown in Figure 13.
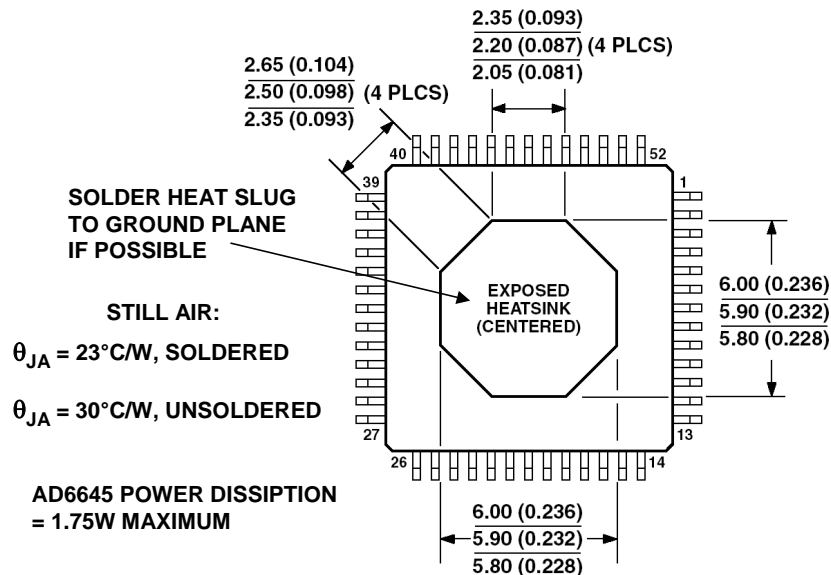

2.35 (0.093)
2.20 (0.087) (4 PLCS)
2.05 (0.081)

2.65 (0.104)
2.50 (0.098) (4 PLCS)
2.35 (0.093)

SOLDER HEAT SLUG
TO GROUND PLANE
IF POSSIBLE

STILL AIR:

θ_{JA} = 23°C/W, SOLDERED

θ_{JA} = 30°C/W, UNSOLDERED

AD6645 POWER DISSIPTION
= 1.75W MAXIMUM

EXPOSED
HEATSINK
(CENTERED)

6.00 (0.236)
5.90 (0.232)
5.80 (0.228)

6.00 (0.236)
5.90 (0.232)
5.80 (0.228)

Figure 13:AD6645 52-Lead Power-Quad 4 (LQFP_ED)
(SQ-52) Thermally Enhanced Package, Bottom View

It is recommended that the exposed center heatsink be soldered to the PC board ground plane to reduce the package θ_{JA} to 23°C/W in still air. For 1.75 W of power dissipation, this places the junction temperature 23°C × 1.75 = 40.3°C above the ambient temperature. For a maximum operating temperature of +85°C, this places the junction at 85°C + 40.3°C = 125.3°C. The thermal resistance of the package can be reduced to 17°C/W with 200 LFPM airflow, thereby reducing the junction temperature to 30°C above the ambient, or 115°C for an operating ambient temperature of +85°C.

High speed CMOS DACs (such as the TxDAC® series) and DDS ICs (such as the AD985x series) also have clock-rate dependent power dissipation. For example, in the case of the AD9777 16-bit, 160-MSPS dual interpolating DAC, power dissipation is a function of clock rate, output frequency, and the enabling of the PLL and the modulation functions. Power dissipation on 3.3-V supplies can range from 380 mW (f_{DAC} = 100 MSPS, f_{OUT} = 1 MHz, no interpolation, no modulation) to 1.75 W (f_{DAC} = 400 MSPS, f_{DATA} = 50 MHz, $f_s/2$ modulation, PLL enabled). These and similar parts in the family are also offered in thermally enhanced packages with exposed pads for soldering to the PC board ground plane.

Further detail on thermal and manufacturing aspects of LFCSP packages can be found in Reference 4.

SUMMARY

These discussions on the thermal application issues of op amps and data converters haven't dealt with the classic techniques of using clip-on (or bolt-on) type heat sinks. They also have not addressed the use of forced air cooling, generally considered only when tens of watts must be handled. These omissions are mainly because these approaches are seldom possible or practical with today's op amp and data converter packages.

The more general discussions within References 5-7 can be consulted for this and other supplementary information.

An interactive design tool, Power Dissipation vs. Die Temperature Calculator, is available on the Analog Devices' website to aid in performing thermal calculations with external heatsinks.

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